Figures and tables for 4.1

Current & voltage	1200 V, 25 A (phase-leg rating)
Cooling	Single side cooled
Coolant temp / back pressure etc	N/A: cold plate, max temperature 115 °C
Choice of SiC die	SiC JFET plus Schottky diode
Electrical and thermal specification	Half bridge (leg) per substrate junction temperature range -60 to 200 °C

Table 1 Original project Specification

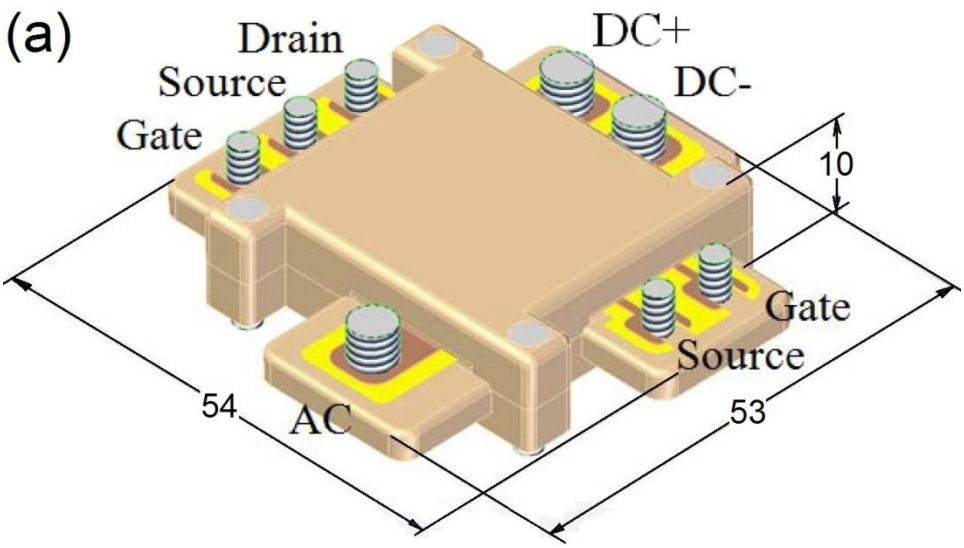

Figure 1 3D View of the Power module

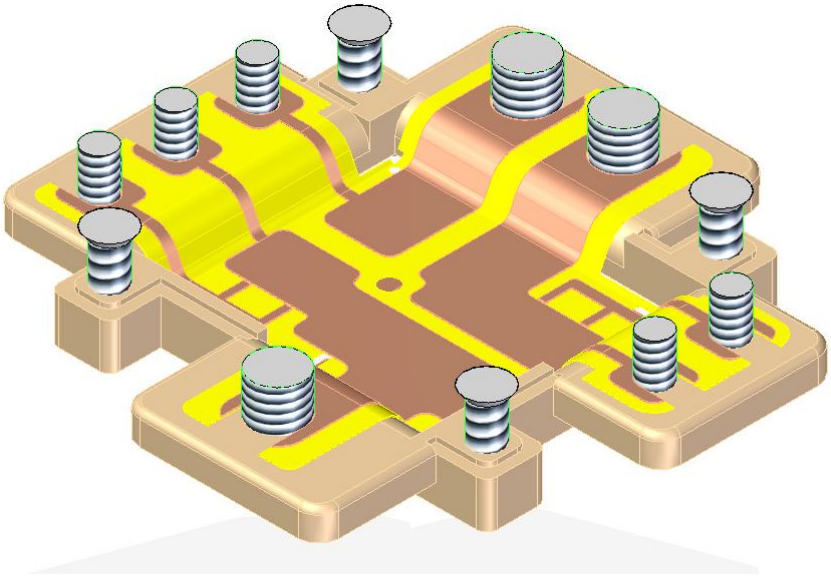

Figure 2 View of power module without lid

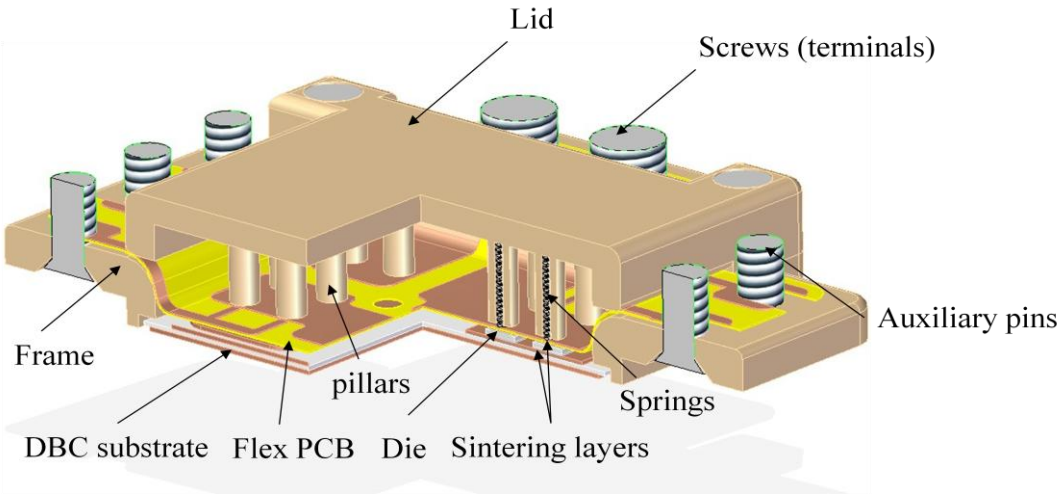

Figure 3 Cross section of the whole module

Component	Material Specification
Switch (JFET)	1200 V, 3.07×3.07×0.35 mm, SiC
Diode	1200 V, 2.35×2.35×0.35 mm SiC
Substrate	Silicon Nitride with silver finish
Supports	Copper (6×3×0.35 mm)
Die attachment	Nano Ag paste
Encapsulant	Silicone gel
Flex PCB	Kapton sandwiched with copper foil
Plastic	Tecator

Table 2 Material selection list

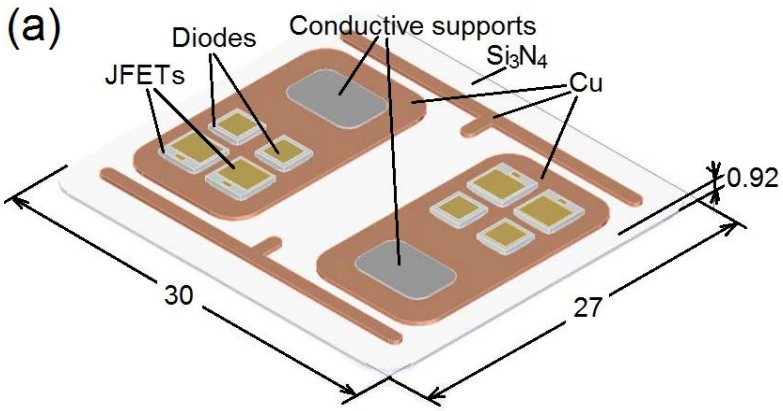

Figure 4 Substrate outline

	Materials	Thickness(mm)
Ceramic	Si_3N_4	0.32
DBC	Cu with Ag plating	0.3
Ag	Ag finish	<0.01

Table 3 substrate material specification

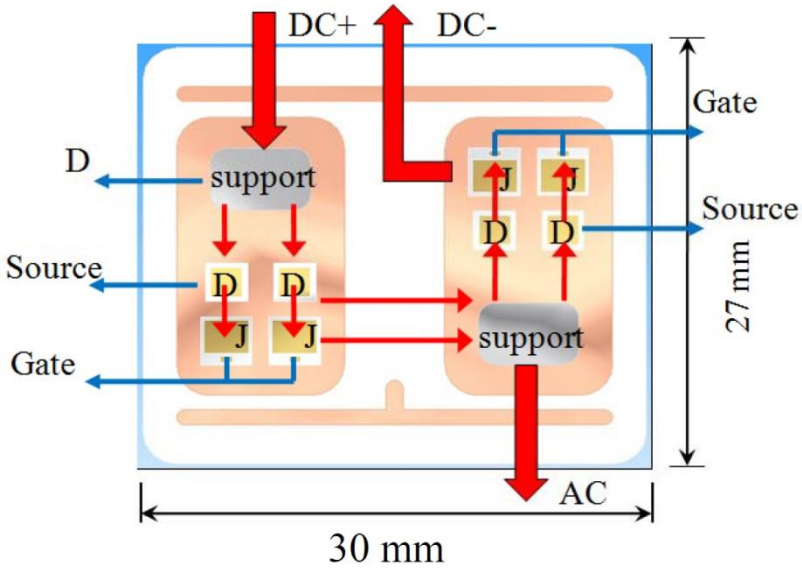

Figure 5 electrical layout

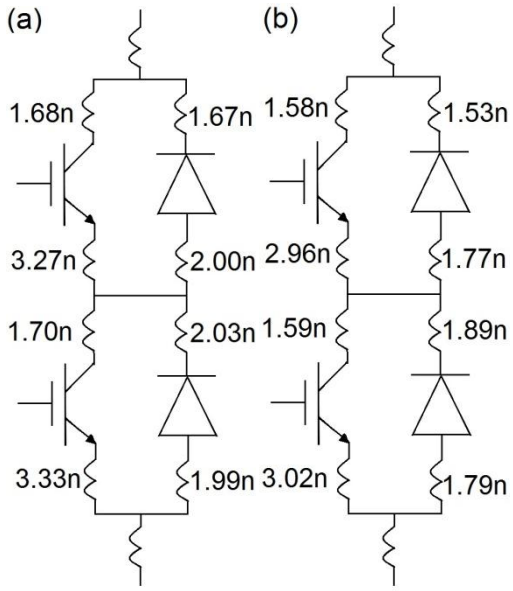

Figure 6 Equivalent circuit with extracted inductance at (a) 1kHz (b) 100kHz

	Materials	Thickness(mm)
Polymer1	Polyimide	0.1
Metal layer	Cu with Ag plating	0.1
Metal via	Cu	Ø0.2
Polymer2	Polyimide	0.05

Table 4 PCB material specification

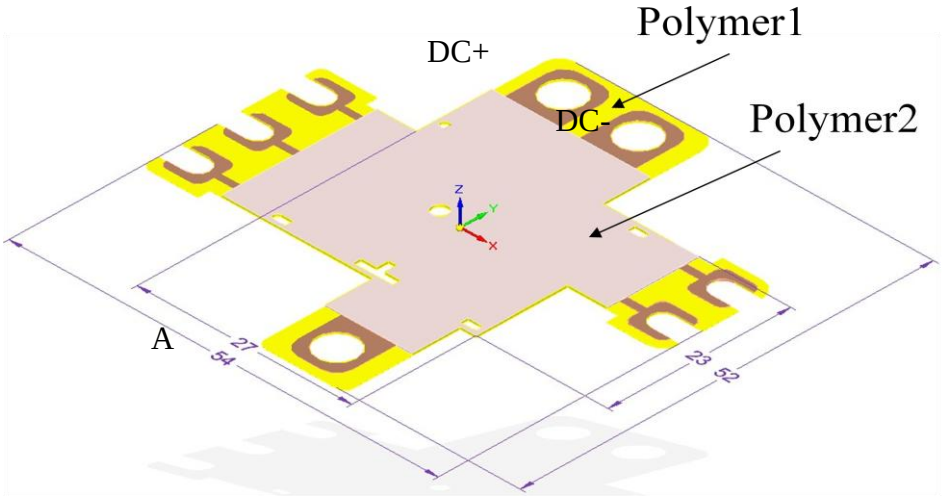

Figure 7 PCB Layout

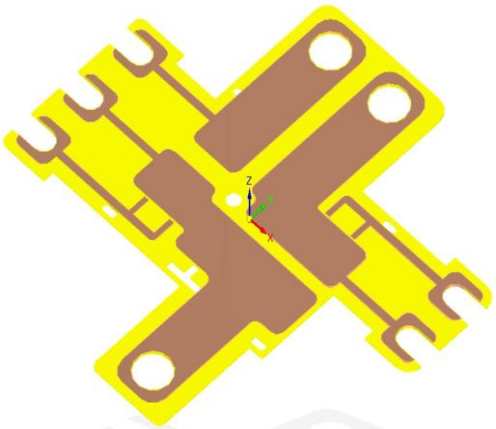

Figure 8 Top metal of PCB Layout

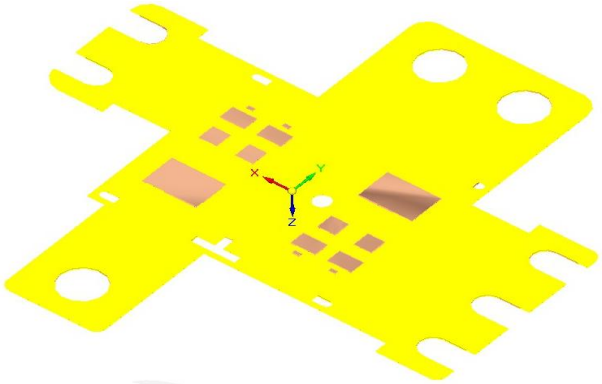

Figure 9 PCB Backside metal layout

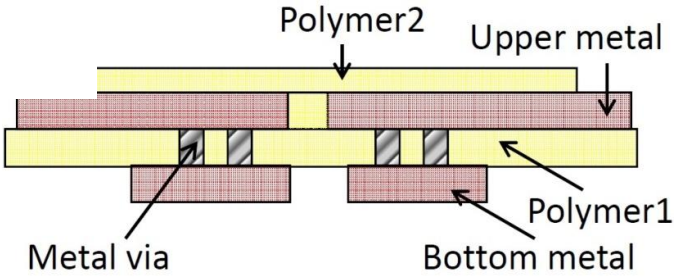

Figure 10 Cross section of PCB

.

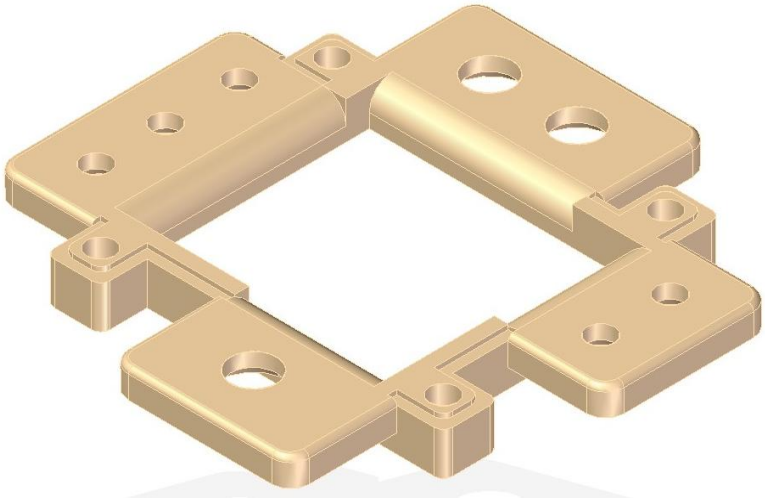

Figure 11 3D profile of the plastic frame

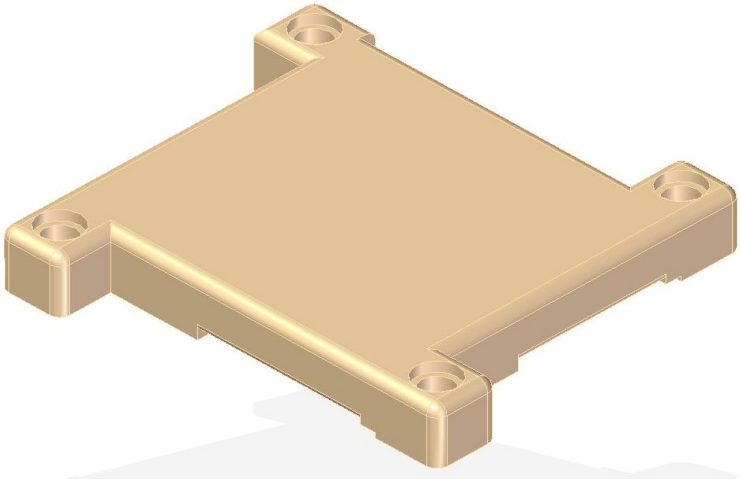

Figure 12 3D profile of the plastic lid

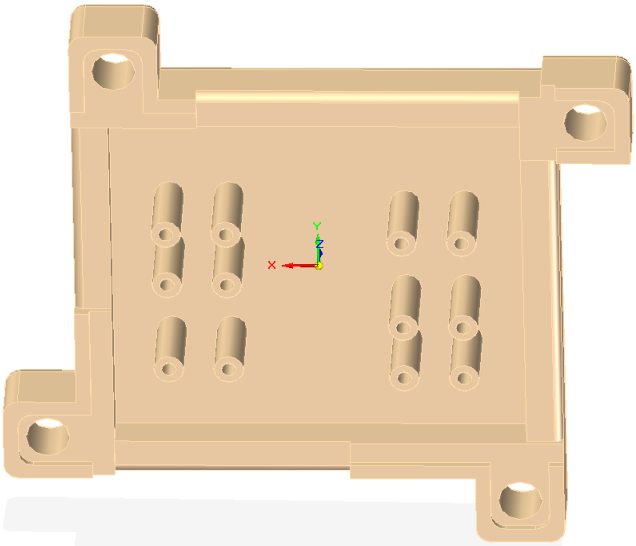

Figure 13 Backside view of the plastic pillars

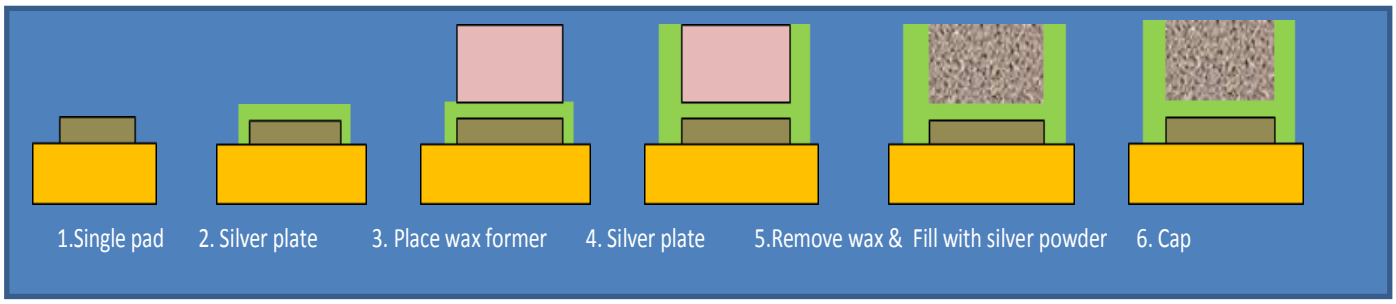

Figure 14 Schematic of Selective layer additive Manufacture process

.

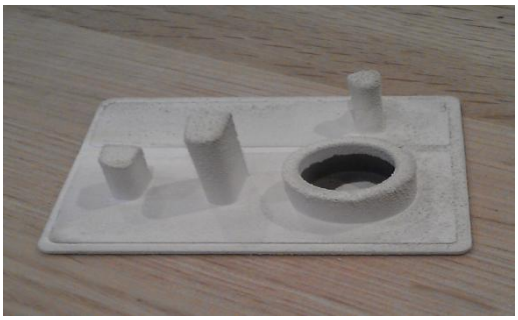

Figure 15 Silver plated wax coupons

Figure 16 Development Plating Tank

Figure 17 Thermal shock equipment

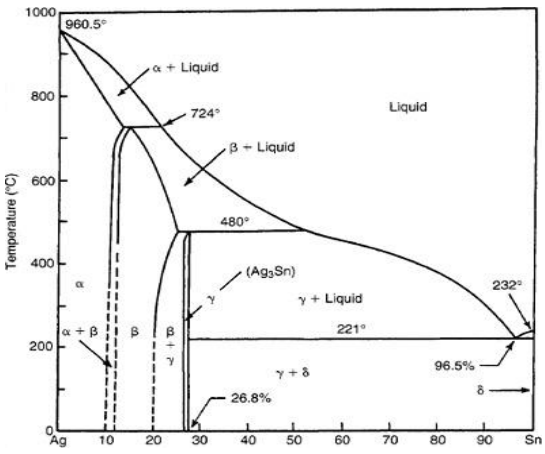

Figure 18 Equilibrium Diagram

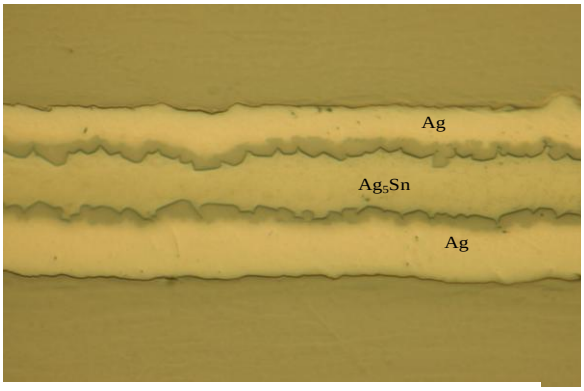

Figure 19 Multi layer plating

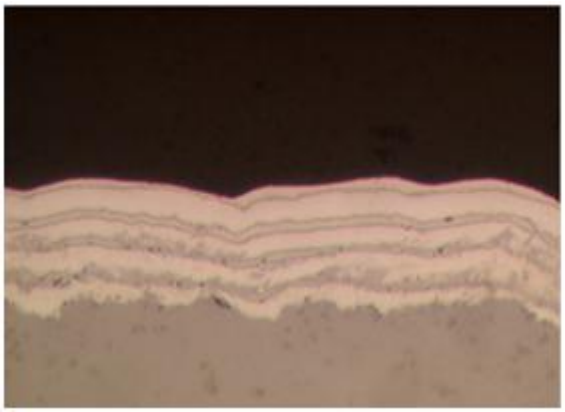

Figure 20Single layer plating

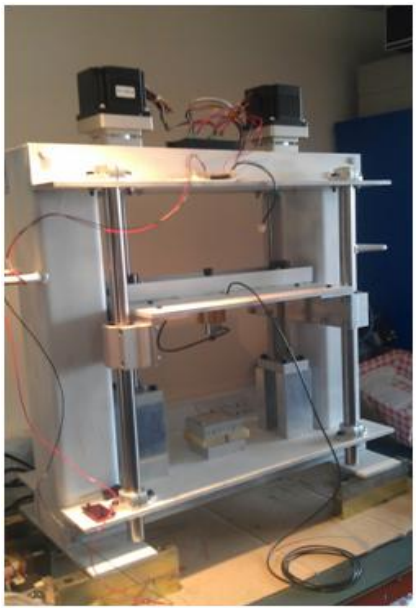

Figure 21 Pick/place machine

Figure 22 Fluidised bed

Figure 23 Photo's of Ormerod 3d printer and Eosint equipment

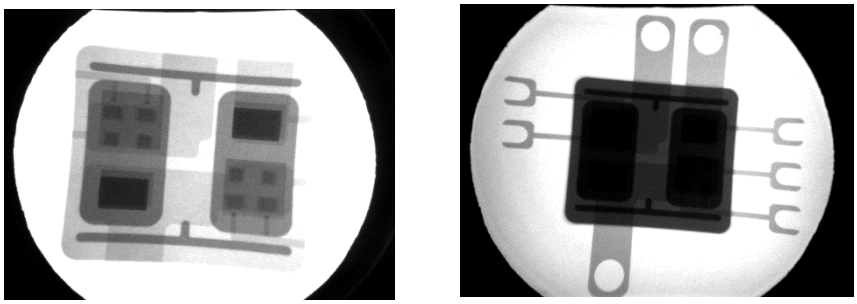

Figure 24 Xray images of the SAM

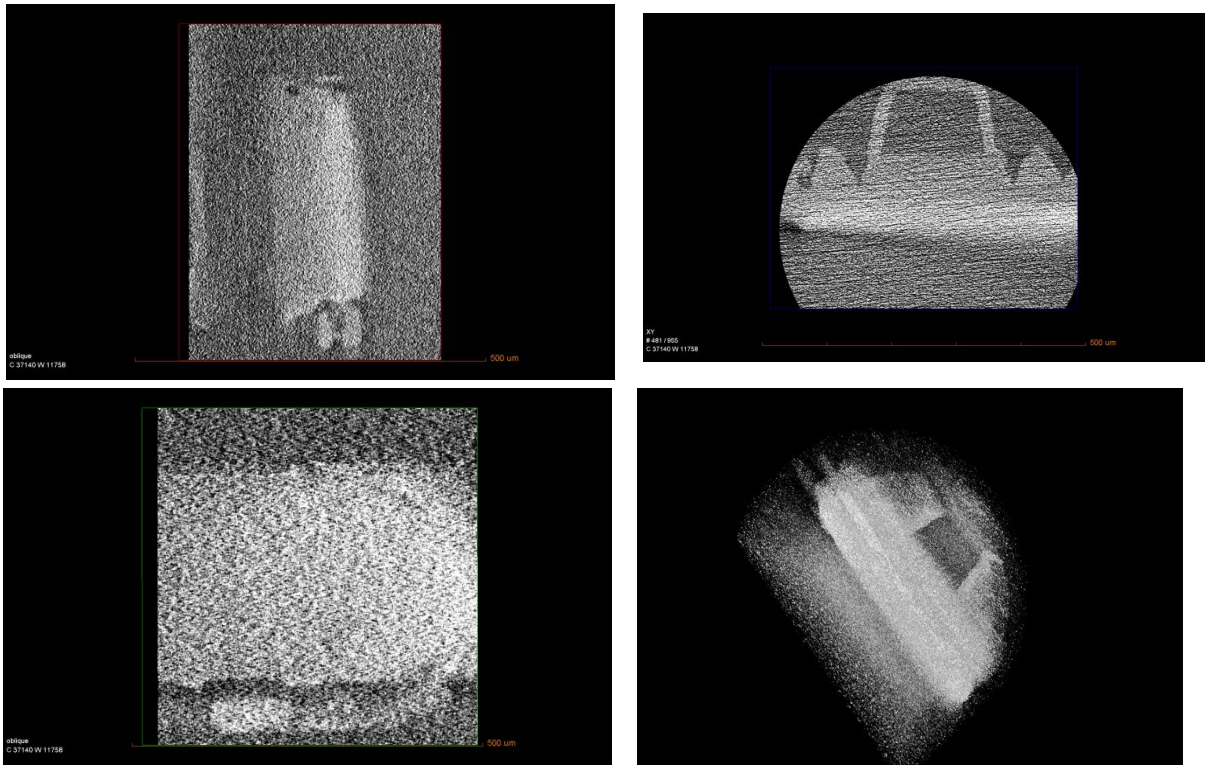

Figure 25Tomography of sinter connection

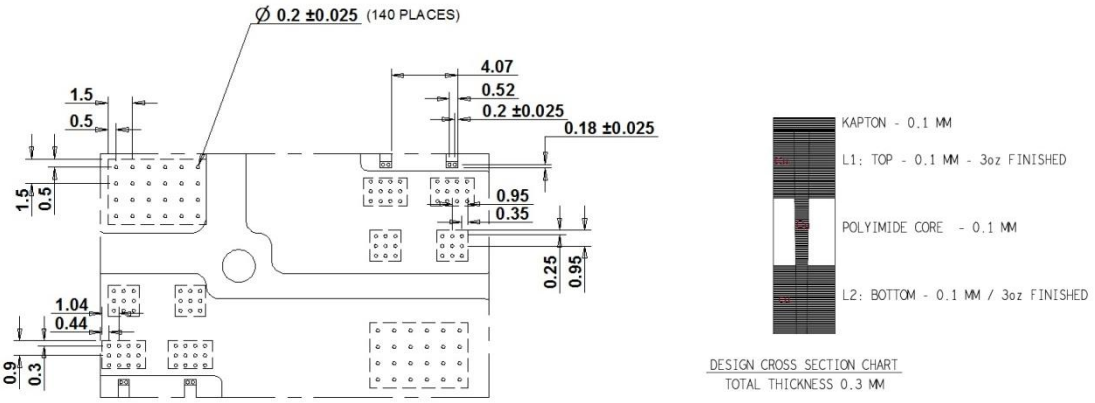

Figure 26 Cu-filled via size and distribution & Cross section of PCB

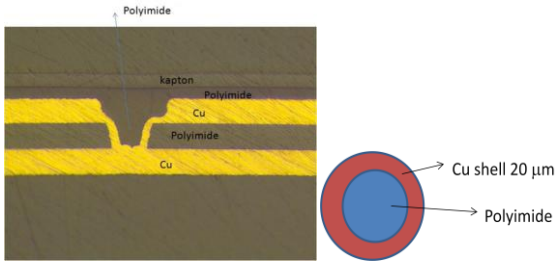

Figure 27 PCB Core Cross Section

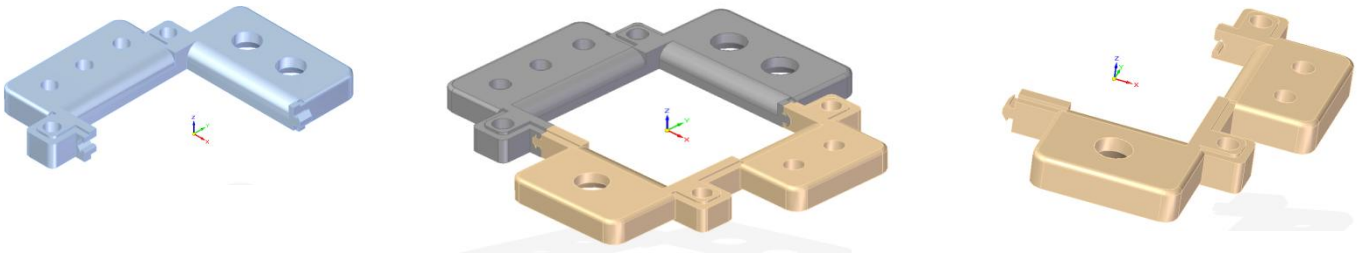

Figure 28 Frame design

Figure 29 New gel / old gel

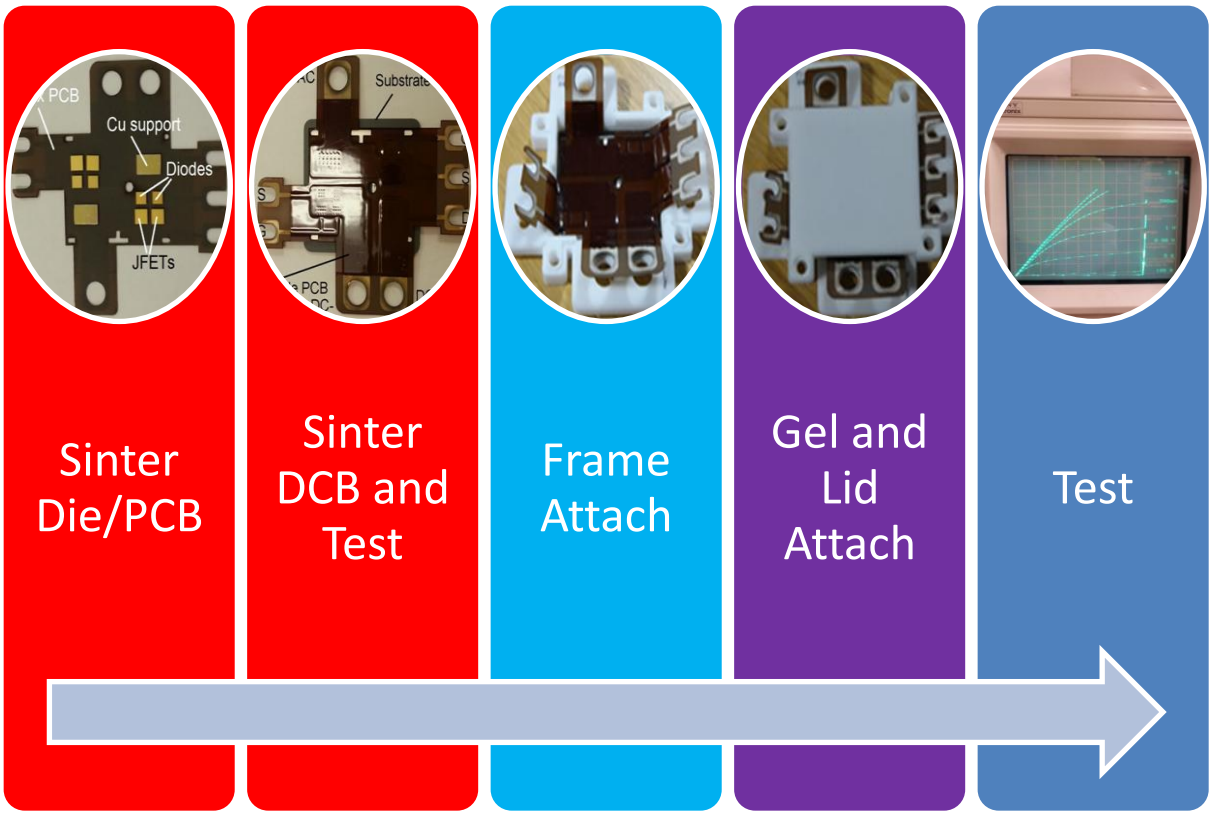

Figure 30 Final process route