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Efficient and Precise 3D Integration of Heterogeneous Microsystems from Fabrication to Assembly

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PROJECT FINAL REPORT

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Final publishable summary report

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1. Executive summary

Micro- and nano system integration is a rapidly developing field where multiple materials, technologies, and functional components form highly integrated micro- and nanosystems for cross-sectorial applications such as medical implantable devices, intelligent sensors, flash memory, computer memory, camera chips, and radio frequency devices in mobile phones. Recently, 3D integration by stacking components vertically became a very promising approach. In many integration tasks, simultaneously high-throughput and high-precision are very important, and it can often became the bottleneck that limits the potential of an otherwise very promising technology.

FAB2ASM uses a novel hybrid microassembly technology to attack the problem of simultaneous high-throughput and high-precision. Hybrid microassembly is a novel technology that joins traditional robotic pick-and-place and self-assembly of microsystems. Using existing high-speed robotic tools, a throughput of tens of thousands unit per hour can be achieved for the fast but coarse feeding of dies to the targets of assembly. Using capillary self-alignment – where surface tension of the liquid aligns small components such as microchips, we can achieve micron accuracy positioning simultaneously with the high speed feeding. Combined with appropriately designed interfaces, permanent fixing and electric connections can be successfully implemented.

In the FAB2ASM project, we developed technologies that covers the whole process chain of hybrid microassembly for microsystem integration, from interface design, capillary self-alignment, bonding techniques, and integration of industrial robots and hybrid microassembly technology. Many novel technologies have been developed, varying from laser ablated micro trenches for self-alignment, assembly of ultra-thin (5µm and 10µm) dies, water mist induced parallel hybrid microassembly, high-throughput handling of small dies (100µm and 200µm) at tens of thousands unit per hour, laser TSV drilling and filling, nanostructured multi-layer bonding materials, etc. High accuracy (submicron) assembly results has been demonstrated using hybrid microassembly. The project completed with three final demonstrators, including a high-speed hybrid microassembly demonstrator that can achieve over 40,000 unit per hour for small die assembly, integration of surface emitting lasers, and 3D integration of thin dies on wafers.

The results of the FAB2ASM provides the European semiconductor industry a new tool in integration technologies such as chip-to-chip, chip-to-wafer, interposer and fan-out for BGA. It reinforces the competitiveness of European nano- and µ-manufacturing with a technology that pushes beyond the efficiency-precision chart of the state-of-the-art integration technology. Moreover, the technology developed by FAB2ASM can be adapted into flip-chip/die bonding equipment and upgrade the existing factory to a new level of performance and cost effectiveness. In contrast to many other technology, the FAB2ASM technologies can preserve the current investment of industry and reuse a great amount of technology know-hows that is the advantages of European industry.

The project is led by Aalto University, together with three industry partners: NXP semiconductors, Beam-Express, 3D PLUS, other two academic partners: University of French Comte, University of Twente, two research centers: IMEC, EMPA, and ALMA consulting.

More information of the project can be found at the project website (URL: www.fab2asm.eu).

2. Summary description of project context and objectives

High-precision low-cost integration of micro- and nano system from components made in different technologies is of great importance for the success of many applications in this post Moore era. A high-efficient and high-precision integration technology is also crucial to the success of 3D integration and heterogeneous technologies. Particularly, die-level techniques, such as die-to-substrate and die-to-die methods are of great interests. Die level techniques have several advantages:

- Increased yield, due to using known-good-dies;
- Flexibility in the assembly process, less design effort for a new system;
- Efficient use of wafer or substrate area in the case of 3D integration.

However, so far the cost of high-volume production has been very high because of the low throughput of pick-and-place assembly, especially when high precision is required (e.g. alignment of optical devices), preventing those highly important technologies to be implemented widely.

An alternative technology is self-assembly, which can simultaneously assemble a great amount of dies on a substrate. However, self-assembly often uses a dramatically different process from the existing integration technologies due to their specific process requirements. Moreover, self-assembly technologies are often stochastic in nature, which cannot guarantee the yield and control precisely many process parameters (e.g. utilizing the known good dies), and also lack the flexibility required in many applications.

The FAB2ASM project develops a new manufacturing technology for 3D integration and heterogeneous integration of microelectronics and microsystems that allow a simultaneously very fast and very accurate process.

FAB2ASM uses a hybrid microassembly technology that merges both robotic technology and self-assembly, resulting a more natural solution to satisfy this requirement of simultaneously high-efficiency and high-precision for die-level integration. Particularly, it uses a very promising technology of self-alignment assisted robotic microassembly. In this technology, self-alignment using e.g. capillary force is responsible of achieving high-precision final alignment at high speed, and the robotic mechatronics is free to carry out high speed mechanical operations such as feeding and coarse positioning of the micro parts without much attention to the precision of the positioning or the effects of the adhesion forces at microscale. The novel hybrid microassembly technology also allows reusing of current industry machines such as die bonders and flip-chip machines and improving their performance with minor modification.

FAB2ASM project addresses the full process chain of integration of 3D and heterogeneous microsystems. It covers the components and interface design, ultra-fast robotic coarse positioning technology, high-precision self-alignment technology, and fixing and bonding technology. It allows both the ultra-fast mass manufacturing of heterogeneous microsystems and more demanding tasks of the stacking of multiple dies. The main process steps of the hybrid microassembly technology in FAB2ASM are shown in Fig 1.

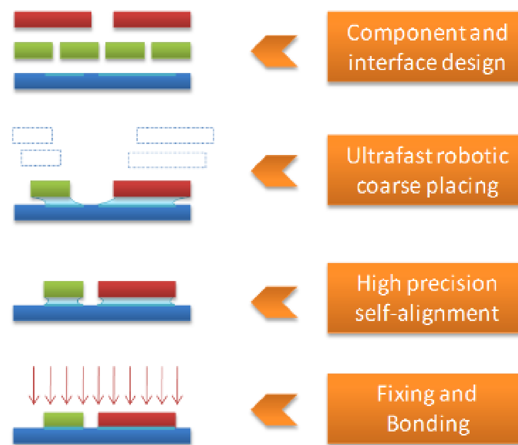


Fig. 1: Main process steps of hybrid microassembly

More specifically, the objective of FAB2ASM is to develop a highly industry relevant technology that not only reuses most of the industrial process steps, but on the other hand dramatically improves the performance of the integration process in terms of precision and efficiency: FAB2ASM will allow handling of small (100 μm) and/or thin dies (20 μm) and ultra-high speed assembly (40,000 unit per hour), while ensuring industry proven reliability. Three industry-led demonstrators are planned to validate the achievements in the fields of manufacturing equipment, photonic IC and microelectronics.

FAB2ASM project joins forces of major research institutes and industry partners in Europe to develop the technology of the hybrid microassembly process. The consortium and their geographical distribution can be found in Figure 2.

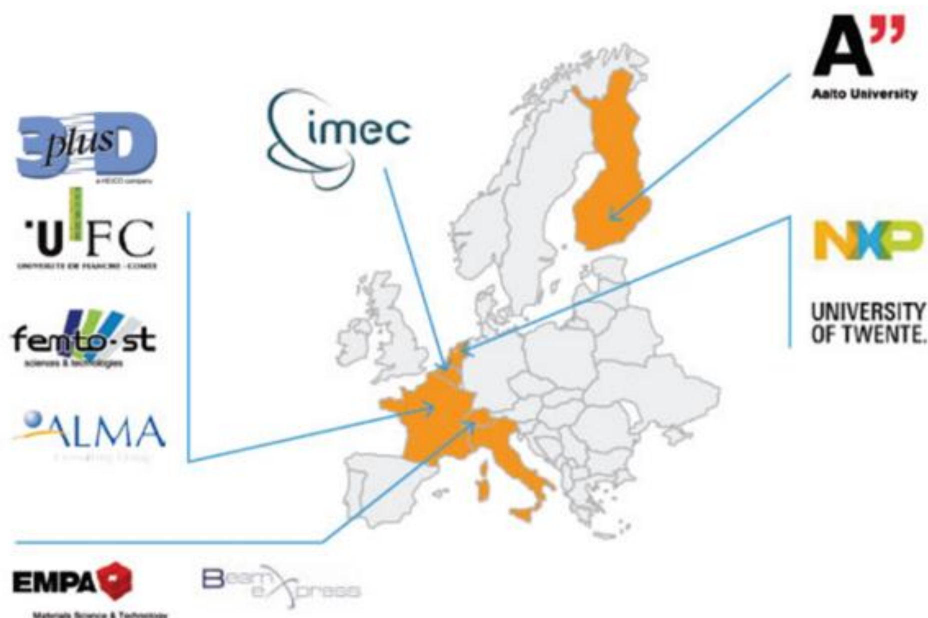


Fig. 2: FAB2ASM consortium and their geographical distribution

3. Description of the main S&T results and foreground

The hybrid microassembly technology developed in FAB2ASM focuses on droplet self-alignment assisted technologies [1]; other possibility such as dielectrophoresis has also been investigated. Droplet assisted hybrid microassembly uses droplet self-alignment to assist robotic microassembly. The process is illustrated in Figure 3, which consists of elements such as substrate, patterns on the substrate, liquid droplets, microchips, and robotic feeding mechanism. A substrate with patterns that can confine the droplets is the basis of the integration process. Appropriate droplet delivery methods, such as droplet dispensing introduces a certain amount of liquid, e.g. water or adhesive, on to the pattern. Then the microchips or other micro components are fed onto the patterns by robotic mechanism. Due to the strong capillary force at milli- and microscale, the chips will self-align to the pattern at a high precision quickly, in tens to hundreds milliseconds for low viscosity liquids. After the self-alignment, the successive steps are carried out to permanently fix the chip with the substrate. Different bonding techniques can be applied depending on the interfacing materials and the liquid between the chip and the pattern of the substrate.

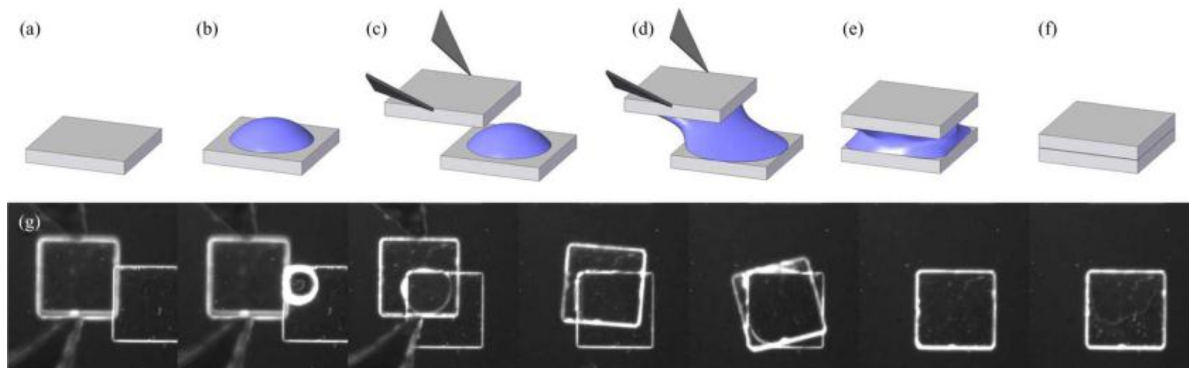


Figure 3. Hybrid microassembly with droplet self-alignment [1]. (a) Assembly site is protruded structure. (b) Droplet of water is dispensed on the assembly site. (c) Microgripper approaches the release site with a part. (d) Droplet contacts with the top part and wets between the part and the assembly site, which forms a meniscus. (e) Microgripper releases the part and the capillary force aligns the parts. (f) Parts are aligned and bonded. (g) Image sequence of the actual experiment, as viewed from the top side.

In the following sections, key process steps of the FAB2ASM hybrid microassembly technology will be introduced, including the component and interface design, hybrid microassembly, and fixing and bonding, followed by the integration of the process steps and technical demonstrations.

3.1. Components and surface design for self-alignment

To integrate of self-alignment into a packaging flow, laser chip (VCSEL) and Si chips were developed and fabricated using industry relevant platform through joint work of IMEC and Beam Express. The Si chips realized in both 130nm and 65nm CMOS node were fabricated on 200 and 300mm wafers. The Si chips comprised Through Silicon Vias (TSVs), and microbumps at 20μm pitch. In parallel, miniaturized VCSEL and Si bench with integrated photonics wave guide were also developed.

The developed miniature VCSELs (see figure 4) have reach industry maturity level and prototypes of Si chips with TSV have been developed.

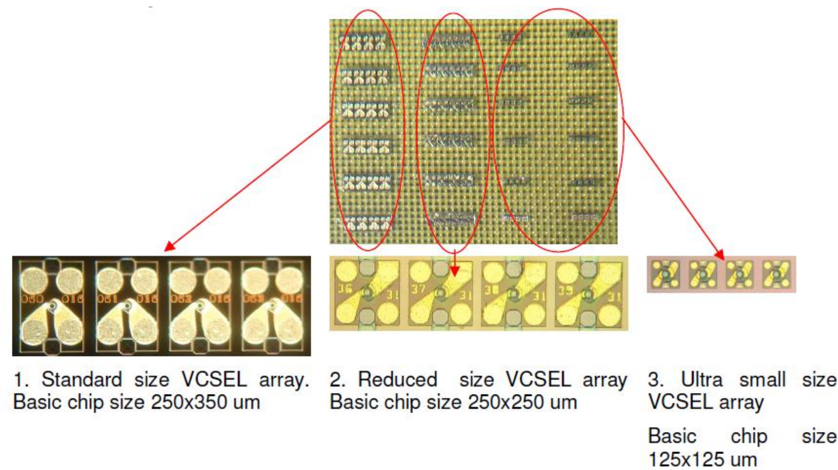


Figure 4. Fabricated 1490 nm VCSELs with different footprints from Beam Express.

To achieve hybrid microassembly, the components need to be designed according to the requirement of the self-alignment process. Interfaces based on chemical functionalized hydrophilic/hydrophobic patterns have been developed to ensure the compatible with the requirements of microfabrication. This approach has been actively pursued by IMEC and Aalto University and the results are rather effective.

Besides chemical functionalization, FAB2ASM has investigated the interfaces based on pure geometrical features, including the novel laser ablated micro trenches for self-alignment (see Figure 4) [2] through joint efforts of University of Twente and Aalto University.

To understand the requirements of manufacturing precision for self-align patterns, low precision patterns with jagged edges have also been investigated by Aalto University. The results show that the self-alignment process is rather robust despite the significant jaggedness of the edges (see Figure 5) and the final accuracy can be much better than the amplitude of the jaggedness of the pattern [3]. This results has important implications in reducing the manufacturing requirements and associated costs for industry implementation of hybrid microassembly technology. Electrical functionality of the interface has been considered during the design process.

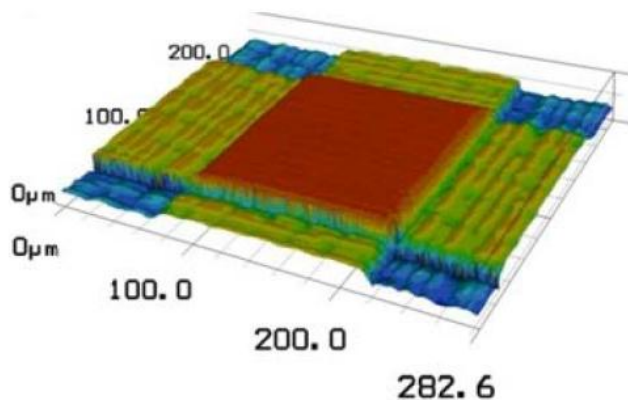


Figure 4. Pico-second laser machined polymer receptor site [2].

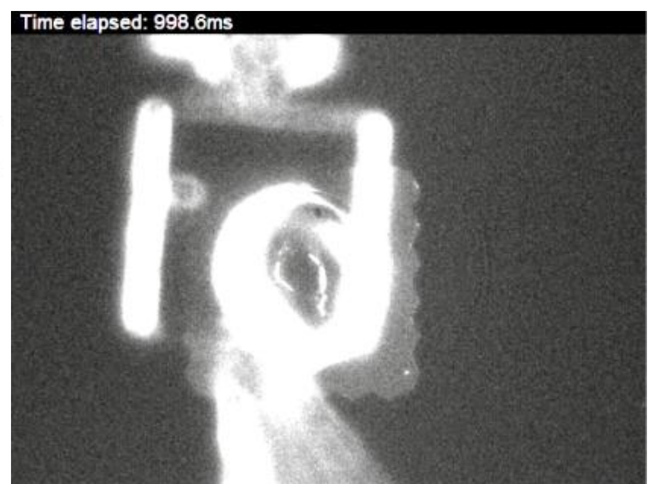


Figure 5: Hybird microassembly of 200 x 200 µm chip on hydrophilic/phobic pattern with jagged eges [3].

3.2. **Hybrid microassembly**

Hybrid microassembly processes based on capillary self-alignment (see Figure 3) has been carefully investigated in FAB2ASM. The process has been applied in the three demonstrators of the project, as discussed in Section 5. High speed robots have been developed, which can pick-and-place small dies at high speed: >20K UPH for 100µm dies and >40K UPH for 200µm dies. Moreover, novel hybrid microassembly process, including extensively stacking of ultra-thin dies (see Figure 6, [4]), dielectrophoresis self-alignment [5] (see Figure 7) and water mist induced parallel hybrid microassembly has been developed (see Figure 8, [6]).

Reducing the thickness of dies is one way to reduce the price of stacked dies. Indeed, thinner the dies are, cheaper the TSVs are. Self-assembly combining with specific die design and handling tools developed in FAB2ASM has enabled to perform the handling of 10µm and 5µm-thick dies. Based on our knowledge, the current state of the art on ultra-thin dies are 40µm-thick. FAB2ASM has shown a significant advance by demonstrating the ability to stack twelve 10µm-thick dies (figure 6, [4]) through the successful cooperation between University of French Comte and Aalto University.

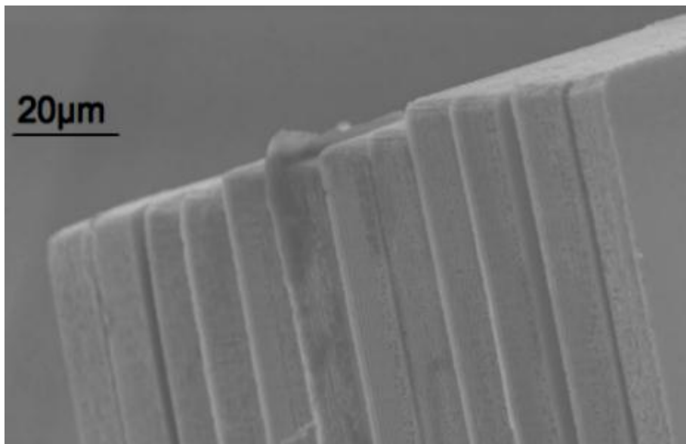


Figure 6. Hybrid microassembly of 12 layers of 1 mm x 1mm die with thickness of 10 µm [4].

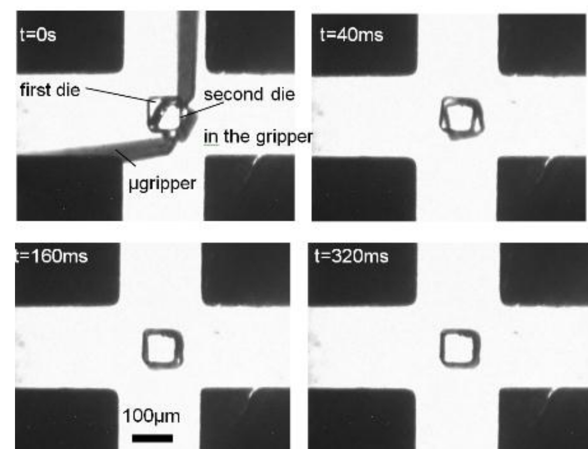
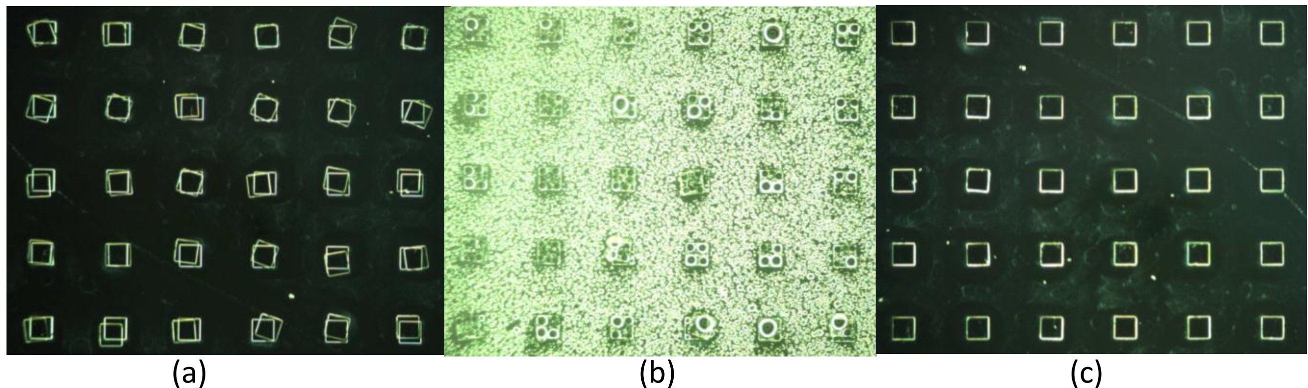


Figure 7: Self-assembly of a two 100µm glass dies using dielectrophoresis

FAB2ASM has also obtained promising results in an original way to perform die self-assembly using electric force field, based on the physical principle “dielectrophoresis”, which is particularly relevant for ultra-small components. It could be used for dies whose surface is below 200µm x 200µm and could be extended to nanotechnology. As a result, University of French Comte has shown that it is possible to microassembly two ultra-small dies using dielectrophoresis (see Figure 7). These results clearly show that dielectrophoresis can be used to achieve self-assembly especially for small dies (up to 100µm). Based on our knowledge it shows the first-time self-assembly of artificial components done using dielectrophoresis.

FAB2ASM has also developed a hybrid microassembly technique for massively parallel assembly of microchips. Aalto University has developed method combining robotic pick-and-place technique and water mist induced parallel self-assembly. A Robotic handling tool is used to place microchips roughly on chips of the same size at a fast speed, and then water mist composed of microscopic droplets is delivered to achieve high accuracy and massively parallel alignment (Figure 8). The results indicate that the technique is promising for assembly of a large quantities of microchips

simultaneously, it has been demonstrated with a matrix of 30 200μm × 200μm SU-8 chips. The alignment can reach sub-micrometer accuracy.



(a) (b) (c)

Figure 8. Parallel hybrid microassembly of 30 microchips with water mist: a) 200μm x 200μm x 30μm chips are placed on the top of a matrix of 30 receptors of the same size with random placement error; b) water droplets are delivered in the form of the water mist; c) the placement errors are corrected and all the chips are aligned with the receptors [6].

3.3. **Fixing and bonding**

Fixing and bonding technologies for hybrid microassembly process have been investigated including metallic bonding, TSV filling and nanostructured bonding materials. Cu/Sn micro-bumped dies with 20 μm pitches have been designed by IMEC, which leads to metallic interconnections with submicron precision after the hybrid microassembly process (see Figure 9, [7]). Laser drilling of TSVs and Laser Induced Forward Transferring (LIFT) for TSV filling has been developed as alternative technology for the TSV manufacturing by University of Twente [8]. Novel multi-layer nanostructured materials for bonding have also been developed by EMPA.

Methods and strategies for laser drilling of TSVs were developed. In 200um thick Si wafers, holes as small as 17um (exit diameter) and 9um (exit diameter) were achieved, implying a diameter-to-wafer-thickness ratio up to (about) 1:20, see Figure 10.

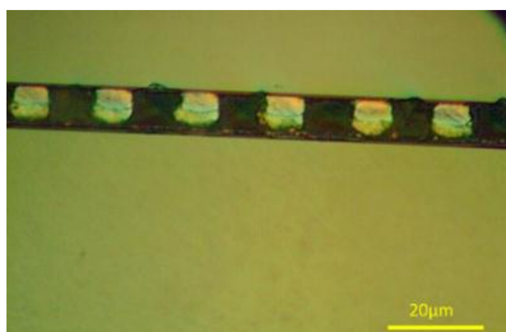
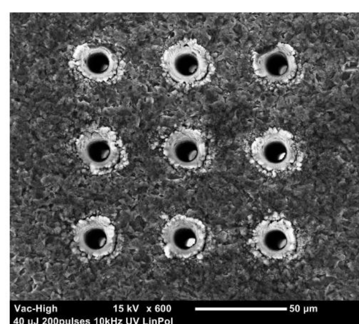
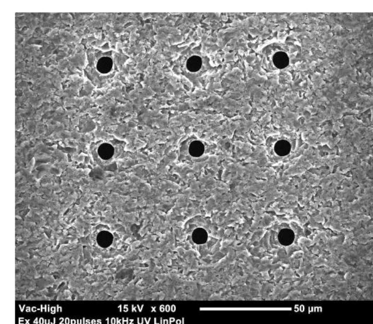


Figure 9. Optical photograph showing, 7.5μm diameter, 20μm Cu/Sn bumps, assembled using capillary self alignment [7].

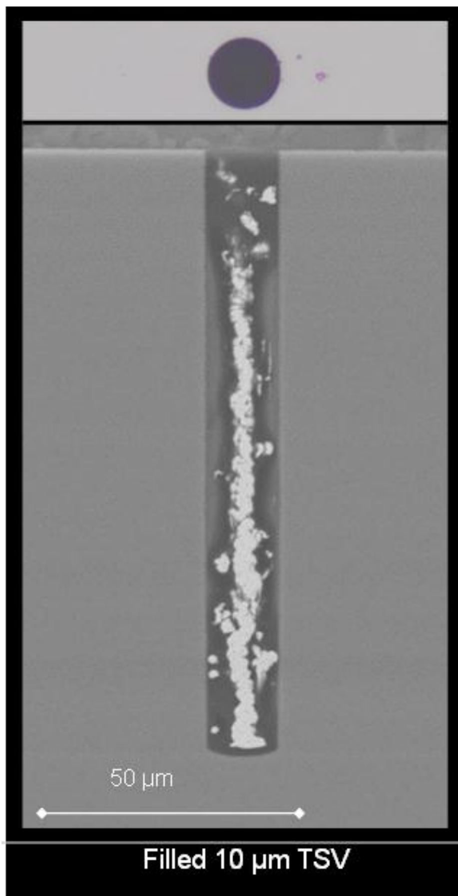


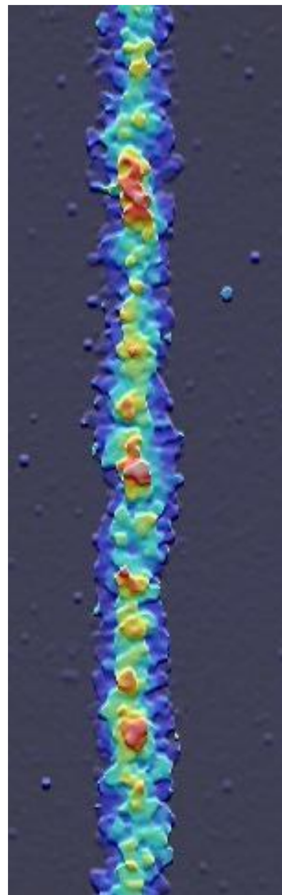
(a) Entrance side of the holes drilled with 200 ultraviolet pulses. The amount of surface debris is minimal, but still small inlet rims are visible.

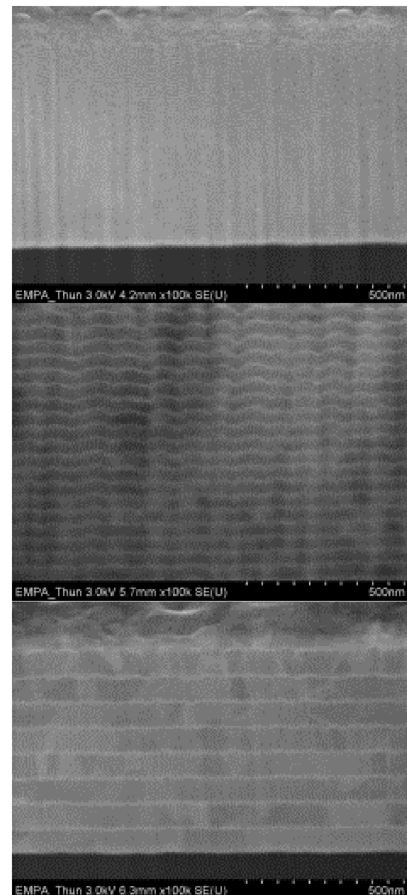


(b) Exit side of the sample, showing regular exit diameters of $9\mu m$.

Figure 10. SEM images of the entrance and exit sides of holes drilled using 343nm (ultraviolet) laser light with 40uJ pulse energy and repetition frequency of 10kHz.







(a) **(b)**

Figure 11. (a) Top view and cross-section of a 10 µm diameter TSV filled with 800 copper droplets using the LIFT process ; (b) Conduction line printed with the LIFT process.

Figure 12. Multilayer nano solders. Top: 5nm Cu / 2nm W; Middle: 50 nm Cu / 2 nm W; Bottom: 100 nm Cu / 2 nm W.

Compared to conventional filling methods, the LIFT process was identified as an innovative method to fill TSV's, see figure xx (a). By filling TSV's, with diameters as small as 10 µm in diameter and up to 110 µm deep, while exhibiting a minimum contamination on the surface, the feasibility of the LIFT process for TSV filling has been demonstrated. Optical microscopy of cross-sections of filled TSV's, revealed voids, but these were qualified as acceptable (see Figure 11a). In addition, further applications of LIFT, like printing of conductive lines (see Figure 11b), have been successfully demonstrated. Futher study would be required to improve these results.

FAB2ASM has also developed several multilayers nano solders. This approach is based on a nanoscale effect that allows for the drastic reduction of melting point for nm thick brazing filler metals (with respect to the bulk melting temperature). Different multilayer solders, including Ag/Cu, Cu-W, have been developed by EMPA.

3.4. **Integration and reliability**

The different techniques and technologies developed in FAB2ASM have been integrated with all process steps from fabrication to assembly validated and chained efficiently. Reliability of the processes and the produced products has been ensured by proper mechanical, electrical and optical characterizations.

3.4.1. Integration of hybrid microassembly station

A set-up for hybrid microassembly experiments has been constructed and integrated at Aalto University (Figure 13). It has served as a proof-of-concept test station for self-assembly and hybrid assembly throughout the project, and directly supported development of process integration for the demonstrators. The station is capable of handling dies of different form factors: there is a tweezer-type gripper for small dies (down to 50 x 50µm), an ultra-thin die handling tool developed by UFC for thin dies (down to 5µm thick), a vacuum gripper for large dies (> 1 x 1mm), and a novel adhesive gripper developed by Aalto University for medium and large dies (> 100 x 100µm). Two dispensers have been integrated in the station: a piezoelectric dispenser for water (minimum volume ~60 pl) and a pneumatic dispenser for other liquids, such as adhesives (minimum droplet diameter ~25 µm).

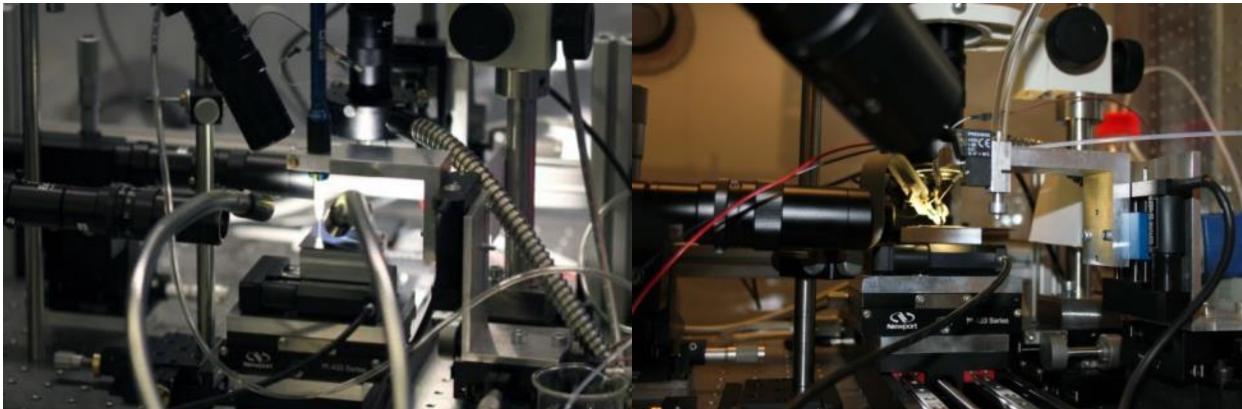


Figure 13. Hybrid assembly test station. Left: pneumatic dispenser installed in the front. Right: ultra-thin die handling tool integrated in the front.

3.4.2. Integration of VCSELs on photonics benches

Processes for integrating VCSELs on optical silicon benches using self-alignment techniques have been developed jointly by Beam Express, IMEC and Aalto University. The assembly processes are suitable for all VCSEL form factors developed by Beam Express, including the ultra-small size (125 × 125 µm). The VCSELs are picked and placed on the benches either as single chips, or in arrays of four. Only rough placement accuracy is initially needed as capillary forces of a water droplet dispensed on the assembly site self-align the parts. The alignment is further enhanced by the following solder reflow step. Figure 14 shows assembled VCSEL arrays on the silicon photonics bench.

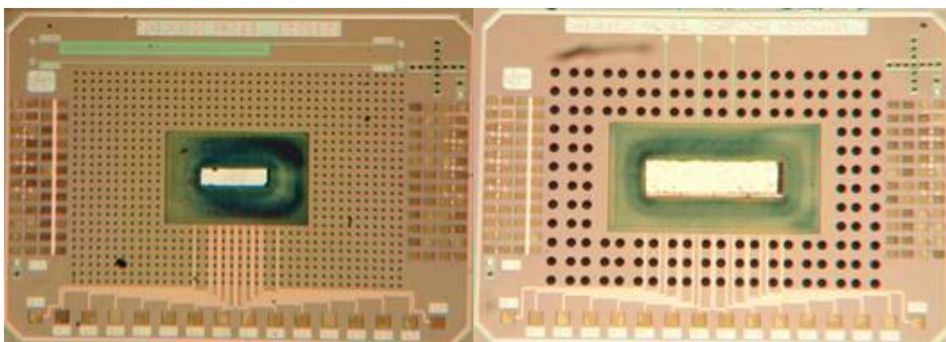


Figure 14. Left: ultra-small (125 × 125µm), and right: reduced size (250 × 250µm) VCSEL arrays assembled on photonics bench using water droplet self-alignment.

3.4.3. Small-pitch 3D chip stacks

IMEC has demonstrated the assembly of through-silicon-via (TSV) chip stacks using water droplet self-alignment. 50µm thin chips with small-pitch (down to 20µm) microbumps and TSVs have been fabricated, and stacked using water droplet self-alignment. On the bottom chips of the stacks, areas were functionalized to provide wetting contrast for water self-alignment. In the resulting assemblies, TSVs are fully connecting the planar metal on top of the chip to the microbumps of the bottom chip (Fig. 15).

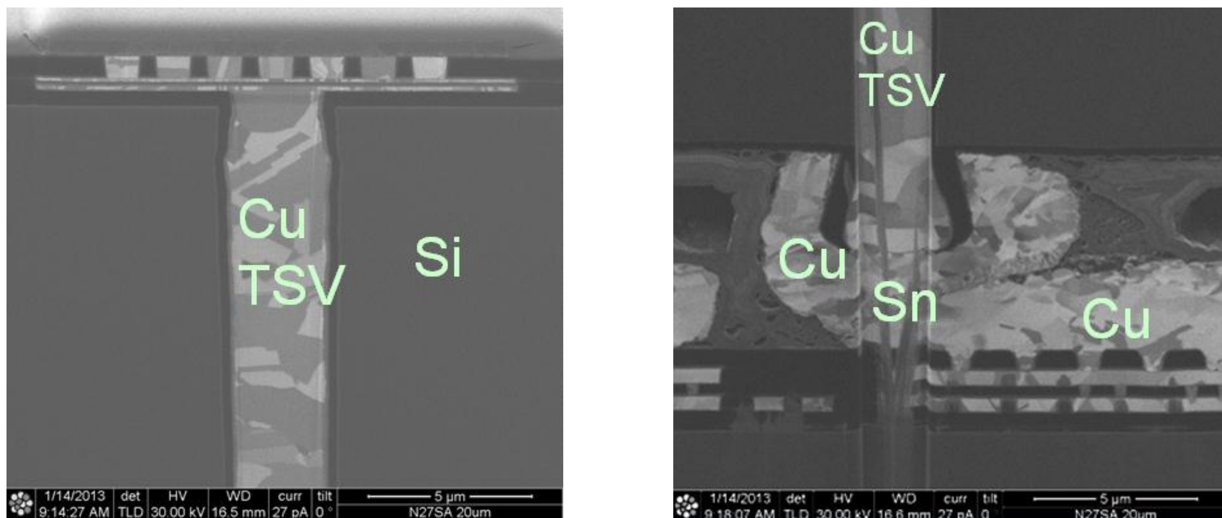


Figure 15. Focused ion beam cross-sectional SEM images of TSV connecting to the metal wiring on the top of the chip (left) and TSV connecting to the microbump of the bottom chip (right).

3.4.4. Reliability and assembly performance

3DPLUS, IMEC, NXP and Beam Express have carried out electrical and optical testing of assemblies produced in the project, including 3D chip stacks integrated at IMEC, high-precision VCSEL packs assembled at NXP and VCSELs on optical silicon benches integrated at Beam Express and Aalto University. Optical testing of the VCSELs has been carried out by Beam Express. Example electrical and optical performance data of ultra-small VCSEL assemblies are shown in Figure 16). The electrical and optical tests have verified reliable functioning of the different assemblies.

Evaluation of the assembly of small low pin count parts using technologies developed in the project has been carried out by Aalto University and NXP. The parts include standard NXP products assembled in Demonstrator 1, and high-precision VCSEL packs (HPV) assembled in Demonstrator 2. The assembly process performance was evaluated in terms of accuracy, mechanical stability, speed and yield. The performance tests showed that no bottlenecks were present in the assembly processes, and the targeted quality of final assemblies was reached.

Mechanical testing of bonding has been carried out by EMPA and UFC. At EMPA, several mechanical strength test methods and set-ups for bonded microparts has been developed, including a wedge opening test to determine interface toughness, a shear test to determine the shear strength of interfaces, and an in-situ (inside SEM) micro-compression test for high temperatures (see Figure 17). UFC has developed two versatile bonding force measurement platforms capable of measuring forces in the nN and mN ranges between objects from nanospheres to micro-components. They have been used to measure e.g. bonding forces of dies assembled by self-alignment. Two

configurations were developed during the project. In the first configuration, force measurements are performed by pulling, and in the second configuration by pushing (Figure 19).

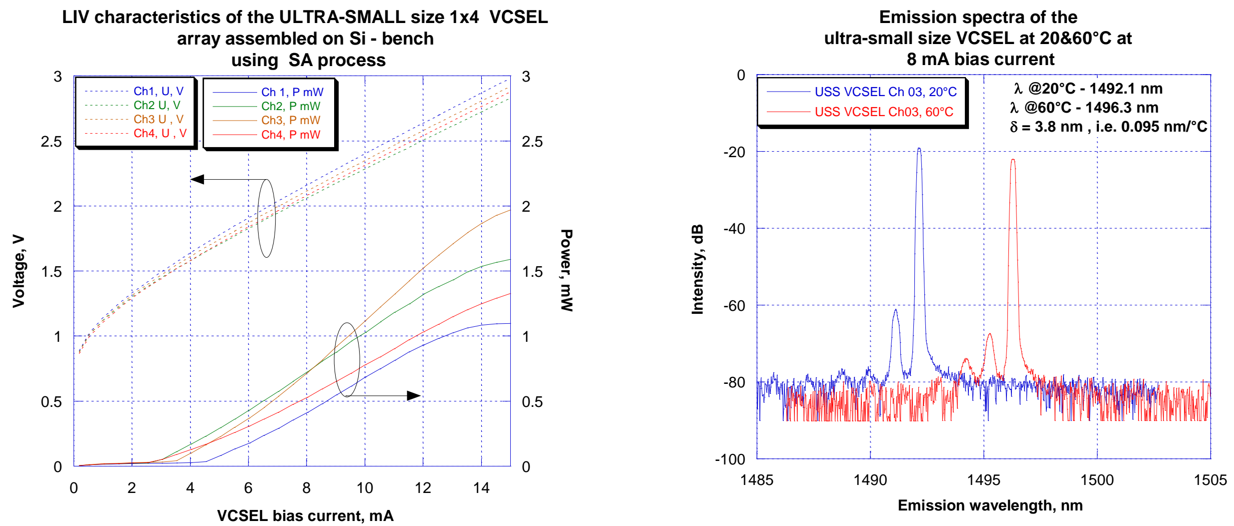


Figure16. Electrical LIV characteristics (left) and optical emission spectra (right) of ultra-small VCSEL arrays assembled on silicon bench.

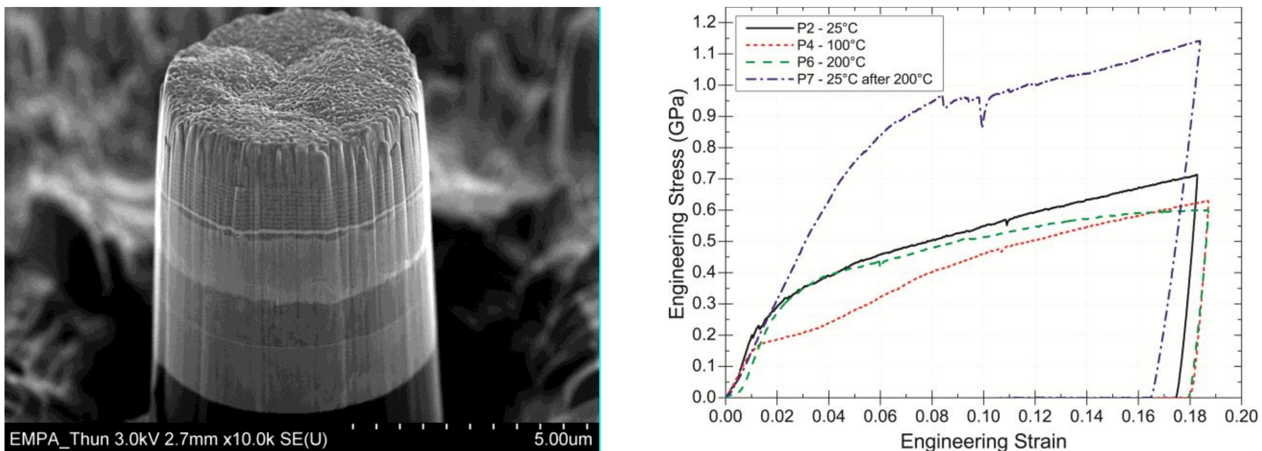


Figure 17. A Cu/Sn multi-layered micro-pillar with tungsten diffusion barriers was compressed at temperatures up to 200°C. At room temperature, the Cu and Sn plastically deform together, but at 100°C the strength of the Sn is significantly decreased, resulting in extrusion of the Sn layer from the multilayer stack. At 200°C, the Cu/Sn reacted to form the Cu_6Sn_5 intermetallic phase, and the reaction was observed to proceed past the tungsten diffusion layers upon the application of sufficient plastic stress to break the diffusion barrier. After cooling the reacted pillars to room temperature, the Cu_6Sn_5 intermetallic was observed to show a 100% increase in strength over the initial pillars

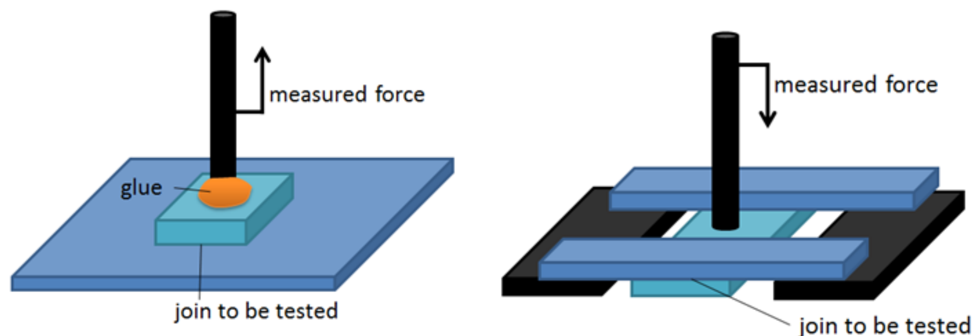


Figure 18. Two bonding force measurement configurations. Left: pulling test. Right: pushing test.

3.5. Demonstrators

Three demonstrators have been developed in FAB2ASM, in die integration on lead-frame, integration of VCSELs on benches, and on 3D integration of dies on substrate.

3.5.1. Hybrid microassembly on lead frame

With the further reduction of die size due to the ever evolving demand of reduced foot print and costs, it is a great challenge to achieve high-precision integration of dies on lead frame with the same or even better throughput. To ensure the functionality and reliability of the integrated device and to reduce the package size, the required die placement precision should be much better than the cases with larger dies, despite the even higher throughput. Technologies relying on pure robotic microassembly are reaching their limits in satisfying such demand.

In FAB2ASM, NXP has integrated capillary self-alignment assisted hybrid microassembly technology in NXP's industry leading high-speed die bonding machine, which can reach a throughput of over 40K unit per hour (UPH).

The initial tests have been carried out on MCD-type of lead frame with cavities around the dies. Low viscosity adhesive has been used at a dispense speed > 40K UPH, and the machine was running >40K UPH during the tests. The initial run of the hybrid process achieved a yield of over 95%, subsequent tests results ~ 97% of dies are well self-aligned. The results are shown in Figure 19. The assembled dies has a position accuracy of about 2μm on the substrate, which is as good as the position accuracy of the patterns where the dies are assembled on. Higher accuracy can be reached with better defined patterns.

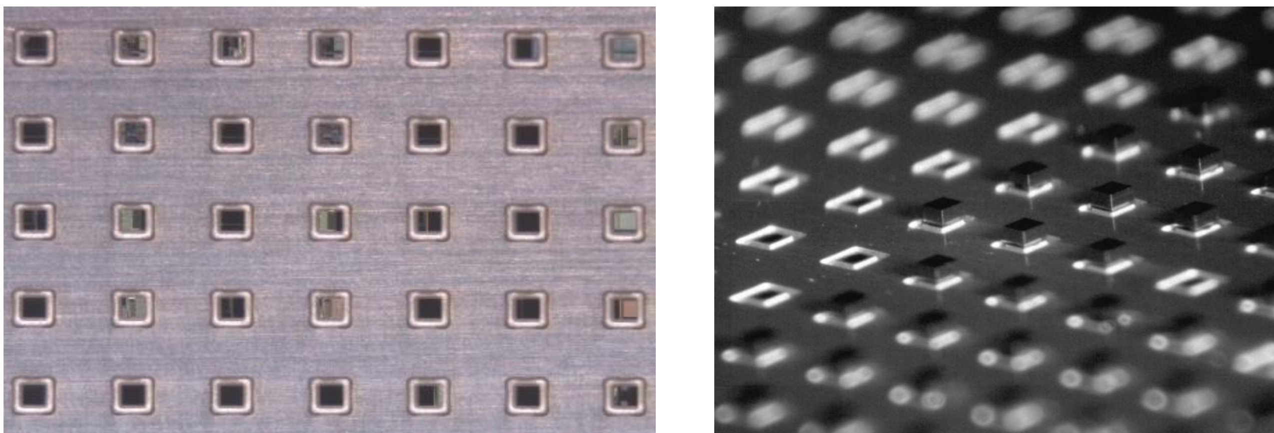
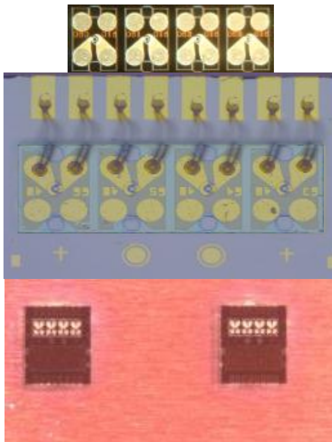


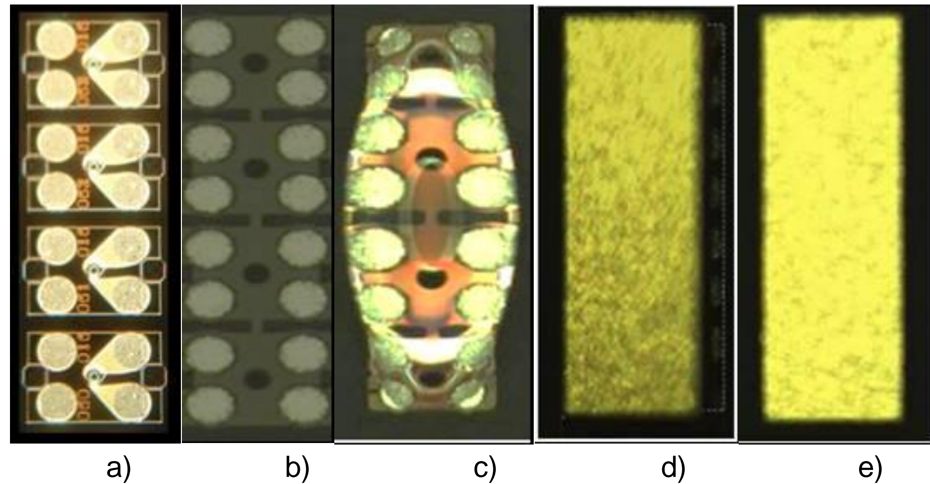
Figure 19. Results of hybrid microassembly of dies on lead frame with NXP high-speed die bonding machine.

3.5.2. Hybrid Microassembly of VCSELs

Silicon photonics platforms together with appropriate light sources are the key elements for ensuring the functionality of the final products in optical data communication, optical sensing, optical computing etc. Low electrical power consumption, circular optical beam profile and emission wavelength compatible with the transmission spectra of the silicon, make the long wavelength (>1200 nm) Vertical Cavity Surface Emitting Laser (VCSEL) an ideal candidate for laser light source for integration on silicon photonics platforms. One of the leading manufacturers of the long wavelength VCSELs is Beam Express SA, which uses a proprietary wafer- fusion technology for

fabrication of such devices. Within the FAB2ASM project we have been fabricated 1490 nm range emitting VCSELs with different footprints: 250 x 350 um, 250 x 250 um and 125 x 125 um, as depicted in Figure 4. The devices have been integrated with high precision accuracy onto two types of assemblies: VCSEL on a specific design carrier (Figure 20) and VCSEL on silicon bench (Figure 21 and 22). The technical functionality and reliability are strongly related to the placement precision (better than 2 µm) and the employed assembling techniques of the components while the cost relates partially to the assembling throughput. FAB2ASM addresses exactly these items, where Beam Express demonstrated the hybrid integration of Long Wavelength VCSEL.

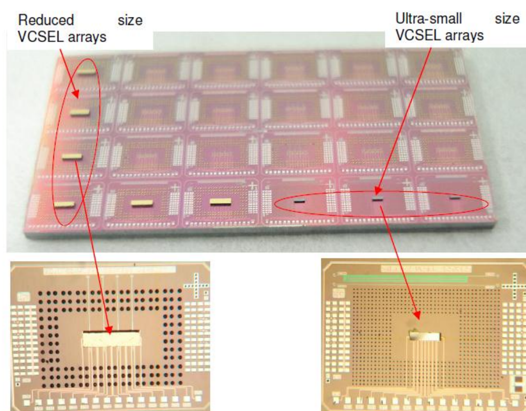




a) b) c) d) e)

Figure 20. 1490 nm VCSEL arrays assembled on specific design carrier. Position accuracy of VCSEL arrays on carrier: σx / σy = 1.6 / 3.1 µm.

Figure 21. Hybrid microassembly of a 1x4 VCSEL (1000x350µm) array on the silicon bench using self-alignment technique. a) 1x4 VCSEL (1000x350µm) array; b) pattern for 1x 4 VCSEL array on Si –bench; c) dispensed liquid droplet; d) Pre-aligned VCSEL array: one can see that the VCSEL array (bottom view of the array) is not precisely aligned yet; e) final self-alignment of VCSEL array with respect to Si- bench pattern.



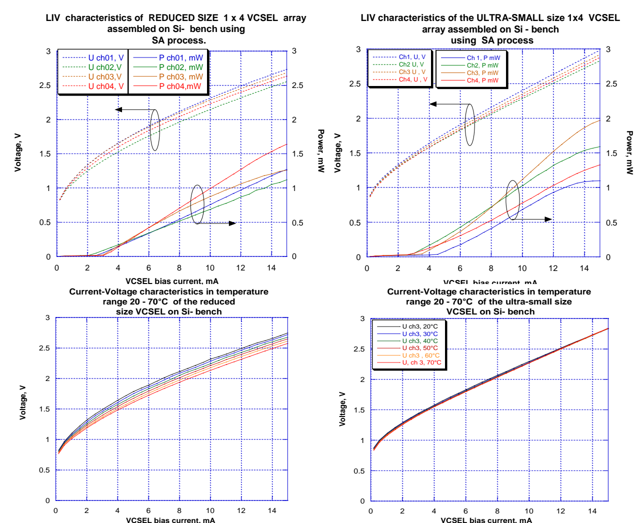


Figure 22. The picture of the Si- bench with reduced and ultra-small size VCSEL arrays assembled using liquid assisted self-alignment (SA) process. Simultaneous SA process of multiple arrays was demonstrated.

Figure 23. Opto-electrical characteristics of the 1490 nm VCSEL arrays assembled on Si- bench using liquid-assisted self-alignment technique.

After assembling of VCSEL arrays on Si-platform the electro-optical characteristics were measured. The results show that the self-alignment process allows the mounting of VCSEL on Si-platform with required accuracy and keeping the full functionality of the devices (Figure 23).

3.5.3. Hybrid microassembly for 3D integration

Heterogeneous integration is a key enabler for 2.5D and 3D integrated device. It allows to fabricate very advanced solutions with components (IC, memory, sensor, MEMS) coming from different sources. Similarly to the hybrid microassembly of VCSELs, micro bumping is a key enabler to be able to stack components with very high I/O pin count. On top of that Through Silicon Vias (TSVs) enable true stacking of dies. Nowadays, this is the path that is followed for memory applications where the sourcing of the unit memory dices and the TSV processing is made during the IC fabrication.

In FAB2ASM, IMEC have used 50µm thin dies containing TSV (5µm diameter) from a 300mm wafer processed on a 65nm technology platform. The thin dies are bonded onto a bottom die coming from a 200mm wafer, processed on a 0.13µm platform (see figure 24). Temporary bonding technique has been used for thin die handling (see figure 25) and integration with the microbumps (see figure 26) using the hybrid microassembly technology based on capillary self-alignment. Three layers stacking has been demonstrated.

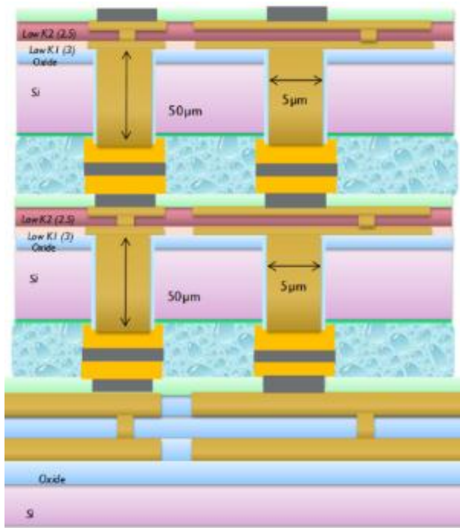


Figure 24. Schematic cross section of die stacking enabled by hybrid microassembly

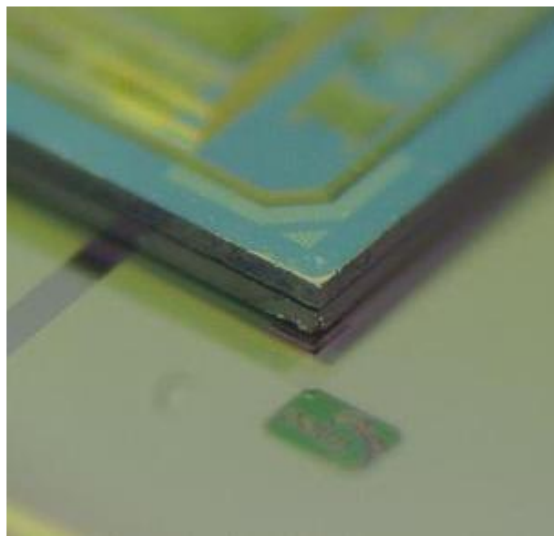


Figure 25. 50µm thin dies bonded on substrate forming a 3 layer stack.

Figure 26. XSEM view showing 3 layer stacks.

4. Potential impact and main dissemination activities and exploitation of results

4.1. Technological impact

Current IC technology is entering a diversification era, where on one hand scaling driven economics have a tendency to pack more transistors per area and where on the other hand a higher level of integration allows for more functions in the form of advanced heterogeneous microsystems. 3D integration, driven by the ever increase pin count of the components, will play a key role as technology enabler for such future products.

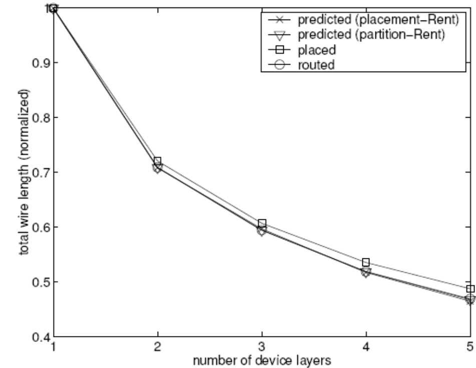


Figure 27. Total wire length vs. number of device layers.

In comparison to traditional 2D SoC, which may be beneficial for mass market, 3D integration applications open new opportunities for low cost solutions for large varieties of applications, from MEMS, Flash memory, DRAM, to RF systems and camera chips, due to its modularity and 3D configuration, shorter total wire length (Figure 27) and shorter time from design to market. Among the various integration technology, TSV based interconnection and related microbump technologies have been paving the way towards high density interconnect at Chip to Chip level. However, special hurdles for a wide spread market introduction of 3D integration is the non-availability of high speed high accuracy pick-and-place systems.

The technological impact of FAB2ASM is on the capability to satisfy the fast approaching demand in 3D integration on low cost, high speed and high accuracy integration by providing a technological path that goes beyond the state of the art approaches. 3D microsystems interconnected by TSVs and microbumps will become increasingly complex, and the requirements for integration accuracy will also increase quickly due to the smaller TSV and microbump size and pitch size, as shown in Figure 28.

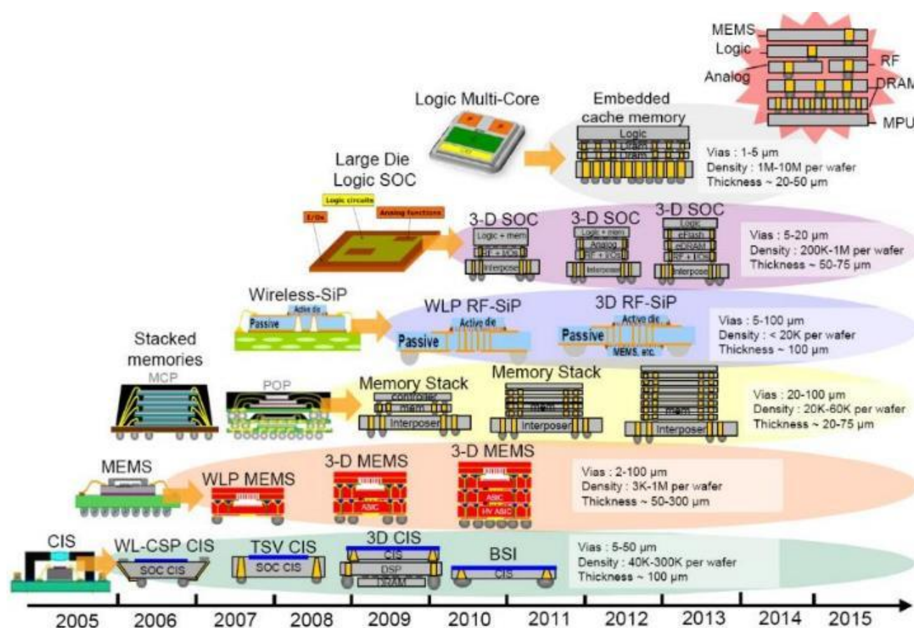


Figure 28. 3D TSV interconnection technology roadmap (source: Yole Development).

FAB2ASM provide a very promising answer to the technical demand in microsystem integration of faster and more accurate assembly of small and thin dies and open doors for the success implement of 3D microsystems.

The FAB2ASM technology satisfies the demands at a low cost by using high speed yet low precision robotic handling, combined with high accuracy self-alignment based on capillary forces. The FAB2ASM approach will dramatically increase the throughput at high accurate (micrometer) integration of microsystems, including the 3D systems based on TSV technology, and will become one of the **key enabling technologies** for next generation 3D microsystems. Furthermore, it will enable manufacturing of new types of products, by allowing the handling and integration of very small dies.

The project contributes significantly to the technical knowledge and capabilities of more efficient and lower cost assembly, and provides a new tools in microsystem and semiconductor integration, allowing a new generation of very small components at a very high precision with low cost**.** The applicability of FAB2ASM technology is illustrated in Figure 29.

Kind of 3D chip assembly	Good	Medium	Non applicable
Wafer to wafer			X
Chip to wafer	X	X	
Chip on chip	X	X	
Interposer	X	X	
Fan-out for BGA	X		
Stacking of the Fan-out wafers			x
Non conductive glues	x		
Conductive glues	X	X	

Figure 29. The applicability of FAB2ASM technology in different microsystem integration applications.

In particular, the technology will be benchmarked with the integration VCSEL into a silicon bench. This will overcome major bottleneck in the current technology, namely efficient coupling and precise alignment (+/- 1µm) of optical laser sources into a silicon photonic benches, when produced in high volume.

The results obtained during realization of the FAB2ASM project are going to have a significant technological impact on further deployment of the long- wavelength VCSEL as a standalone device and also as a component for integration into silicon photonics platforms. Generally speaking the passive components on silicon photonics platforms such as optical waveguides, optical multiplexers/ de-multiplexers, modulators, filters, etc. have a high level of technological maturity, while there are no silicon – based lasers yet. Thus the hybrid integration of the conventional laser chips fabricated from compound semiconductor materials with silicon photonics platform elements is the only viable solution for ensuring its full functionality. From the two main semiconductor laser light sources, edge emitting and surface emitting, the most appropriate choice for a large number of application in silicon photonics is the Long Wavelength (> 1200 nm) Vertical Cavity Surface Emitting Laser (VCSEL). Low electrical power consumption, circular optical beam profile and emission wavelength compatible with the transmission spectra of the silicon, make the long wavelength VCSEL an ideal candidate for laser light source for integration on silicon photonics platforms. The design of such

VCSELs is giving the opportunity to assembly them onto silicon photonic chips by using the same assembling procedures applied to surface mountable devices.

In the frame of the project we have been fabricated 1490 nm spectral range VCSELs with different footprints. In terms of technological impact it has been demonstrated that the smallest footprint device (125 x 125 um) can be fabricated without introducing penalties on device performance and also that such device can be successfully integrated on Si-platform using liquid assisted self-alignment technique. These two elements – appropriate VCSEL device and assembling technology are paving the ways for decreasing the cost of the component itself and also for development of high precision, high through put assembling systems.

In general, the results of the FAB2ASM provides the European semiconductor industry a new tool in integration technologies for their individual product requirements, which has a positive impact on the competitiveness of European industry in microelectronics and microsystems technologies.

4.2. **Economic impact**

FAB2ASM will provide a competitive edge to European semiconductor industry and equipment manufacturers, against competitors in USA and Asia through lower manufacturing cost.

Packaging in semiconductor and microsystems industry is absorbing an increasing share of costs compared to the waferfab costs (die costs). Traditionally assembly costs were at a 15% level of finished package costs. Nowadays this level is often exceeding 50% for new packages. Innovative and competitive Si-integration and packaging concepts need to be explored and developed in order to be able to meet the stringent cost demands.

As an application of the technology platform developed in the FAB2ASM, passive alignment of a light source on Silicon substrate will make possible the fabrication of very low-cost photonic ICs. To date, the mounting of a single mode laser on its optical sub-assembly is done using active alignment, which is a lengthy and costly process. Being able to mount a single mode VCSEL laser using passive alignment drastically reduces the assembly time and therefore the cost of the laser optical subassembly, opening the way to the fabrication of very low-cost Hybrid Photonic Silicon IC.

The results of FAB2ASM are positioning Beam Express as a manufacturer of the long wavelength VCSELs having a specific design features compatible with self-alignment assembling technique as well as with conventional ones. Such light sources are suitable for integration into Si- photonics platforms, which can be used for development of optical transmitters for different optical data transmission applications such as Fiber-to-the-Home (FTTH), high speed (40 and 100 GB/s) Ethernet etc. The overall market size of the corresponding assemblies for such applications is estimated to be up to 100's million pieces per year. This is a good opportunity for BX for deployment of VCSEL products in this field and opens the possibilities for successful business in the coming years after the project.

For NXP, having the technology available to produce very small semiconductors at a competitive (low) cost level, is a major requirement. The semiconductor portfolio of NXP is dominated by products where the packaging cost is a significant part of the total cost price. Similarly, the market demands smaller products to fit in portable applications, such as portable phones.

The technologies developed in FAB2ASM matches these two requirements: semiconductors can be assembled at higher speed (because alignment is less critical) and also more accurately (because the self-assembly is more accurate than mechanical alignment).

Some of the results of FAB2ASM has already been applied in the production lines of NXP, which already improves the productivity in manufacturing.

4.3. **Societal impact**

The number of people in Europe working in the microsystemm integration market including 3D integration is more than 100.000. By reducing the cost of the packaging process by speed up and self-align, competitiveness will increase, with growth as an opportunity for the company.

Due to the continuous need for higher and higher bandwidth, largely driven today by consumer internet video, digital television and enterprise back-up applications, it is expected that optics is going to invade many new consumer applications. It is foreseen that optical silicon ICs, today a high-tech and expensive solution, will become a commodity product produced in very large volume, leading to e.g. a larger adoption of fiber-to-the-home technologies.

Furthermore, the technologies developed in FAB2ASM will lead to a significant reduction of power consumption in two ways: directly, by the reduction of power consumption in manufacturing through higher output of equipment, and indirectly, by building low-power photonic solutions, thus decreasing the power consumption of next generation of Telecom equipments. This will contribute to the environmental European initiative for saving energy.

Addressing the expected impact of the topic FoF.NMP.2010-3
establish and to support a competitive European nano- and μ-manufacturing industry, creating favourable conditions for private investment and economic growth
FAB2ASM reinforces the competitiveness of European nano- and μ-manufacturing with a technology that pushes beyond the efficiency-precision chart of the state-of-the-art integration technology. The partners in the consortium compose a major share of European industry in nano- and μ-manufacturing. With the results of FAB2ASM, it is expected to improve competitiveness of European nano- and μ-manufacturing industry.
enable new factories, new equipments and new products with micro- and nano-scale functional features, integrating results from manufacturing of nano-materials & nano-surfaces and production technologies for μ-components;
FAB2ASM utilizes innovative nanostructured surface for the interfacing between microcomponents, and provide superior functionality for both positioning and bonding. This provides a promising path that integrates often scientific oriented nanotechnology with industry relevant manufacturing technology. Such combination leads to new manufacturing equipment and production processes.
upgrade existing factories by means of effective integration of nano-manufacturing processes
The technology developed by FAB2ASM based on innovative micro-nano integration can be adapted into flip-chip/die bonding equipment and upgrade the existing factory to a new level of performance and cost effectiveness. In contrast to many other technology such as fluidic self-assembly, which will use a totally different process than the current industry base, the FAB2ASM technologies can preserve the current investment of industry and reuse a great amount of technology know-hows that is the advantages of European industry.

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6. Address of the project website

http://www.fab2asm.eu/

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