Project no.

FP6-2003-IST-2-511466

Project acronym

MEPHISTO

Project full title

Merger of Electronics and Photonics Using Silicon Based Technologies

Instrument: STREP
Thematic Priority: IST-2002-2.3.2.2
Optical, opto-electronic, photonic functional components

Publishable Final Activity Report

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Project coordinator name:	Dr. Norbert Grote
Project coordinator organisation name:	Fraunhofer-Institute for Telecommunications, Heinrich Hertz Institut

Table of contents

0 Project information

Partners

1. Fraunhofer Institute for Telecommunications, Heinrich-Hertz-Institut, Berlin, Germany (Coordinator)

2. Okmetic Oyj, Vantaa, Finland

3. Freescale Halbleiter Deutschland GmbH, Munich, Germany

4. Hymite AS, Lyngby, Denmark (until April 2006)

5. VTT Technical Research Center of Finland, Espoo, Finland

6. Intexys Photonics SA, Toulouse, France (since Dec 2006)

Duration: August 2004 – October 2008 (incl. suspension phase and amendments)

Available total budget/EC contribution: 4,057 k€ / 2,100 k€ (not exhausted)

Web site: www.hhi.fraunhofer.de/mephisto

1 Overview of general project objectives

The increasing demand for photonics components featuring enhanced functionality, complexity, miniaturisation, performance and reliability and requiring reduced assembly costs is believed to be achievable only by integration technologies. In particular, the call for smaller and smaller footprint of devices has been attracting much awareness today in order to accommodate more functions in smaller form factor modules.

Basically the integration technologies pursued worldwide may be divided into the following categories:

Monolithic integration using *one* common material system for the different devices to be integrated. Compound semiconductors – for telecommunication applications usually InP based compounds – are the materials of choice, in principal allowing for implementing all the active and passive optical functions desired for those components, and electronic devices as well. Having been a dream since the late 1970th this approach has seen remarkable progress in recent years, especially driven by the US company Infinera.

With **hybrid integration** *different* material technologies are employed to ”take the best from different worlds”. Integration is accomplished by attaching different device chips - such as laser and photodiodes, SOA, electronic ICs, but also thin film filters - to an optical waveguide board utilising suitable micro/nano-assembly techniques. To this end different material platforms are utilised including silica-on-silicon, SiON, ion-exchanged glass, and also polymers, each of them having inherent virtues and drawbacks. Hybrid integration itself offers advantages with respect to optimising overall performance due to application of different materials; yield management; versatility and flexibility, and others. The latter aspect renders this technology especially useful for small to medium production volumes.

An integration platform that has attracted extremely high interest in recent years is **silicon-on-insulator (SOI)** where Si acts as core waveguide layer optically isolated from the Si substrate by an

intermediate SiO2 layer. Using this material optical waveguides of widely varying dimensions and related device structures can be implemented, and naturally electronic circuitries. In addition, realisation of high-speed electrooptical modulators was successfully demonstrated by different groups, and if combined with Ge films high-speed detectors can also be monolithically integrated. In this way SOI can serve as platform for quasi-monolithic integration ("Si Photonics") as well as for traditional hybrid integration, and can hence cover a wide intermediate range between truly monolithic and hybrid optical integration. What is still far out of reach is the realisation of practical Si based laser structures still necessitating hybridisation for such devices. One major advantage of using SOI is the CMOS fabrication compatibility thus exploiting all the advantages of Si technology. Further synergy is offered by the wide use of SOI in MEMS applications.

The Mephisto project was focussed on hybrid integration on SOI. Integration of optical components implemented in SOI togethjer with active III-V devices (namely laser diodes) and Si electronics was to be developed and demonstrated. A 40 Gbit/s optical transmitter comprised of four dense-wavelength multiplexed (DWDM) lasers each capable of 10Gb/s modulation was chosen as test vehicle for developing the key technologies needed for SOI based hybrid integration and demonstrating them. The individual components adapted for integration– SOI based optical wavelength multiplexer, InP based DWDM laser diodes, and dedicated electronic laser driver circuits – had to be developed. In addition various technologies and device structures related to SOI were investigated for potentially utilising them in future generations of integrated components.

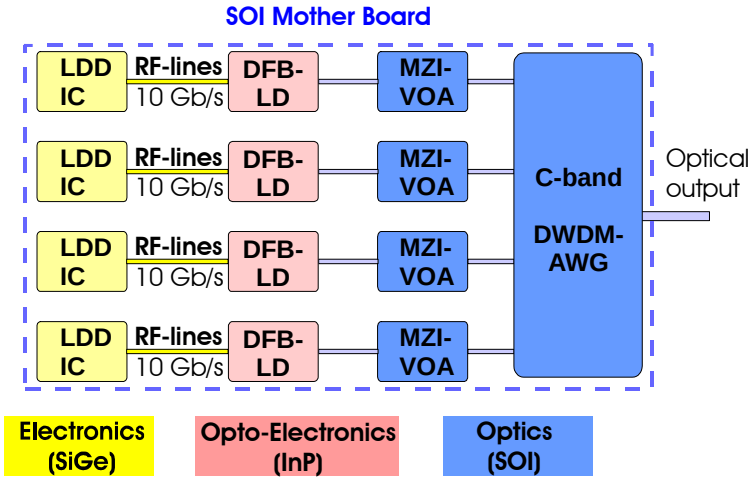


Fig. 1: Schematic representation of the integrated transmitter to be demonstrated in Mephisto employing hybrid integration (LDD = laser diode driver; DFB-LD = single mode laser diode; MZI-VOA = Mach-Zehnder interferometer based variable optical attenuator to enable power equalisation in the different channels; DWDM-AWG = dense wavelength division muliplex arrayed waveguide grating forming the wavelength multiplexer)

Initially, the Mephisto project was started to use SOI as hybrid integration platform *onto* which active III-V devices and electronic Si chips were to be integrated. In this approach the SOI board serves two purposes: *bench* for hybrid integration, and *optical waveguide* board for implementing optical functions, namely wavelength multiplexers and optical attenuators. Fig. 2 illustrates how integration would be carried out in this approach in principal.

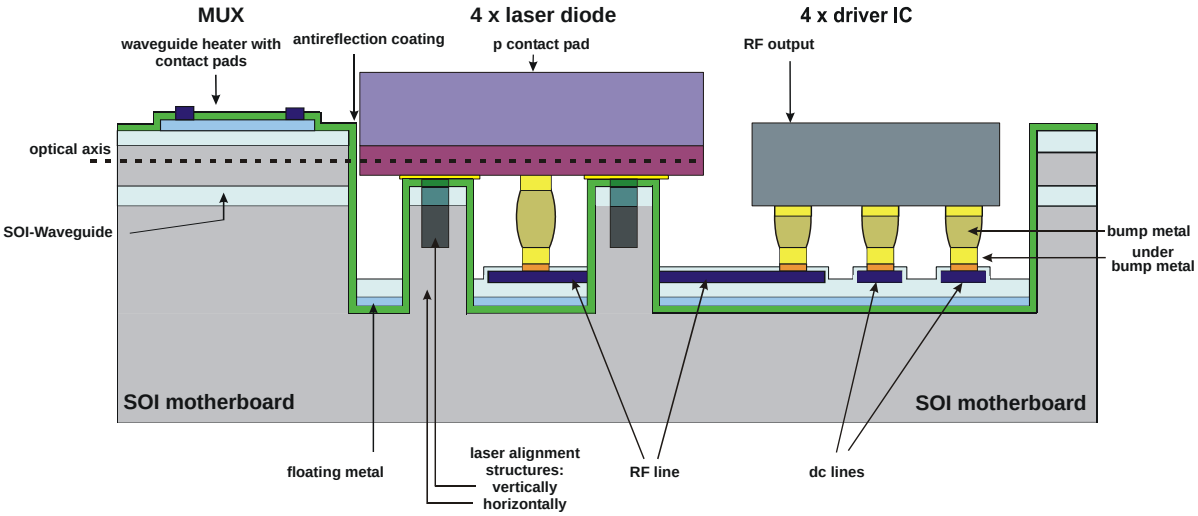


Fig. 2: Original integration scheme planned in Mephisto for mounting active optical and electronic devices onto an SOI waveguide board containing the optical wavelength multiplexer (MUX, including a variable optical attenuator)

After the first half of the scheduled 3 years project duration, when Intexys Photonics joined the project as a new partner (see section 3), the project was revised and restructured and an alternative technology pursued since then. The major change was that the SOI waveguide circuit (AWG and VOAs), the lasers, and the driver ICs were to be hybridly integrated onto a common Si optical bench (SiOB) rather than using the SOI waveguide circuit board itself as optical motherboard. The SiOB serves as mechanical mounting platform for the different individual chips also carrying the electrical dc and rf connection lines but providing no optical functions (Fig. 3).

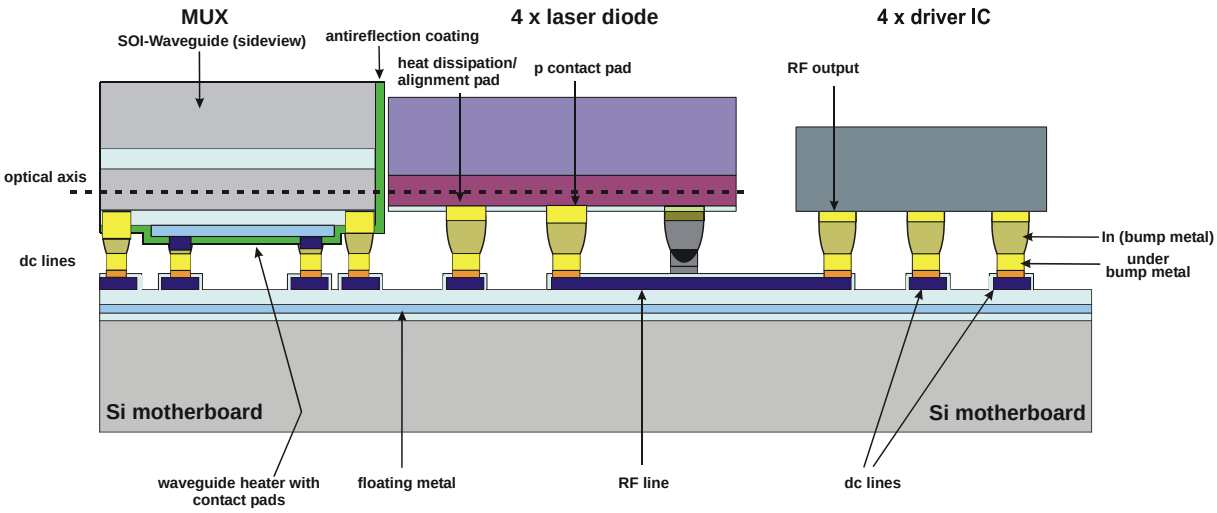


Fig. 3: Silicon optical bench (SiOB) based hybrid integration scheme.

The key to this approach was a self-aligned flip-chip technology using Indium bumps which has been the unique know-how of Intexys. One particular challenge in this solution was the achievement of precise passive optical coupling of the lasers and the SOI waveguides. There was a number of other open issues that needed to be investigated including the mounting of arrayed laser chips.

The SiOB solution is believed to offer some distinct advantages: The fabrication of the SiOB board is less complex and demanding due to its planarity, and hence to be more cost effective. The components to be integrated can be tested and selected individually prior to assembly, thus providing better yield management. The consumption of the relatively expensive SOI material is reduced as the active chips are now placed on an inexpensive Si wafer.

2 Potential applications

Once developed hybrid integration is believed to be applicable to a large number of photonic components in a versatile manner. Applications will be not only in the field of optical telecommunications and data communications but also in optical interconnections, sensors and metrology, and related areas. An example may be a broadband light source for fiber sensors or optical coherence tomography applications being comprised of multiplexed LED spectra.

Multi-wavelength integrated transmitters in particular will be very useful in different parts of optical networks, as summarized in the following diagram. Different wavelength channel spacings ranging from DWDM (> 50GHz/0.4 nm spacing) to CWDM (20 nm) including intermediate solutions (dCWDM, e.g. 5; 10 nm) will be applied. 4x10 Gb/s to enable low-cost 40 Gb/s transmission, and 4x25Gb/s and

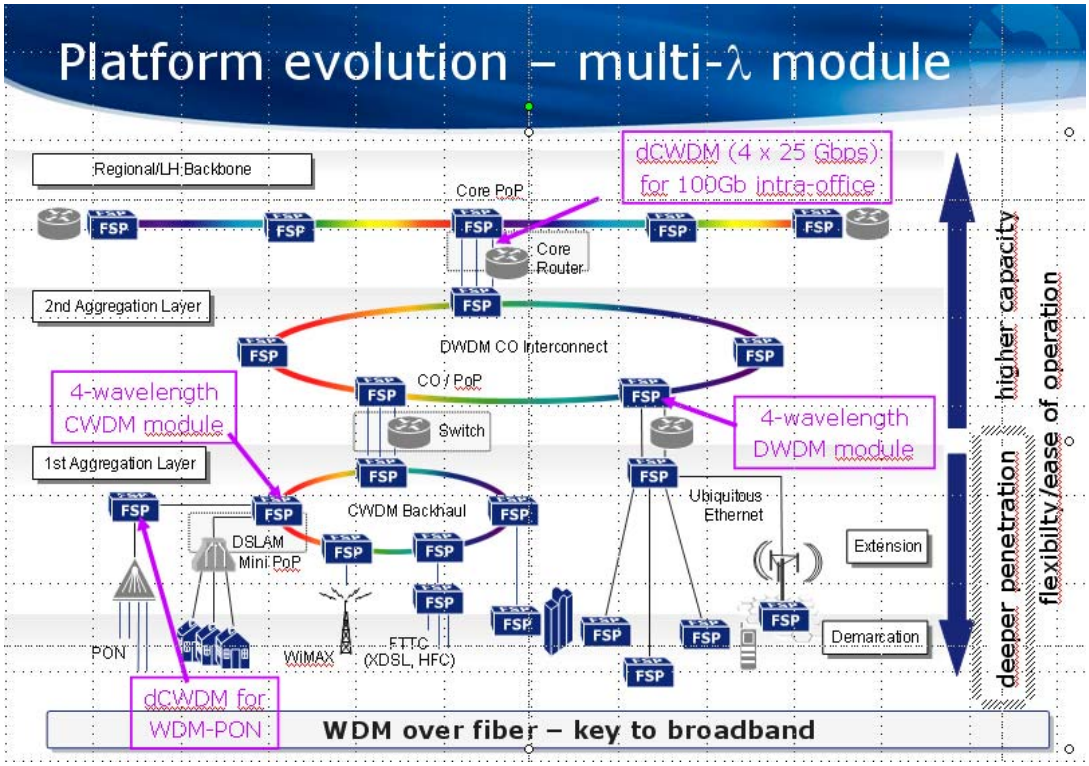


Fig. 4: Application scenarios for multi-wavelength transmitter modules (courtesy: ADVA Optical Networking, Meiningen)

even 10x10 Gb/s for 100 Gb/s transmission are potential solutions that were recently agreed in standardization bodies concerned. In the frame of next generation optical access networks use of both CWDM and DWDM technology is intensely being discussed. For this low-cost transmitter and receiver devices with a large number of channel counts and low footprint are demanded. In view of these perspectives the goals of the Mephisto project were well defined even before these applications really emerged.

3 History of the project

The MEPHISTO project suffered from exceptional circumstances which eventually led to its early termination. A history in brief:

- February 2006: Clean room of VTT partly destroyed by fire; took almost 1 ½ year to fully re-establish process performance for Mephisto devices
- April 2006: Consortium partner Hymite resigned from the project because of strategic changes of the company
- May – November 2006: Project suspended to allow for searching a new partner to replace Hymite; Intexys Photonics acquired as new partner, and integration technology concept in Mephisto substantially revised; preparation of 1st amendment
- December 2006: Approval of 1st amendment, project to end March 2008; project work resumed
- 2008: continuous delays in the project mainly due to Intexys related bottlenecks; increasingly emerging business problems at Intexys seriously affect the project
- March 2008: Approval of 2nd amendment, project to finish end of 2008
- October 2008: Intexys' notification of insolvency and termination of Mephisto partnership
- November 2008 - January 2009: 2nd suspension phase; consortium proposes plan to finalize the project without new partner, 3rd amendment submitted
- January 2009: Decision to terminate project by Oct 31st, 2008

It is not the intention to blame solely Intexys for the unsatisfactory completion of the project. However, the integration technology pursued in the project since Intexys joined was strongly relying on their specific expertise in flip-chip technology and the technical resources which were not available with any of the other contractors. It is very understandable that in order to survive as a company absolute priority had to be given to business demands which apparently detracted too much resources and attention from the project. Intexys' persons involved in the project were undoubtedly highly motivated and willing to do the best to contribute to Mephisto.

4 Achievements and major results

4.1 Basic technologies

4.1.1 SOI wafer technology

In Mephisto the principal material basis has been silicon-on insulator(SOI) in which the optical waveguide structures and devices were implemented. In the first integration approach pursued it was simultaneously to serve as assembly board for hybridization. To be able to design and reproducably fabricate optical waveguide devices precise control of the effective optical refractive index and thus of the thicknesses of the waveguiding layers involved is of utmost importance. To this end optimization of SOI wafers for optical applications represented part of the project, particularly aiming at a thickness

uniformity of < 0.5 µm on 150 mm wafers. The project partner Okmetic, a world leading manufacturer of SOI wafers, was mainly responsible for this task.

There are two kind of SOI wafers: (a) SOI wafers with *thin* active silicon layer and (b) SOI wafers with *thick* active layer. The first kind of SOI wafers is most common, but those wafers are almost exclusively used for submicrometer VLSI electronic devices. The active layer thickness is << 1 µm, typically ranging from 20 nm to 220 nm. Such wafers are available up to 300 mm diameter in size. A typical example of an end product made on this kind of SOI wafer is a microprocessor. Thin layer SOI wafers are made mainly using a layer transfer technology (named SmartCut® by the leading manufacturer).

SOI wafers with thick active layer have silicon layer with typical thicknesses ranging from from 2 µm to > 100 µm. Earlier wafers with 150 mm diam. were most commonly used, but nowadays usage of 200 mm wafers is significantly increasing. Thick layer SOI wafers are produced mainly by bonding two wafers together, followed by mechanically thinning (grinding) and chemo-mechanical polishing (CMP) the top layer. Typical applications are in the field of sensors (MEMS) and high voltage devices, and of course photonics, as in Mephisto. Okmetic is manufacturing SOI wafers with up to 200 mm diameter with thick active layers only. In Mephisto SOI wafers with 4 µm Si technology were continously utilized.

A crucial parameter of SOI wafers is the uniformity of the Si layer.With *thin* Si layer wafers made by layer transfer uniformities within about +/- 1 nm up to 40 nm layer thickness and +/- 3 nm up to 90 nm layer thickness are achievable. If the layer thickness is increased to 1.5 µm, the uniformity deviation may rise to +/- 5%. When increasing the layer thickness by epitaxial growth of additional Si the typical achievable uniformity is +/- 2% in best processes.

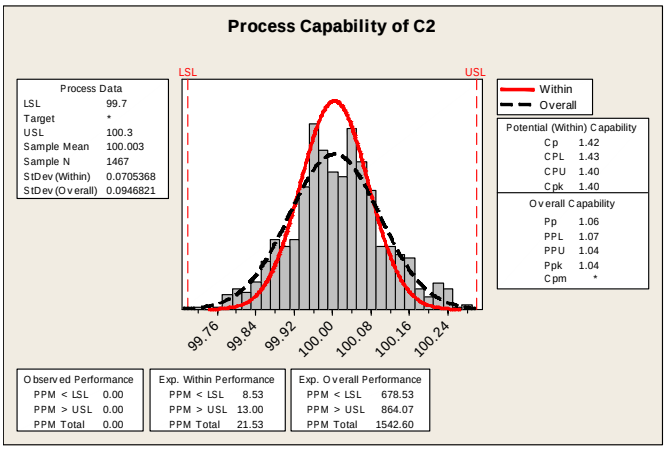


Fig. 5: Example of current SOI layer thickness variation for a 100.0 µm thick Si layer. The process capability can meet the requirement ± 0.3 µm for thickness variation making these wafers well applicable to high performance optical waveguide devices.

With bonded *thick Si* layer SOI uniformities of +/- 0.5 µm had to be considered as benchmark previously, increasing to > +/- 1µm in case of very thick (100 µm and more) layers. In Mephisto, by carefully investigating the various process details involved Okmetic has developed and optimized a process which allows for reproducably achieving +/- 0.3 µm tolerance only, independent of the final layer thickness. In Fig. 5 the thickness distribution is illustrated for a 100 µm-Si, 150 mm diam. SOI

wafer featuring a +/- 0.3% (+/- 0.3 µm) non-uniformity only. Although the combined SmartCut®+ epi process can provide wafers with even better uniformity for wafer thicknesses < 15 µm, there are other restrictions, such as limitations in making highly doped active layers or in selecting bond interfaces freely. Moreover the additional cost of epitaxial overgrowth renders these wafers expensive. Therefore for thick Si layer SOI material wafers made by bonding and mechanical thinning process are usually preferred, and thanks to the developmental work performed in Mephisto Okmetic's wafers are at the leading edge today regarding uniformity.

4.1.2 Advanced waveguide structures

Investigations were also carried out on advanced optical SOI waveguide structures that are generally attractive for future generations of optical SOI based components but were not intended to be included in the project demonstrator. First, vertical tapers were studied to enable low-loss optical spot size conversion between a single-mode fiber or a laser diode and a SOI waveguide, or between waveguides of different geometries. Secondly, vertical couplers between two superimposed SOI layers were studied to support spot-size conversion, 3D waveguide integration and polarisation manipulation. Thirdly, tight waveguide bends and waveguide mirrors were designed and fabricated intending to significantly reduce the size of optical devices made on SOI. Depending on the refractive index conditions, their overall size may be largely determined by waveguide bends the allowed radius of which is limited by the associated radiation loss.

(a) Vertical tapers

The vertical taper is a structure that adiabatically changes the waveguide thickness to convert the mode field of an input beam (e.g. from a single-mode fiber) into the one of the waveguide on the SOI chip. A schematic 3D view and the operational principle of the vertical taper are illustrated in Fig. 6 which also shows that adiabatic conversion can be accomplished even in the case of finite mask

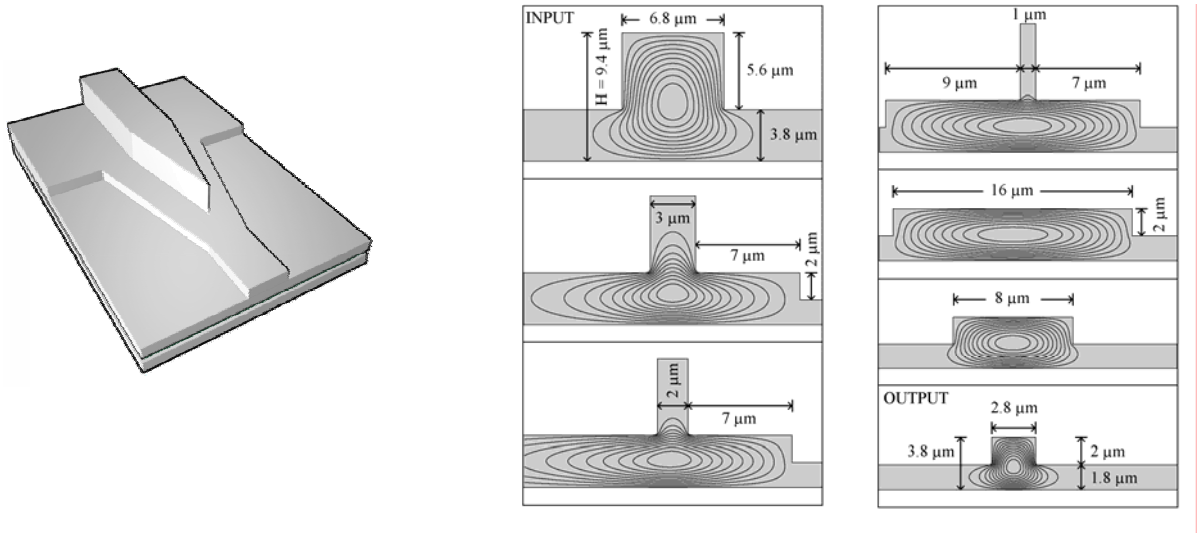


Fig. 6: Schematic view of a vertical taper fabricated with multi-step patterning. Note that in reality the taper is much longer. Input (e.g. from fiber) at the top side, output into chip waveguide: bottom side *(left).* Different cross-sections along the vertical taper with calculated intensity distributions for the fundamental TE mode. The results for TM polarisation are almost identical. Misalignment of 1 µm is assumed between the two masks. Otherwise dimensions are identical to those measured from the fabricated devices in 9 µm SOI (*right*)

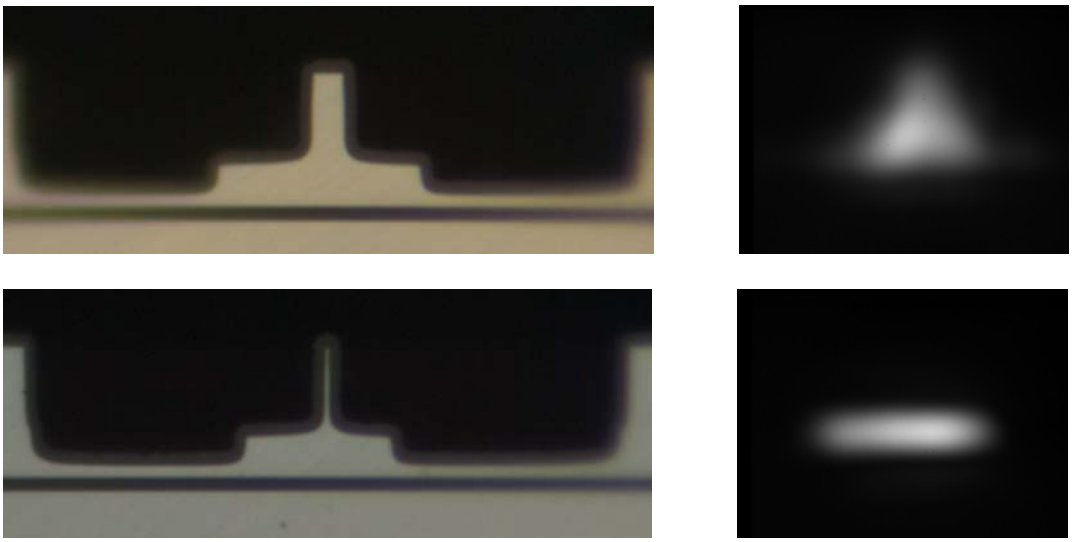


Fig. 7: Microscope images of two cross-sections of a vertical taper (left) and corresponding IR images of the optical output from the same cross-sections (right). The heights of the thicker and thinner SOI waveguide are 9.5 and 4 µm, respectively. The width of the narrow tip in the lower figure is less than 100 nm.

alignment accuracy. By tuning the etch depths the type of the thinner waveguide can be adjusted between a shallow-etched rib waveguide and a through-etched strip waveguide. Tapering between 9 µm and 4 µm, and 4 µm 2 µm thick SOI waveguides could successfully be demonstrated. Microscope images and IR output images of such vertical tapers are shown in Fig. 7 for two cross-sections.

Measured results are summarised in Fig. 8. The lowest taper loss obtained was as low as 0.09±0.13 dB for TE and 0.17±0.13 dB for TM polarisation. Thus the demonstrated multistep-type vertical taper structures have proven not only to be optically highly efficient but also tend to be robust and fabrication tolerant.

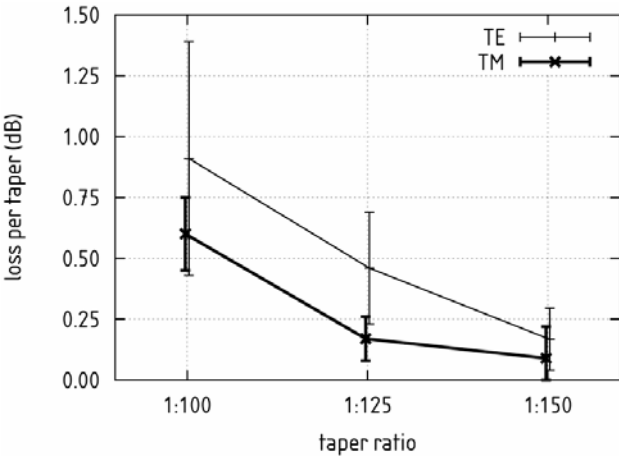


Fig. 8: Insertion loss of a vertical taper in 4 µm SOI as a function of the linear tapering ratio.

(b) Vertical couplers

The goal of this activity was to develop adiabatic coupling between two SOI waveguide layers placed above each other and separated by a very thin oxide layer. Such coupling structures are considered very useful for realising again spot-size conversion but even more 3D photonic integration and polarisation splitting. The proposed coupling principle can be applied to any SOI layer thickness. Since the main focus in Mephisto was on 4 μm thick SOI waveguides the vertical couplers were primarily designed to couple light from 4 μm thick waveguides to either 2 or 8 μm thick waveguides, or vice versa. The lower SOI layer was always thicker (4 or 8 μm) and patterned into a multi-moded strip waveguide. The upper SOI layer was thinner (2 or 4 μm) and either unpatterned or patterned into a single-moded rib waveguide.

The first device had a strip waveguide patterned into a lower SOI layer, an oxide layer everywhere around the coupling region and a rib waveguide patterned into the upper SOI layer. The fabrication process included: (lower) SOI patterning with deep trenches, shallow etching (1-2 μm) around the coupling region, oxide filling, chemical-mechanical polishing (CMP), bonding of an unpatterned SOI wafer, substrate removal by grinding and wet etching, BOX removal, patterning of the upper SOI layer and cladding deposition on top. A schematic cross-section of such a structure is illustrated in Fig. 9, along with a mask design for a test device and the expected optical behaviour.

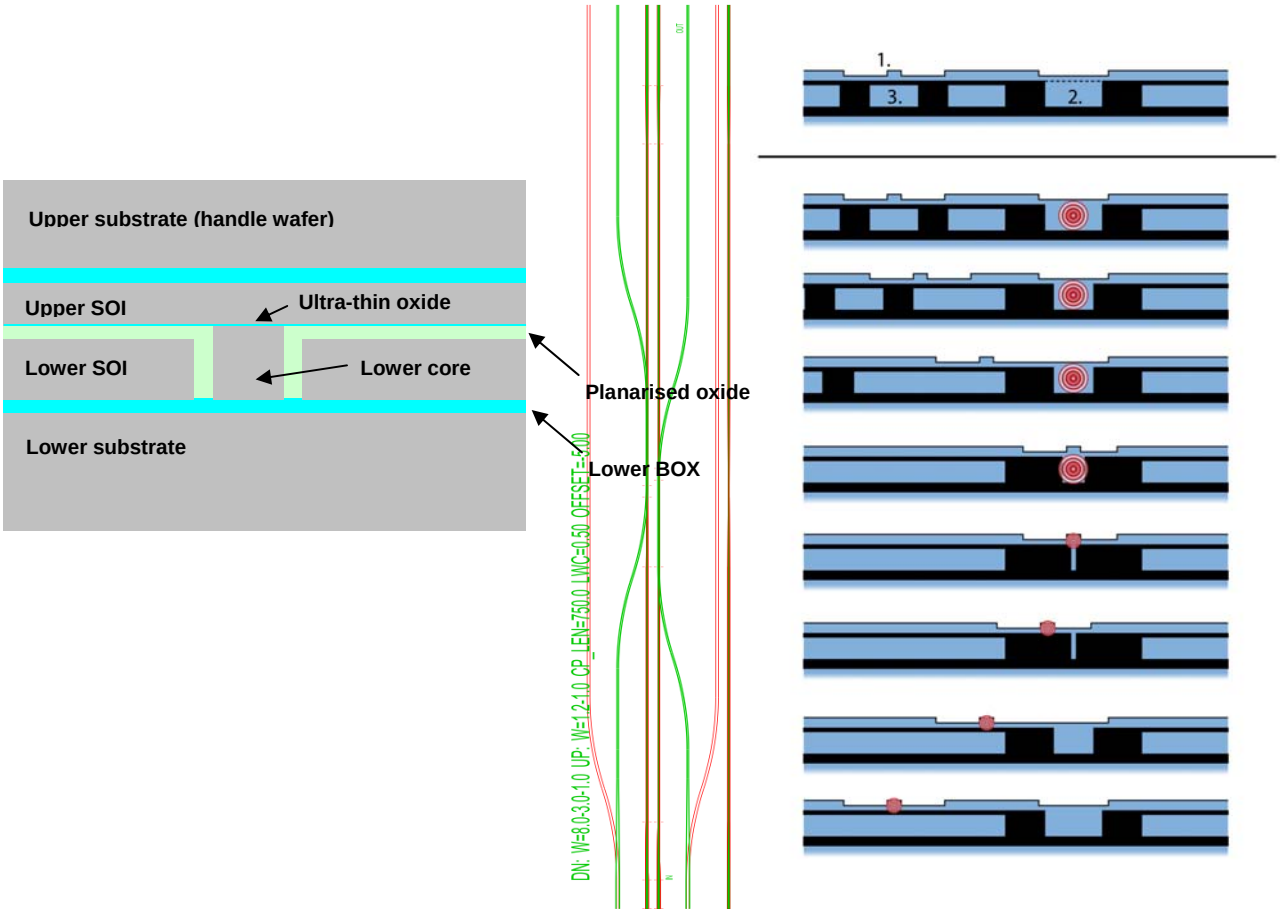


Fig. 9: Vertical coupler: schematic cross-section (left); mask design of a test component (middle); expected optical behaviour of the vertical coupler illustrated with a number of cross-sections along the device (right).

Based on simulations and preliminary experiments it could be concluded that the vertical gap between the SOI layers should be <20 nm, thinner than originally estimated. Various technological problems were encountered in the realisation of such devices, e.g polishing and trench filling issues. To overcome those problems different approaches were experimentally tested. Optical coupling between the layers could be demonstrated, but the fabricated vertical couplers did not exhibit the desired adiabatic operation.

(c) Tight waveguide bends

Groove-type bends and waveguide mirrors, as depicted in Figs. 10 and 11, were developed and successfully demonstrated. The purpose of these optical waveguide elements is to change the propagation direction of the wave-guided light either adiabatically (bends) or abruptly (mirrors). In this way they can help significantly reducing the footprint of waveguide circuits by locally increasing the effective horizontal index contrast.

The bending structure is sketched in Fig. 10 which also shows the effect of the etched structure on the guided wave. The demonstrated structures were formed in both 4 μm and 9 μm thick Si waveguide layers by multistep patterning. This way the applicable bending radius of a 90 deg bend in 10 μm thick rib waveguide could be reduced almost by an order of magnitude, i.e. from centimetres to millimetres. In the thinner waveguides the relative improvement was of the same order. When comparing bends of 1 mm radius to equally long straight waveguides no extra loss could be measured. Whenever the bending angle is large a groove-bend has smaller insertion loss (dB/90°) than a corresponding classical bend that is much longer.

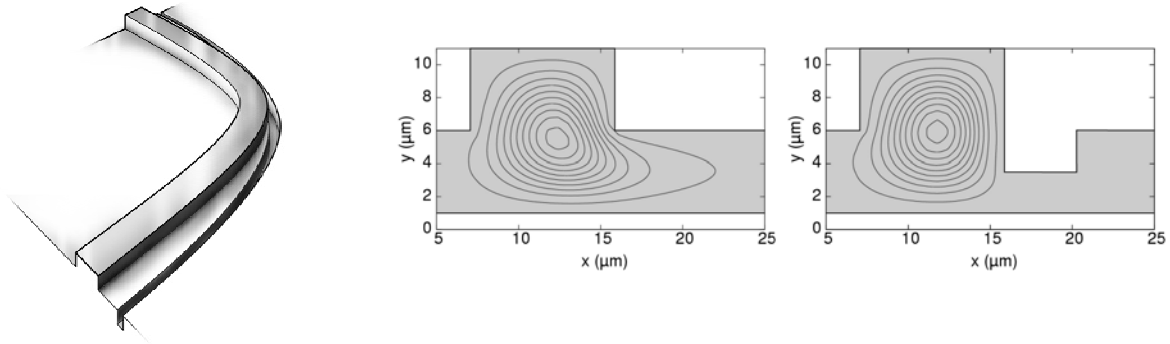


Fig.10: Tight waveguide bends: Schematic structure (left) and calculated mode profiles for a traditional rib waveguide bend (middle) and a groove bend (right). The contour lines illustrate the intensity distribution of the fundamental mode bent with a radius of 20 mm. Both waveguides are 10 μm thick and 8.8 μm wide. Simulation results show clearly the contraction of the optical mode distribution in the grooved bend.

(d) Waveguide mirrors

A waveguide mirror represents an even more compact structure to turn the propagation of light. These structures were implemented by vertical etching as illustrated in Fig. 11.

Fig. 11: Basic design of a waveguide mirror (left) and microscope image of a waveguide mirror fabricated in 4 µm SOI

Losses measured on mirrors in 4 µm SOI waveguides are summarized in table 1. Losses of well below 1 dB were obtained. Apart from the size advantage, a mirror has smaller insertion loss (dB/90°) than a corresponding classical bend, at least when the bending angle is large.

	Loss (dB)			
Offset (µm)	**TE**	**TM**	**Average**	**PDL**
-0.2	1.10	1.07	1.08	0.03
-0.1	1.01	1.13	1.07	0.12
+0.1	0.79	0.88	0.83	0.09
+0.2	0.80	0.79	0.79	0.01

Tab. 1: Insertion loss of 90° mirrors in 4 µm SOI with variable offsets in the mirror position with respect to the symmetrical reflection point of the optical axis.

4.2 Single devices

The following block diagram (already depicted in fig. 1 in the first section) represents the integrated 4x10 Gb/s transmitter component that was to built in the Mephisto project. In the following section the individual devices which have been developed for the hybrid flip-chip technology based assembly are described. Basically there are three groups of devices:

- SOI based wavelength multiplexer + variable optical attenuator (for individual adjustment of optical power in each channel)
- 10 Gb/s DFB laser diodes for each DWDM wavelength channel
- Laser driver IC

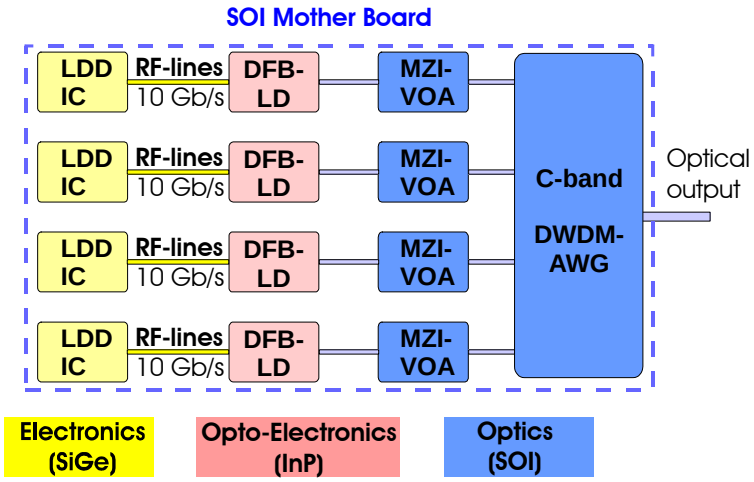


Fig. 12: Block diagram of the integrated transmitter to be demonstrated in Mephisto

4.2.1 SOI based optical wavelength multiplexers

The optical wavelength multíplexers developed relied on Arrayed waveguide grating (AWG), and the integrated VOA on thermo-optically controllable Mach-Zehnder interferometer (MZI) structures. For the demonstrator device the AWGs were designed for C-band wavelengths with a channel spacing of 200 GHz (1.6 nm). 4-8 operation channels were implemented. Besides using the traditional AWG design so-called mirror (M-)AWGs were introduced which were aimed at significantly reducing the footprint of the relative large AWG structures, basically cut by half. Furthermore single CWDM AWG multiplexers were designed and fabricated responding e.g. to the emerging LAN-CWDM standard to be used for future 4x25 Gb/s transmitters. All these components were jointly designed, fabricated on SOI, and evaluated.

For the SOI waveguides a ridge height of 2 - 2.2 µm, a ridge width of approx. 3.4 µm, and a total SOI thickness of 4 - 4.3 µm were used throughout the project yielding an effective refractive index contrast of some 0.7%. These parameters were chosen as a reasonable compromise considering total chip size, laser and fiber coupling loss, optical waveguide and waveguide bending losses, optical cross-talk in AWG structures, thermal issues, and other technological aspects. The waveguide loss was as low as 0.3 dB/cm as best value.

(a) DWDM AWG multiplexer

In Fig. 13 the measured spectral transmission characteristic of a representative 8-ch AWG with 200 GHz channels is shown. Insertion loss is close to 5 dB, and the crosstalk at 26 dB (”floor”). Excellent matching with the specified ITU wavelength channels was achieved, with neligible variation across the wafer. The temperature dependent wavelength shift of the AWG wavelengths was determined to be 0.08 nm/K. Hence, a temperature shift of 20 K is required to tune the wavelength between two neighbouring 200 GHz channels.

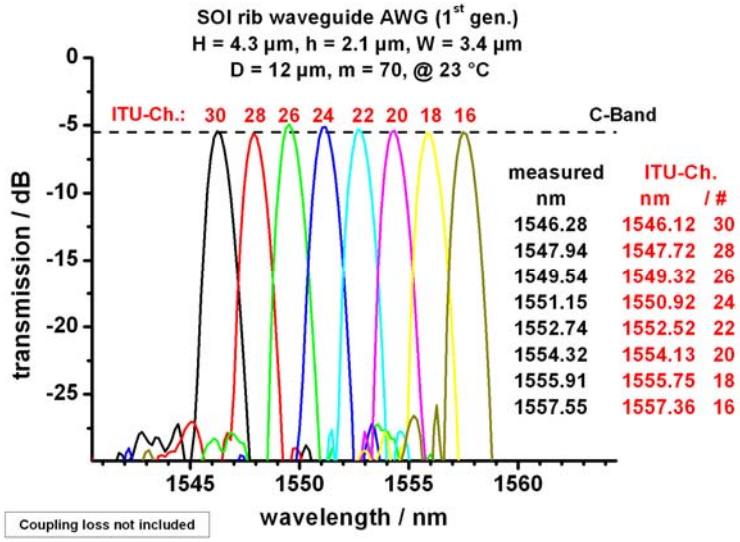
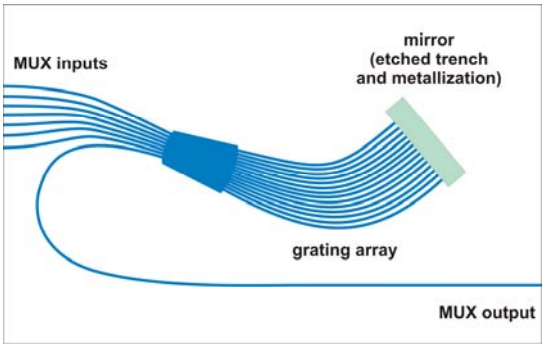
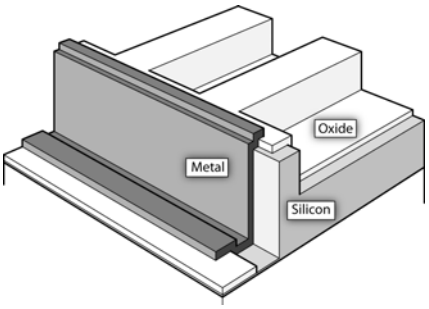


Fig.13: Measured characteristic of an 8-channel 200 GHz AWG, bend radii around 10 mm; (D = waveguide pitch at the star coupler input/output, m= grating order)

(b) Mirror-AWG structures

Mirrored AWG multiplexers were formed by incorporating a vertical mirror facet midway in the phase forming waveguide array to result in a folded lay-out. The mirror is fabricated by etching a trench through the SOI layer and depositing a metal layer in order to reflect the light back into the input star coupler.





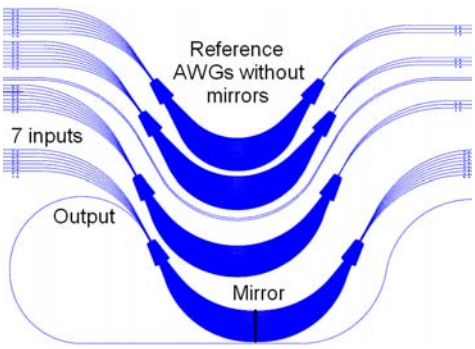


Fig. 14: Schematic layout of an M-AWG with mirrors etched at half path of the arrayed waveguides (left) and formation of the waveguide mirror (right); layout of mask with different AWG versions (bottom)

Fig. 15 shows the measured transmission curve of a M-AWG. The insertion loss proved to be higher by about 1.5 dB compared to the traditional reference AWG from the same wafer. There are options for further improvement yet including optimizing the mirror technology and minor design modifications.

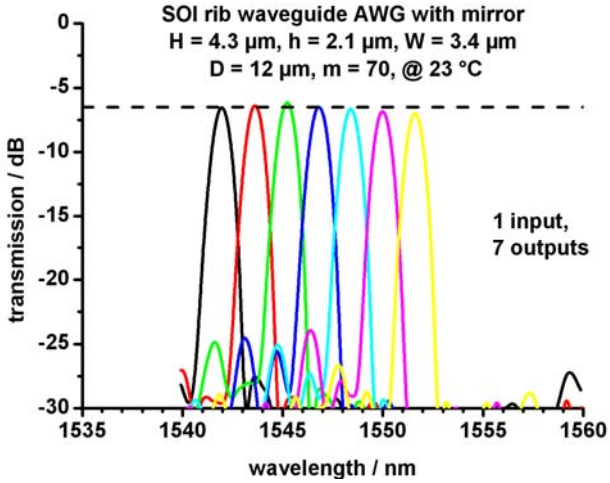


Fig. 15: Spectral characteristics of a mirrored AWG with design parameters corresponding to the standard AWGs (c) CWDM AWG design and performance

(c) CWDM AWG multiplexer

Besides using dense wavelengths, coarse wavelength division multiplexing (CWDM) is another technology of choice, not only for telecommunications but even more for datacom applications to enable 40 Gbit/s and even 100 Gbit/s data transmission. 4 × 10 Gbit/s wavelength multiplexed solutions are agreed in the standardization bodies concerned for implementing 40 Gbit/s,and 10 × 10 Gbit/s and particularly 4 × 25 Gbit/s for 100 Gbit/s transmission. Whereas 20 nm channel spacing is common to CWDM a new standard with 800 GHz (~5 nm) spacing in the 1300 nm window has recently emerged to be used for 4 × 25 Gbit/s transmission. Demanded for CWDM filter devices is a flat-top rather than a Gaussian transmission characteristic. In case of the 20 nm spaced channels the flat-top width has been specified to be 12.5 nm between the -1 dB decay points.

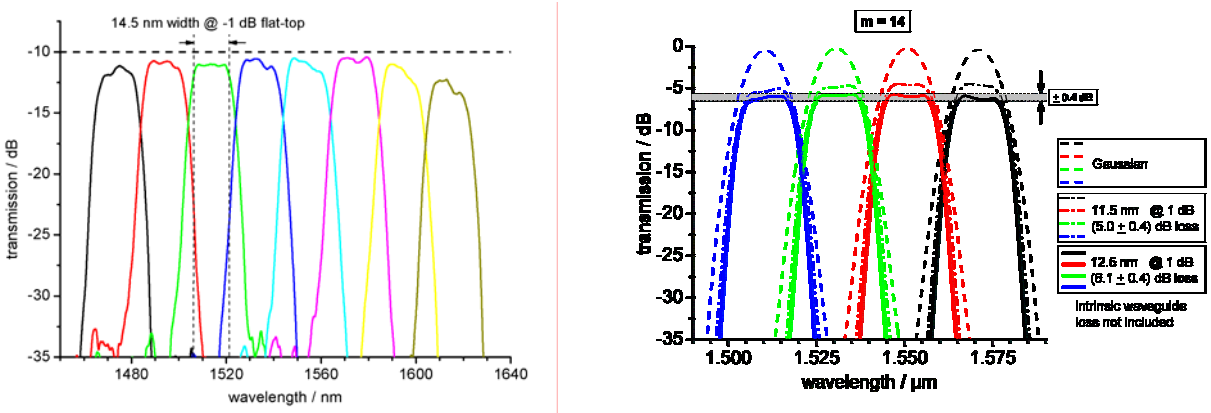


Fig. 16: Measured transmission characteristics of an SOI based 8-channel flat-top CWDM AWG multiplexer (left), and simulated LAN-CWDM results (right)

Fig. 16 depicts the transmission characteristics of a fabricated 8-channel flat-top AWG device which basically meets the flat-top demands though only for the inner channels. The insertion loss of 11 dB is in line with the expected value. The loss difference of 6 dB compared to the Gaussian AWG is mainly due to the formation of the broad flat-top in accordance with simulation results. The relatively high transmission loss of flat-top AWGs will considerably impede their use in integrated components. A simulation study for a LAN-CWDM AWG structure is shown in the right part of fig. 16.

(d) Integrated variable optical attenuators (VOA)

In a VOA the light intensity is adjusted by the imbalance of a symmetric MZI, controlled by heating one waveguide arm. Fig. 17 shows the schematic layout. As 3 dB-couplers standard 2×2 multi-mode interference (MMI) structures and newly designed 1×2 types with body widths of 18 µm and 20 µm were were implemented, the latter one providing higher process tolerances.

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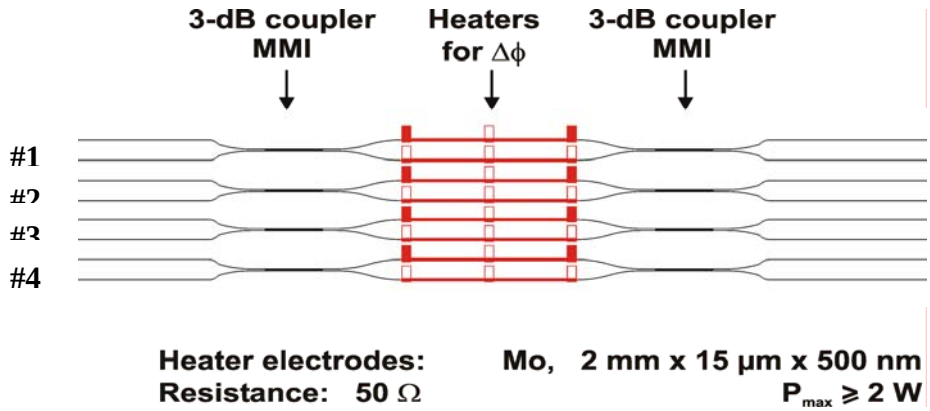

Fig. 17: Schematic layout of thermo-optically controlled MZIs functioning as VOAs. Only one heater stripe will be activated to detune the MZI, whereas the other one is available for redundancy reasons.

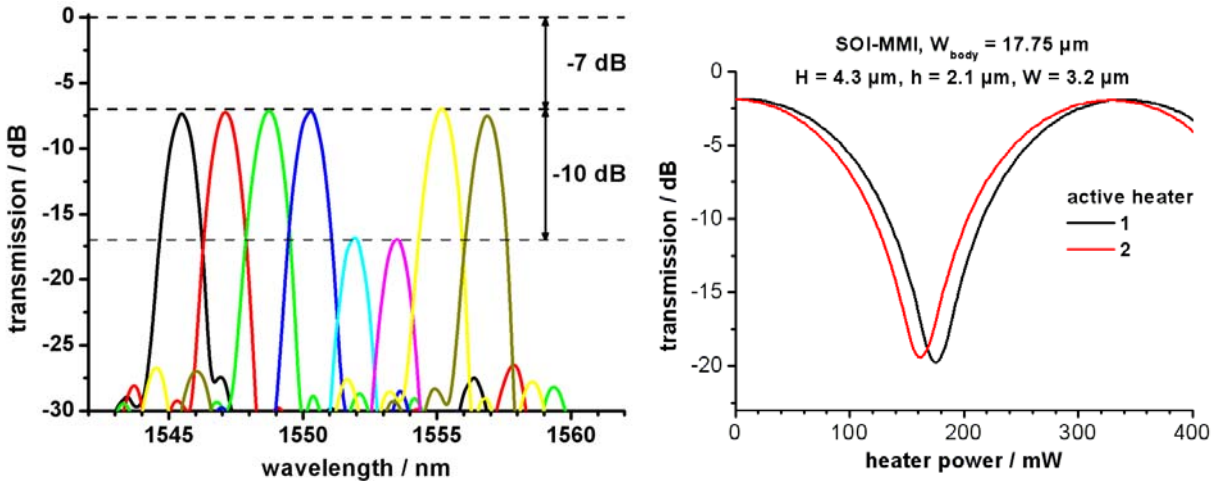

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Fig. 18: Measured characteristics of an 8-channel 200 GHz AWG integrated with a MZI-VOAs; channels #5 and #6 are attenuated by 10 dB in this example. Maximum attenuation of > 15 dB is achieved at 170 mW of heater power (right)

VOA structures were monolithically integrated with both standard AWG and mirror-AWG multiplexers. They exhibited an excess loss of 1.5 dB yielding a total insertion loss of the integrated AWG+VOA of 7 dB. The dynamic range turned out to exceed 15 dB when applying a heater power of about 170 mW. Fig. 18 represents a measured 8-ch AWG+VOA transmission characteristic with two channels attenuated by 10 dB in this case. Thermo-optical switching can be performed with rise/fall times below 10 µs.

4.2.2 Integratable laser diodes

The DFB laser diodes to be integrated in the wavelength-multiplexed transmitter component had to fulfil the following key demands which are much beyond the design and properties of ordinary commercial laser devices:

- 10 Gbit/s modulation capability
- single wavelength emission meeting specified ITU DWDM wavelength grid in the C-band
- adapted beam divergence for enabling high optical coupling efficiency to SOI waveguides
- flip chip compatibility (p- and n- contact on wafer surface) for hybrid integration
- pad layout compatible with co-planar electrical transmission lines on SOI-wafer
- precise height adjustment of active layer and cleaved facet postion relative to flip-chip contacts
- integration of an additional heater stripe to allow for precise wavelength adjustment
- implementation of mechanical alignment features

As regards coupling efficiency, assuming SOI waveguide dimensions as used in the project and a circular input beam of the laser the optimum far-field of the laser beam is characterized by a FWHM angle of around 22° and around 18°, if the SOI waveguide is laterally tapered. Respective simulation results are shown in Fig. 19. These values are to be compared to some 30...35° representing the far-field of conventional laser diodes featuring a so-called buried heterostructure (BH) design. Only this structure garantuees a more or less circular beam shape. As a consequence, to minimize coupling losses tapered laser diodes are required to adjust the far-field.

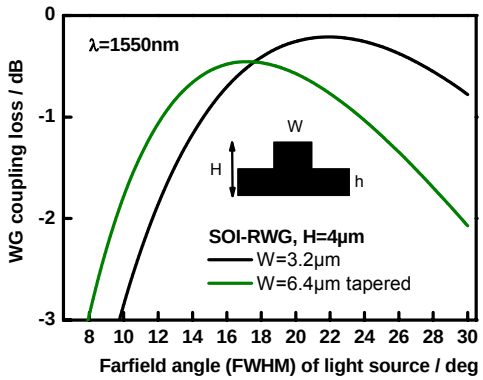


Fig. 19: Calculated butt-coupling efficiency of laser/SOI waveguide with given dimensions as function of the laser beam divergence (circular beam)

To this end two different tapered DFB laser structures relying on a BH design were developed in Mephisto. In the beginning a laser structure with an integrated *passive* optical taper was pursued. In the course of the project, however, an innovative design was introduced which uses an active taper in that the active laser stripe is tapered itself. Due to various inherent advantages of this kind of laser,

which is referred to as curved-stripe (CS) DFB laser, the focus was on this structure only later in the project. The CSDFB laser has been patented (European Patent: EP1677396B1) and is in a good way to be commercialized soon. In the following results will be summarized for both tapered laser structures.

(a) BH-DFB-Laser with integrated *passive* optical taper section

This structure consists of separate laser and a passive integrated taper section. Optical coupling of the laser light into the passive part is realized using an integrated twin guide (ITG) design with a common n-InGaAsP-waveguide layer in both sections to avoid additional selective epitaxial regrowth. The taper function is implemented by laterally narrowing the InGaAsP-waveguide layer towards the front facet. The length of the DFB-section was 300 µm, and that of the adjacent taper section 200 µm. Fig. 20 schematically shows the cross-sectional layer structure, and a top view of a fabricated chip.

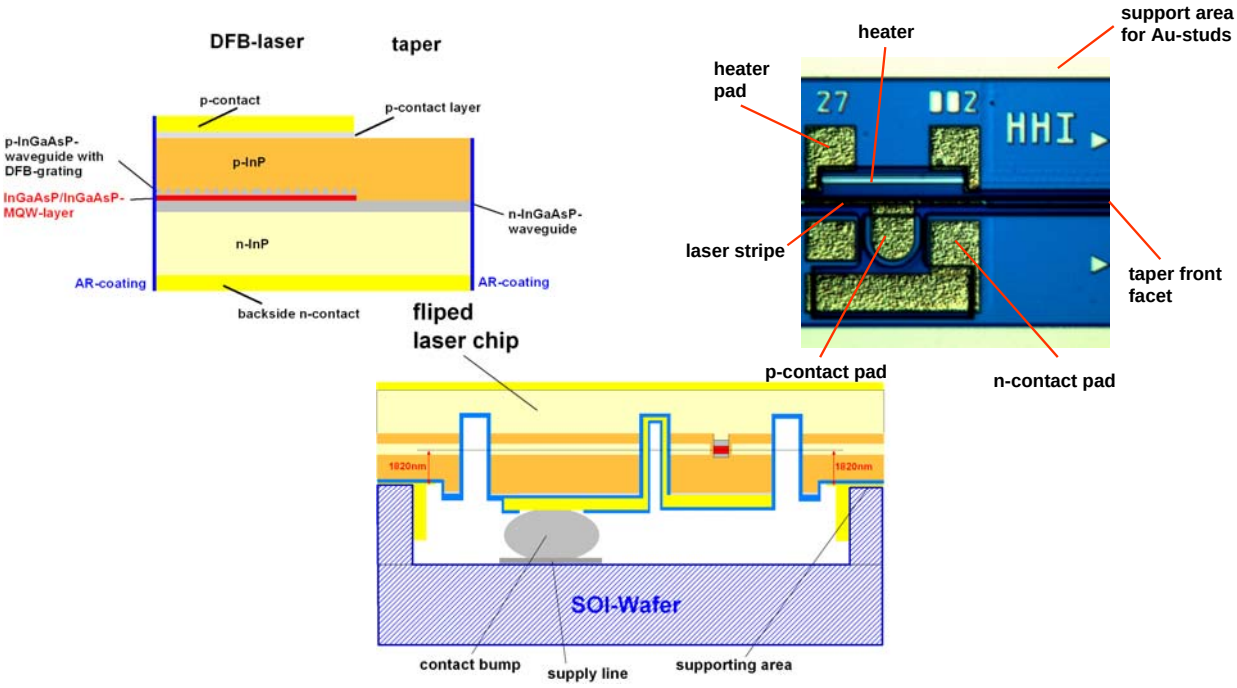


Fig. 20: BH-DFB laser diode with integrated passive taper section: cross-section of layer structure (top left); top view of fabricatzed chip; and flip-chip mounting scheme (bottom)

In order to enable a flip-chip mounting all contact pads, including the strip heater, were formed on the chip surface. With the intended “on-SOI board” assembly scheme the laser chip was to rest on support areas to enable precise vertical alignment to the SOI waveguide. To laterally centre the laser chip during the flip-chip mounting process with the help of mechanical guiding structures cylindrically shaped Au-studs were incorporated at each corner of the laser chip (fig. 20, bottom). The p-contact pad is connected via a suitable solder bump to the underlying electrical supply lines.

In fig. 21 typical static characteristics are represented. Room temperature threshold current is as low as 6 mA, and side-mode suppression ratio of even more than 50dB was achieved. Depending on the width of the taper end FWHM farfield angles could be adjusted between 11° and 24° meeting the afore-mentioned target values, though some ripple pattern were to be noticed on the far-field curves, seemingly associated with the integrated taper structure. Regarding the high-frequency behaviour a

- 3 dB modulation bandwidth of 10GHz suitable for 10Gb/s operation was obtained at a total operation current of 35mA whereas at higher currents the modulation bandwidth tended to decrease due to parasitic capacitance attributed to the integrated taper section.

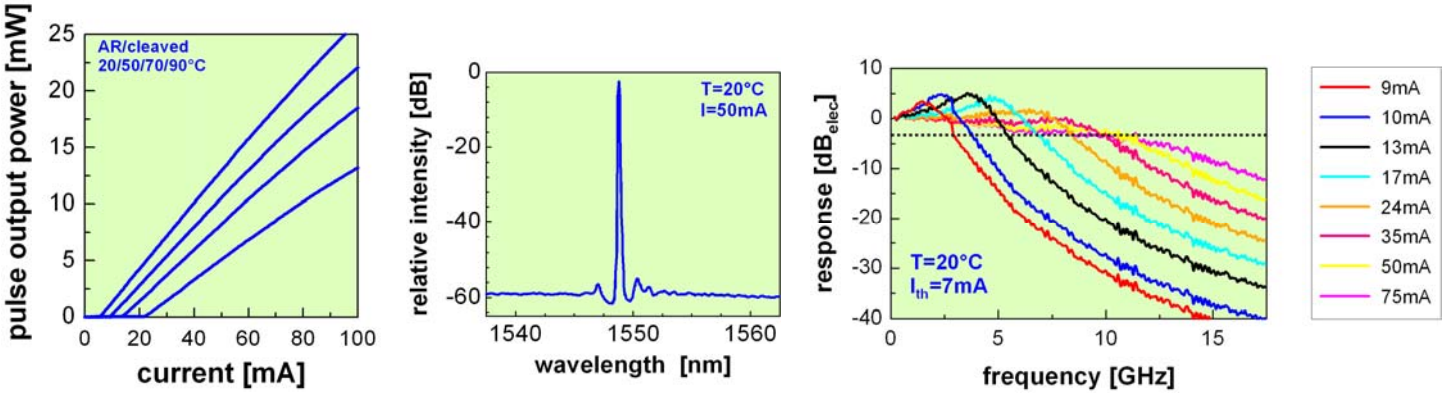


Fig. 21: Optical output power (left); CW-spectrum (middle) and small-signal response (RT, right) of the developed "passive taper" BH-DFB laser device

(b) CSDFB laser diodes

The CSDFB laser was invented and developed alternatively to the above tapered laser device. Apart from providing spot size conversion, however, this type of laser was found to exhibit additional key performance advantages making it the predominant choice, not only for integration but also for conventional transmitter applications.

The CSDFB laser structure comprises, as an integral part of the laser cavity, a tapered *active* waveguide stripe (Fig. 22). Different from traditional designs this stripe is curved to compensate for the resulting effective refractive index variation along the stripe in conbination with a uniform DFB grating. As a consequence the front facet is tilted causing the output beam to exit the laser chip at an angle of some 30° but largely facilitates AR coating. As regards fabrication no additional or modified processing steps are needed compared to state-of-the-art DFB devices.

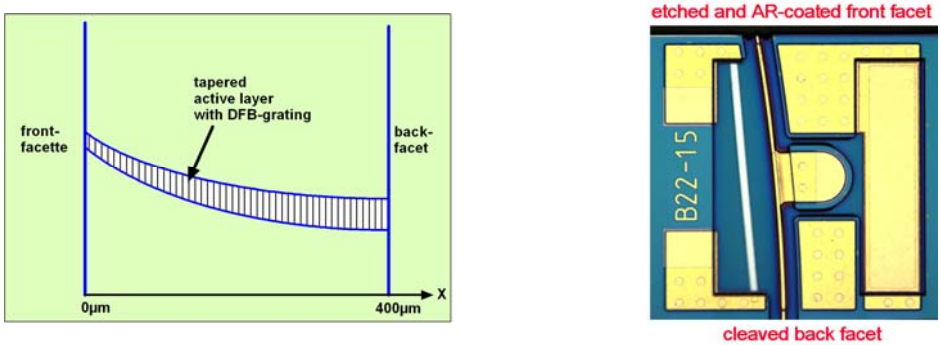
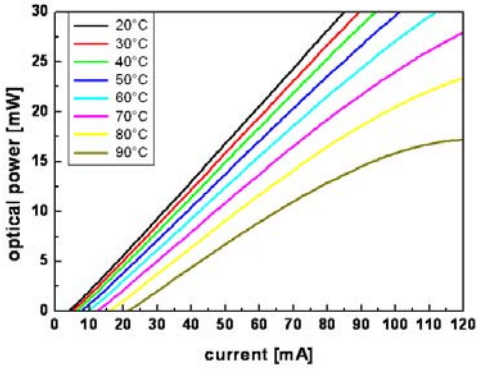


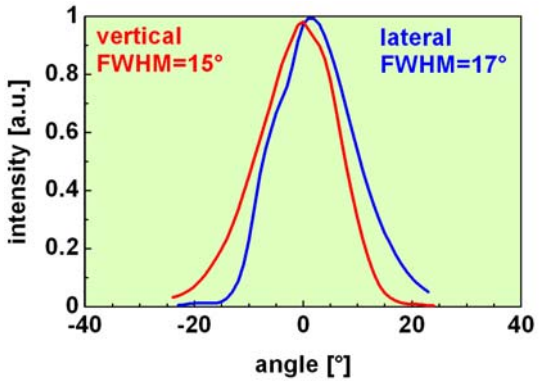
Fig. 22: Schematic layout of the CSDFB laser (left) and top view of a fabricated chip with strip heater (white line) left of the curved laser stripe

In addition to the intended implementation of the taper function the CSDFB laser features the following outstanding properties:

- high single-mode yield (90%) even without any facet coating and without applying a phase shift in the DFB grating, and simultaneously
- high optical output power/ high slope efficiency (> 0.3 W/A) even with as-cleaved back facet (no HR coating)
- high single mode stability over the full operation temperature range from – 40C to +85C
- uncooled 10 Gb/s capability
- superior immunity against optical feedback

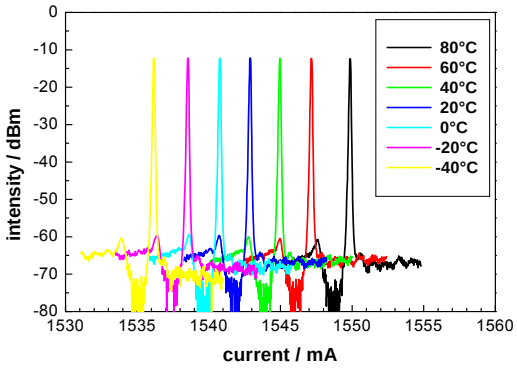
Representative static characteristics are shown in the following figures (a)-(d) illustrating the afore-mentioned features:

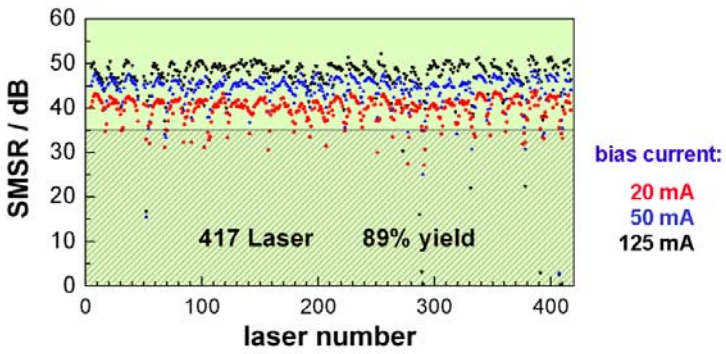




(a) Temperature dependent P-I curves
20°C slope efficiency: 0.38 W/A;
etched AR coated front facet; backside as-cleaved

(b) Optical far-field patterns





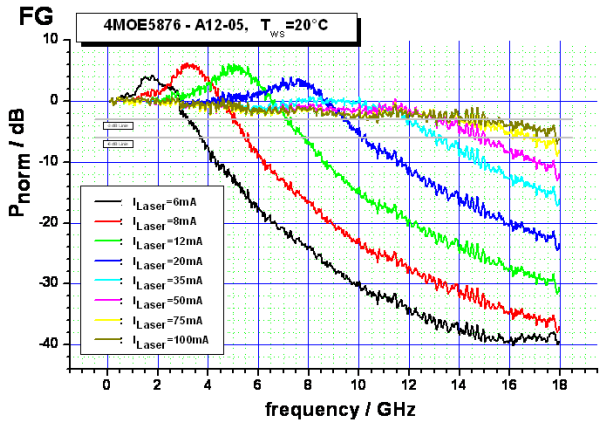
(c) Stable single-mode behaviour from – 40°C to +80°C

(d) Some 90% single-mode yield (SMSR > 35 dB) measured on as-cleaved CSDFB device

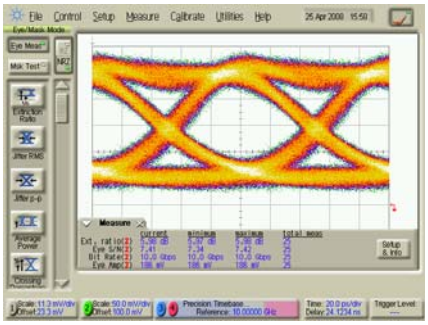
Fig. 23 (a-d): Summary of static characteristics of CSDFB laser diodes developed in Mephisto

Fig. 24 gives results of the high-frequency performance and of the optical feedback behaviour, respectively. The devices exhibit a maximum -3dB modulation bandwidth of about 15 GHz at 20°C and 9 GHz at 90°C rendering them well suited for 10Gb/s modulation. This is evidenced by the displayed 10 Gb/s eye diagram taken at 90°C. The optical feedback sensitivity was evaluated using

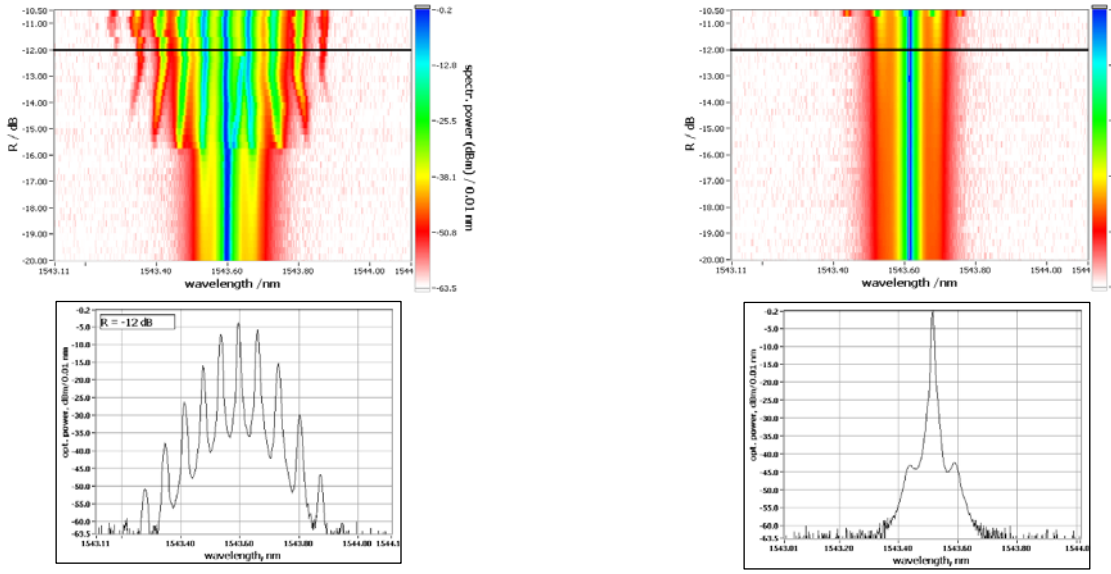
standardized measurement conditions. Both static and dynamic (10 Gb/s OMA) measurements were performed. The devices were operated at 50mA and 0dBm optical power was coupled into an optical fibre. Compared to ordinary BH-DFB lasers of otherwise similar design the CSDFB devices haven proven to be distinctly superior.



(a) Small signal high-frequency response at 20° (indicated currents incl. of threshold current)



(b) 10 Gb/s Eye diagram at 90°C (EYE 10Gb_s DC_55mA Data_0.80V Temp 90°C BER_3E-13 -15dBm)



(c) Optical feedback measurements indicating feedback threshold of the CSDFB device to be higher by 4-5 dB as compared to a BH-DFB laser with traditional design. Measurements were made in accordance with IEEE Standard 802.3ae™-2002.

Fig, 24 (a)-(c): High-frequency and optical feedback behaviour of CSDFB devices

Due to unavoidable fabrication tolerances the emission wavelength of CSDFB-lasers on a wafer varies in the range of +-0.5nm at best. For covering a wider range of channels the wavelength was intentionally varied across the wafer for further selection. In order to be able to finely adjust the

emission wavelength to match with the wavelength channels of the AWG multiplexer a metal strip heater was implemented on the chip (see fig. 22) for thermo-optical tuning. As demonstrated in fig. 25 the tuning efficiency was 1.24 nm per 100 mW of electrical heater power, hence tuning between two adjacent 200 GHz (1.6 nm) channels can be achieved with 130 mW.

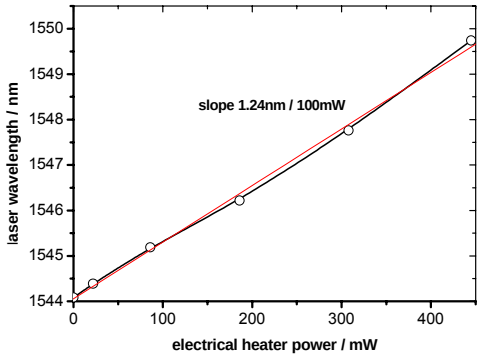


Fig. 25: Thermo-optical wavelength tuning of a CSDFB-LD using a strip heater on the surface of the laser chip

The need for implementing special “mechanical” features in the laser chip arose from the flip-chip based optical butt-coupling of the CSDFB devices to the SOI AWG wavelength multiplexers. Not only pad openings in the passivating SiNx surface layer were to be provided matching to the flip-chip solder bumps on the silicon optical bench, but more demanding the position of the front facet needed to be very precisely adjusted relative to these patterns. Since this cannot be accomplished by any cleavage process the front facet was defined lithographically and etched by chemically assisted ion beam etching (CAIBE). Subsequently these etched facets were AR coated in a full on-wafer process (fig. 26). Apparently the etched facet did not affect at all the performance of the laser devices.

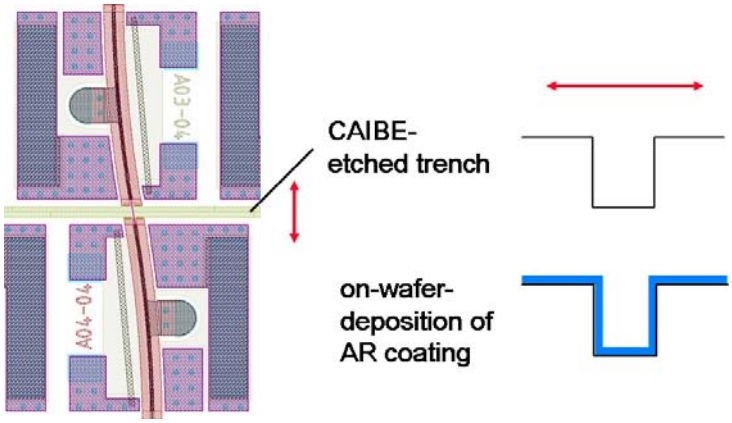


Fig. 26: CAIBE-etching of front facet and subsequent on-wafer AR coating of the facets

4.2.3 Laser driver circuits

To drive the four laser diodes in the planned integrated 4-channel transmitter device laser diode driver (LDD) ICs were developed. These driver circuits not only should be capable of 10 Gb/s modulation but in particular were aimed at providing low output impedance of about 10 Ohm to match the electrical

impedance of the CSDFB laser diodes as good as possible. LDD chips have been available, at least at the time of the project, with 50 Ohm or 25 Ohm output impedance only implying substantial power dissipation and associated heat generation. Optimizing impedance matching without using dedicated resistors was therefore crucial for integration but is of course of large benefit for any laser drive application. In view of the integration scheme pursued in Mephisto the LDD chips had to be furnished with solder bumps for flip-chip mounting. Besides single LDD chips also 4-channel LDD arrays were planned to be developed but had to be abandoned in the course of the project.

The circuit of the 1-channel 10 Gbit/s laser driver IC was designed and laid out in the Freescale 0.35 µm CDR1 BiCMOS technology. The flip-chip capable chip area was about 1.92 mm × 1.6 mm. For the biasing of the laser diode integrated digital controls were implemented initially but an analogue-only bias control design was used in a later run (LDR-V2). T. In order to perform initial on-wafer tests, a laser diode emulator and an on-wafer pad-frame was added to the flip-chip version. The laser diode emulator was constructed by lumped on-chip resistors, MIM capacitors and transistors (Fig. 27a). The simulated behavior is shown in Fig. 27b. The large-signal behavior of the laser diode emulator was optimized to represent the laser diode behavior. The total chip size, including on-wafer pad-frame is approx. 2.3 mm × 2.3 mm. The pad frame of the chip was constructed such that the electrical functionality of the IC can be tested on wafer even with metal bumps already processed. Operation was possible both with positive and negative supply voltages and with a single positive supply voltage, which simplifies the biasing of the circuit. Pre-bias current and the modulation current can be controlled by an analogue current.

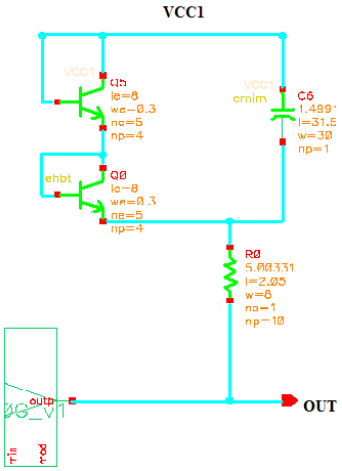


Fig. 27a: Schematic of the laser diode emulator circuitry

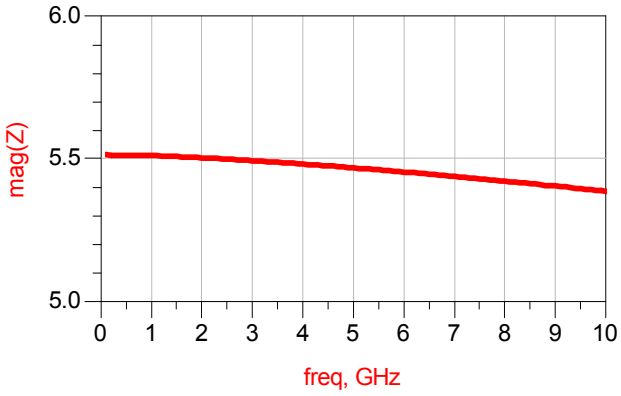


Fig. 27b: Simulated behavior of the laser diode emulator (dummy diode)

The LDD circuit was designed using the Freescale 0.35 µm CDR1 BiCMOS technology. This technology is based on the CDR1 CMOS logic triple-layer metal platform. The BiCMOS process supports up to four levels of AlCu metallization as well as electroplated Cu for inductors. CDR1 BiCMOS is built on P- substrate in support of integrated passives and mixed-mode block-to-block signal isolation. An N+ buried layer followed by a thin epi-silicon growth is used to create NPN, GCPMOS and isolated-well N-channel devices. Tungsten plug technology is used for contact and vias. The metal system is comprised of Ti/TiN/AlCu/Ti/TiN. Stacking of contact and vias is allowed in addition to tolerating unlanded vias and uncovered contacts and vias. Several device process options are available in CDR1 BiCMOS technology. These include isolated-well N-channel MOS transistors

(unilateral, natural, bilateral, standard-Vt and low-Vt), lateral PNP, substrate PNP, P+ sinker isolation and low-resistance substrate contact, and HVCMOS. The HBT (fig. 28) utilizes a SiGe:C base epi layer, which allows higher boron doping for lower base resistance and higher Early voltage, as well as increased RF performance.

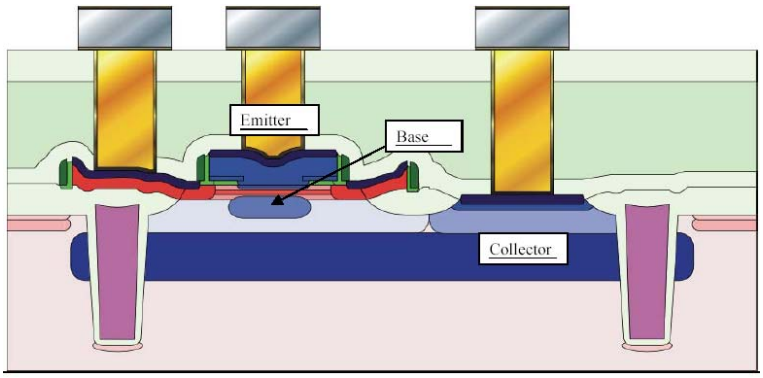


Fig. 28: HBT integration in the CDR1 BiCMOS technology

The carbon doping reduces the base diffusion spreading, allowing the HBT to be more easily integrated into the high thermal-budget BiCMOS flow and permitting a more heavily doped base for very low RB. The HBT device is designed for high fT/fmax at low current, high Early voltage, and 3.3 V BVCE0. The enhanced HBT device (eHBT) is designed for higher fT/fmax (80 GHz/120 GHz), lower noise figure, lower collector resistance, and a nominal 2.5 V BVCE0. Additionally, a higher breakdown voltage enhanced HBT device (eHBT_3p5V) is also available. In the eHBT_3p5V device, peak fT/fmax performance (56 GHz/115 GHz) is balanced with lower collector-base capacitance, high Early voltage, along with low noise figure, low collector resistance, and a nominal 3.6 V BVCE0. Fig. 29 gives a performance comparison of the three different SiGe:C-HBTs.

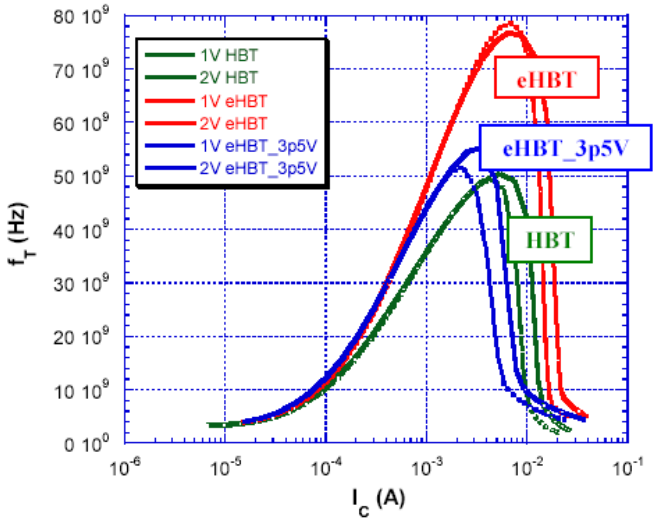


Fig. 29: Comparison of the transit frequency for the three different types of SiGe:C HBT available in the CDR1 BiCMOS technology

Two wafer lots with the LDR-V2 design were fabricated at Freescale applying Cu and SnPb bumps, respectively. Images of respective chips are shown in the following photographs. For further usage in the project wafers were thinned and diced.

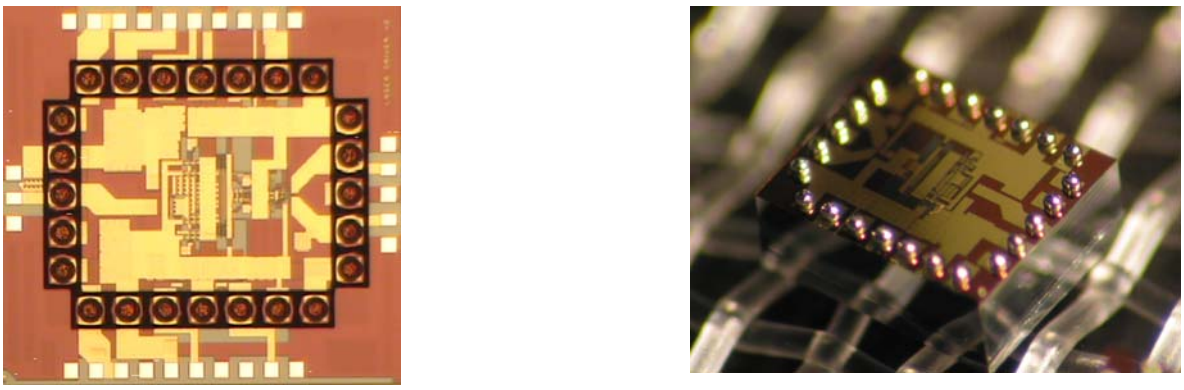
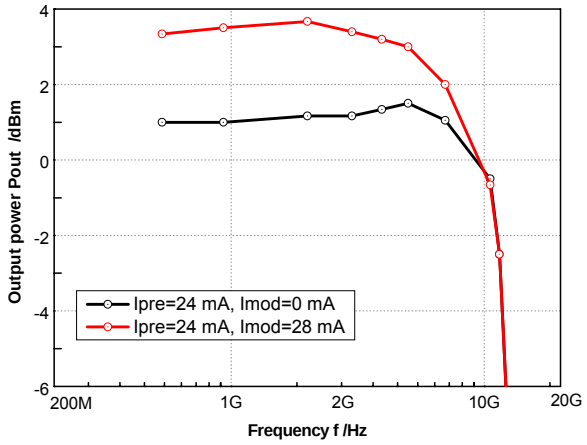


Fig. 30: Laser diode driver ICs with Cu (left) and SnPb bumps (right)

Typical bandwidth measurements of the laser driver IC LDR-V2 performed on-wafer are shown in Fig. 31. Proper functioning was proven up to 12 GHz, with the 3 dB bandwidth amounting to 10 GHz.



Imod (mA)	Vout (Pk-Pk mV)
0	420 - 445
4	455 - 466
8	468 - 476
12	488 - 502
16	505 - 512
20	520 - 532
24	537 - 549
28	544 - 565

Fig. 31: Bandwidth of Laser Diode Driver IC LDR-V2 (left) and measured output voltages at different analogue modulation current settings (right).

To prove the functionality of the modulation current settings, some static measurement have been performed. The peak-peak voltages of the output signal were measured with respect to different analogue control current (Imod). The results are summarized in the table included in fig. 31. The

output voltage variations are in good agreement with simulations and the resolution requirements are fulfilled.

To assess the on-chip thermal distribution, to locate heat spots and to derive the maximum junction temperature of the SiGe-HBTs thermal simulations were conducted taking into account the thermal properties of Si/SiGe material, the flip-chip bump material and electrical power densities of each device. Fig. 32 shows a detailed view of the thermal distribution inside the power amplifier stage of the laser driver IC. For an ambient temperature of 25°C the maximum junction temperature was found to be 43°C, an increase of only 18 K compared the ambient temperature.

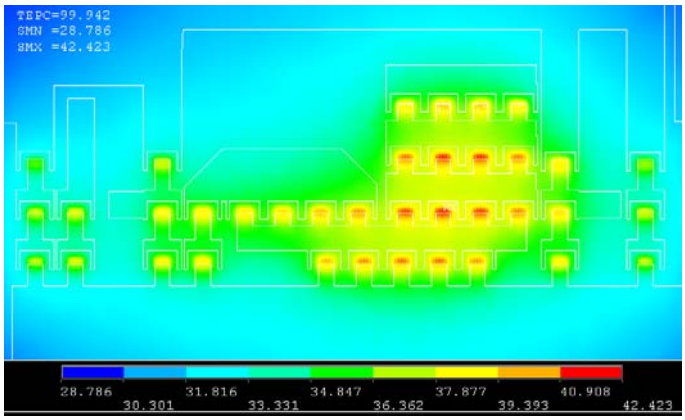


Fig. 32: Results of thermal simulations study on flip-chipped LDD chip. Maximum chip temperature was computed to be 43°C at ambient temperature of 25°C, and thermal resistance junction-to-ambient 25 K/W.

4.2.3 Transmission lines

Electrical high-frequency transmission lines were needed for two purposes: (a) to electrically interconnect the laser diodes and the laser driver chips flip-chipped on the integration board, and (b) to provide the electrical input connections. The main targets were to achieve a low attenuation electrical bandwidth > 7 GHz suitable for supporting 10Gb/s signal transmission, and impedances of 10 Ω and 50 Ω for the interconnections and the input lines, respectively. When this work was started the concept of hybrid integration *onto* a SOI waveguide board was still envisaged which posed large demands on the fabrication of those lines as they had to be placed in deep (some 20 µm) etched trenches. Respective restrictions had to be considered, as well as the impact of the underlying Si substrate material (specific resistivity, space charge layers).

Three types of RF transmission lines, namely a coplanar waveguide (CPW), a coplanar stripline (CPS), and a coplanar stripline with a floating metal (CPF) were designed, fabricated and evaluated. CPS lines appear to be suitable for the implementation of transmission lines of relatively high characteristic impedances only. Achieving characteristic impedances below 50 Ω turns out to be rather difficult since it would require such narrow slots that are very hard to fabricate, particularly on deeply structured wafers. Furthermore, in order to decrease the detrimental effect on attenuation of a low-resistivity induced charge layer at the Si surface the oxide layer should be removed from the slot region. Again, this measure is rather impractical with very narrow slots. If the presence or the impact

of the low-resistivity induced charge layer can be eliminated, the CPS attenuation can however be lower than that of CPF lines.

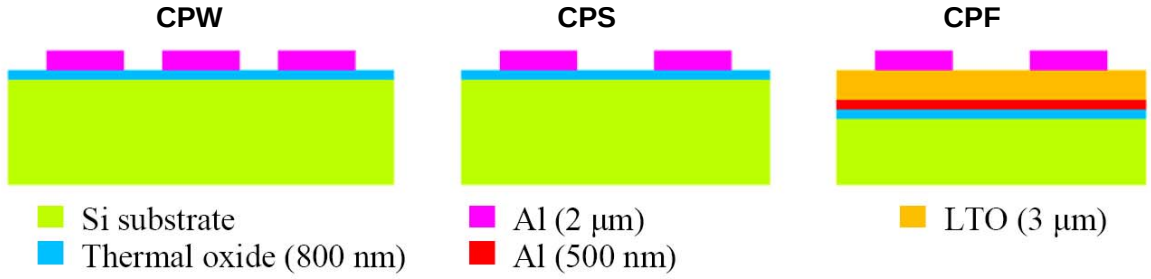
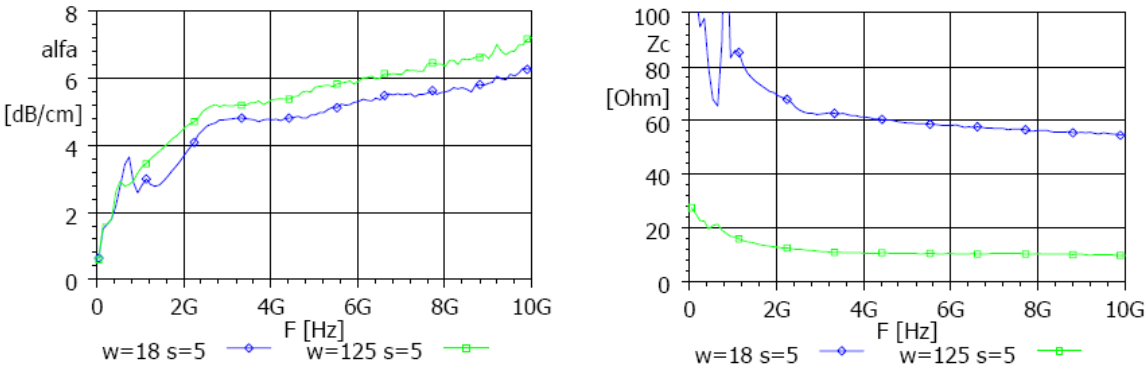


Fig. 33: Cross-sections of CPW, CPS and CPF transmission line structures

CPF lines are favourable for reaching low characteristic impedance. The properties of CPF lines are virtually independent of the substrate resistivity. The attenuation is essentially determined by the thickness of the intermetal dielectric between the floating plane and the coplanar lines, and decreases with increasing oxide thickness. A distinct advantage of CPFs is the insensitivity of the propagation characteristics to the slot width. Therefore, CPF lines allow for more relaxed fabrication tolerances (namely lithography) thus overcoming issues in conjunction with an unfavourable substrate topography. The attenuation of the CPF input line was measured to be in the range of 6 dB/cm @ 7 GHz). With slot widths below 40 µm the characteristic impedance approaches the 10 Ω target, slightly dependent on the stripe width (fig. 34)

The CPW configuration was considered for the 50 Ω input transmission lines only. To realize low attenuation CPW transmission lines the specific resistivity of the silicon substrate needs to be sufficiently high. A value of 20 Ωcm results in > 10 dB/cm attenuation. To allow to utilize also lower resistivity substrates CPF lines were employed for the input lines as well.



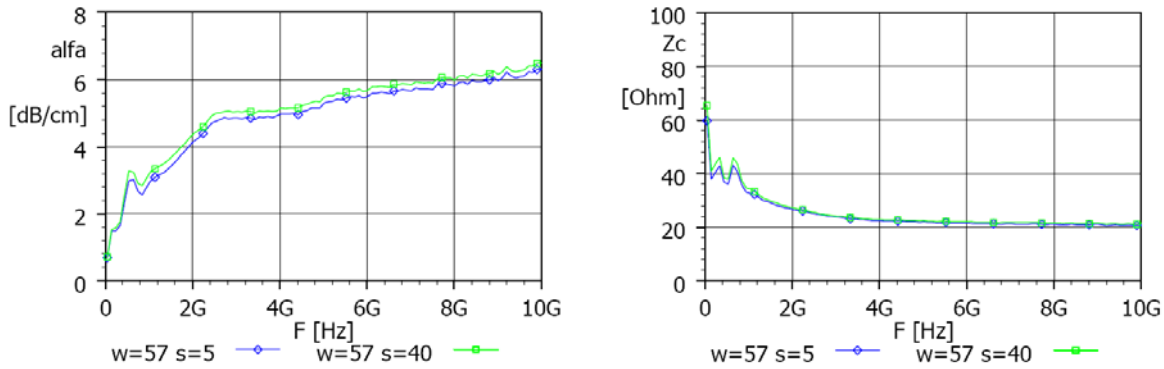


Fig. 34: Measured attenuation constant and characteristic impedance of CPF lines for different stripe slot widths (note: correct slot widths are w=18µm (left) and w=57µm (right))

4.3 Achievements towards hybrid integration

Using the single devices previously described the final goal of Mephisto was to hybridly integrate them by self-aligned flip-chip technology on a silicon optical bench (SiOB). The 4x10 Gb/s transmitter as sketched in fig. 1 served as proof-of concept demonstrator. Whereas, as already outlined in section 3, the initial plan was to perform the hybrid integration on the optical SOI waveguide board, the SiOB concept was followed only since the partner Intexys joined the project bringing in their great expertise in flip-chip processing. In fact the flip-chip based integration task relied essentially on the respective experience and resources of Intexys.

Due to the exceptional conditions partner Intexys was faced with in the later phase of the project (refer to section 4) which finally led to bankruptcy of this company and to the early termination of the Mephisto project the final goal of the project, could unfortunately not be achieved. The individual devices involved were ready for this demonstration. The flip-chip based pairwise integration of laser diodes and SOI waveguides on the one side and of laser diodes and laser drivers on the other side was basically demonstrated but showed insufficient results yet and would have required more iterations. In addition to these experiments thermal simulation studies of the entire device were carried out to assess the thermal conditions of the assembled device since these may potentially seriously affect its performance. Finally, basic studies on hermetic sealing were included to investigate paths of protecting those devices against detrimental environmental effects, particularly moisture.

4.3.1 Silicon optical bench (SiOB)

The SiOB provides the mechanical integration platform for flip-chip assembly including under bump metallization and mechanical pads. In addition the SiOB carries the electrical CPF-type transmission lines the fabrication of which is greatly facilitated since, differently from the SOI board approach, no deep structures are present. In fig. 35 the SiOB cross-section is schematically depicted.

The SiOBs were fabricated on 100 mm Si wafers. A variety of structures were designed not only for implementing the demonstrator with different SOI multiplexer devices but also to provide chips for optical and electrical coupling tests. Fig. 36 presents an overview of the lay-out indicating the different structures.

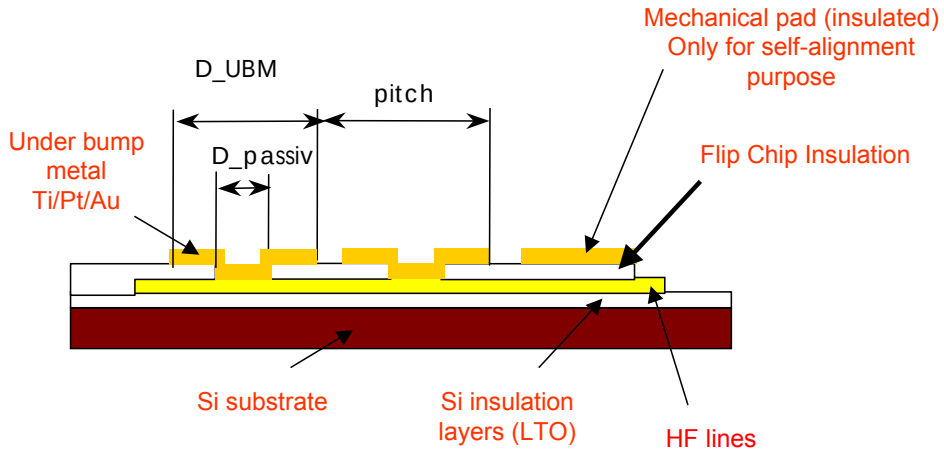


Fig. 35: Schematic cross-section of Si optical bench

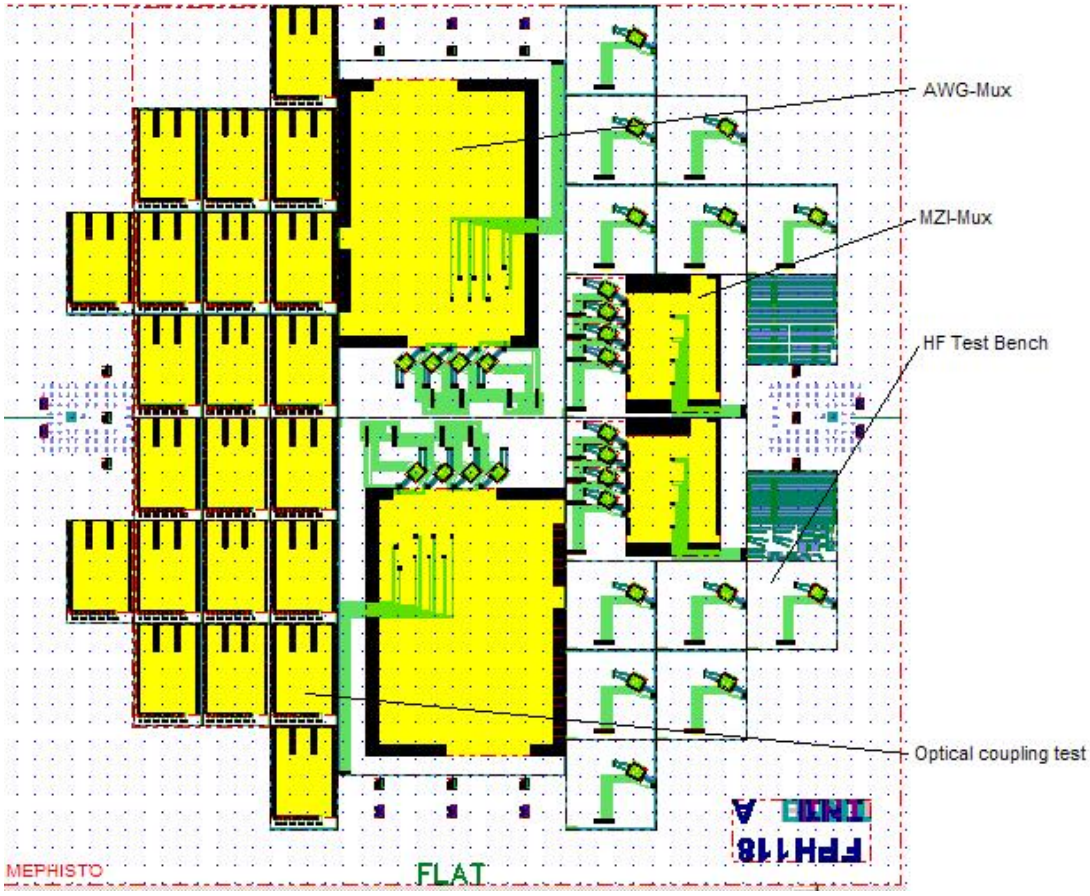


Fig. 36: Layout of a MEPHISTO SiOB wafer (diameter: 100 mm) containing three different types of SiOB chips as indicated

4.3.2 Integration of SOI multiplexer and CSDFB laser devices

The optical coupling of the SOI based MUX+VOA chips with the CSDFB laser diodes was crucial for the success of hybrid integration pursued in the project. The cross-section of the SOI chip is illustrated in fig. 37. An overhang was formed in the SOI material for vertical mechanical alignment purposes by etching a trench from the backside. The facet was indented relative to the chip edge to avoid the risk of damaging the laser output facet due to mechanical contact. A corresponding recess was etched in the laser diode, as shown in the lower part of the figure. Taking into account the tilted beam (some 30° to air) of the CSDFB devices the SOI waveguides had to be angled accordingly. Waveguides with different angles were designed on test chips for experimental evaluation. Fig. 38 shows the lay-out of the SiOB coupling test chip, and a fabricated waveguide. The waveguide fabrication requires a total of three masks, two for the SOI layer patterning and one for the substrate etching.

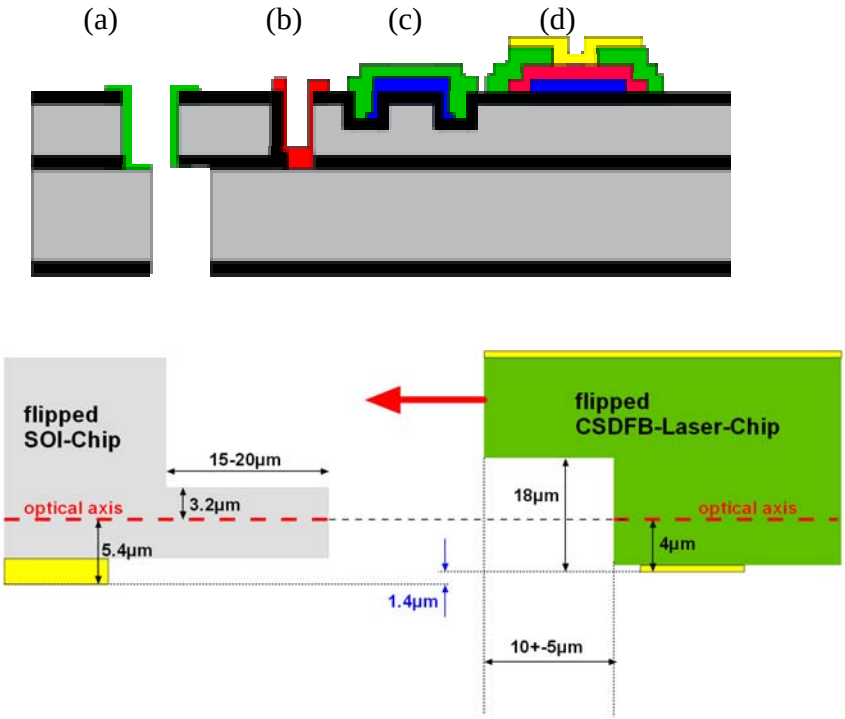


Fig. 37: Target structure for the demo SOI chips. From left to right, the schematic cross-section illustrates the opening of the SOI layer and the substrate for laser coupling (a), a through-etched mirror facet for M-AWG (b), a rib waveguide (c) and the bonding pad (d). The layers at the bonding pad are from top to bottom: Au+TiW (yellow), SiN passivation (green, also as an AR coating), Al (red, also for mirrors) and Mo (blue, also as VOA heater).The lower part shows details of the vertical SOI-laser alignment features.

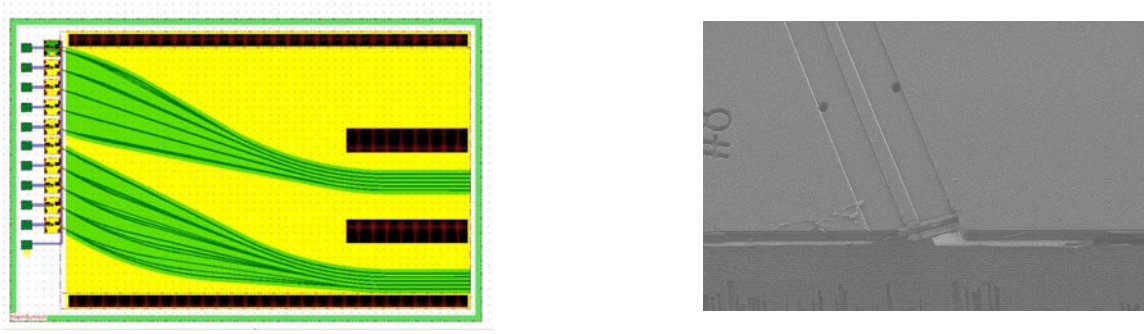


Fig. 38: SiOB coupling test bench (left) and SEM image of fabricated angled SOI waveguide (end facet tilted)

The lay-out of the respective SiOB bench encompassed varying bump diameters and bump offsets to allow for investigating different coupling configurations, and eventually to find out optimum conditions. Indium bumps were used with these test devices for flip-chip mounting although tests with Au/Sn were also in progress.

Fig. 39 shows the power output characteristic and spectrum of a single flip-chipped CSDFB diode. The absence of power saturation even above 30 mW/100 mA power/drive current is indicative of efficient thermal power dissipation via the bumps.

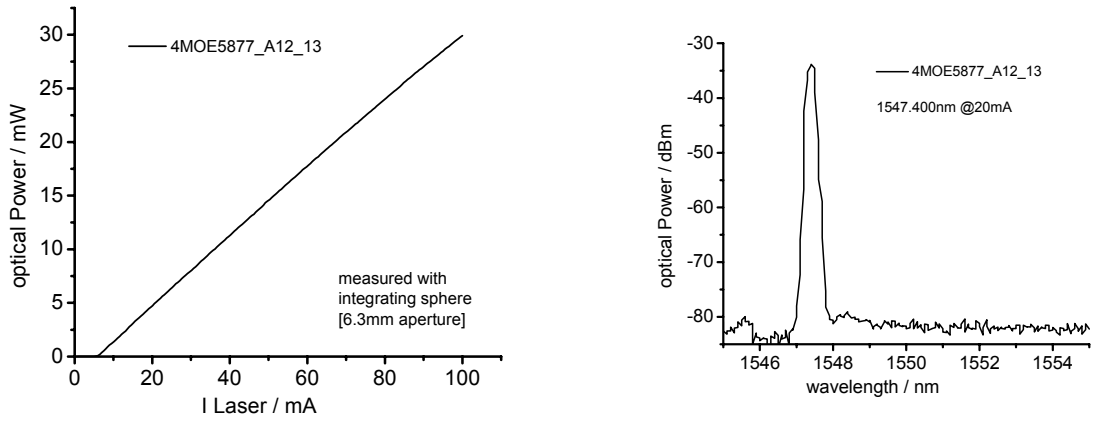


Fig. 39: PI curve and spectrum measured on a single flip-chipped CSDFB laser diode

Co-mounting lasers and SOI optical waveguide chips did not produce successful coupling results with the first runs. It turned out that the relative height of the bonding pads of the SOI and laser chips with respect to their optical axes did not match well. The repeatability of the vertical alignment of the laser chips on top of the SiOB was approximately ±1 µm or worse although an accuracy of ±100 nm was expected in all three dimensions. Based on microscopic analysis there seemed to be significant variations in the size and shape of the In bumps. To remedy these defects different correction measures were started but suffered from the situation with Intexys and couldn't be investigated anymore.

Outside the Mephisto project, partner VTT successfully investigated a thermo-compression (TC) bonding method for vision controlled flip-chip integration of optoelectronic chips directly on the SOI waveguide platform. This concept is similar to Mephisto's original integration concept, except that there are no flip-chip bumps, which significantly simplifies the processing of the chips. Thanks to advances made with respective equipment this technique may eventually emerge as the most straightforward and most economical way for carrying out hybrid integration by co-flip-chipping of optical devices, as introduced in the Mephisto project.

4.3.3 Electrical integration of laser diodes and laser driver chips

Using dedicated test boards implemented on the SiOB wafers CSDFB laser diodes and laser diodes driver (LDD) chips were flip-chip mounted to assess the electrical performance. Bonding the LDD chips was complicated by the different metallisation schemes used for the LDD bumps and the underbump metallisation on the SiOB, the latter consisting of Ti/Pd/Au. Regarding the LDD bumps the

only choices available were Cu and SnPb. No flip-chip processes were established to combine these "incompatible" metallisations. Therefore Intexys spent considerable effort to resolve this issue. Eventually LDD chips could be bonded on the SiOB by using Au stud bumps, though the bonding results were not yet perfect, partially because of the difficult bonding process and partially because of a small layout error made in the SiOB design. For bonding the LD chips Indium bumps were formed on the SiOB.

Fig. 40 shows the lay-out and an assembled chip. The LD chip is indicated by the smaller, and the LDD chip by the larger tilted red area. The big patterns marked in brown colour represent the probe heads. To operate the chip a larger number of signals were required including DC and RF ones. Specially designed probe heads had to be used. Provisions were made to get access to two channels simultaneously bringing the total number of DC and RF connections to 14 and 2, respectively.

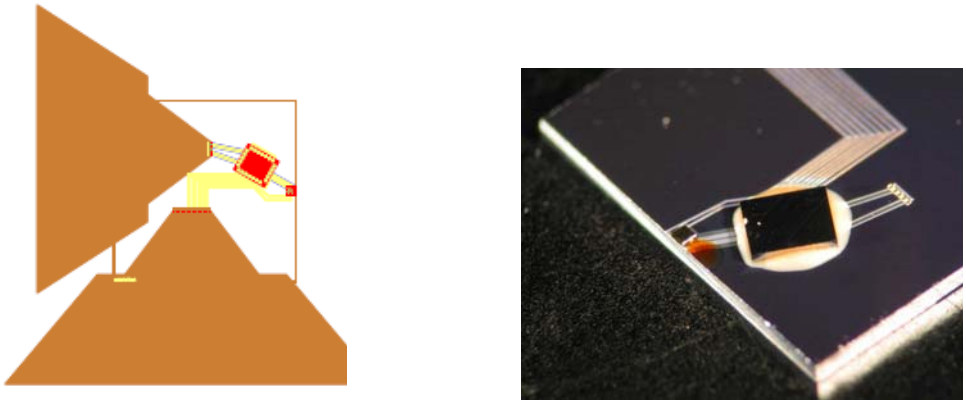


Fig. 40: LDD-LD test chip and measurement arrangement (left); photo image of test chip of 1x1 cm^2 size (right)

Fig. 41 depicts a measured, reasonably well behaved static transfer characteristics (laser output power as function of LDD input voltage). Since some of the bumps were found to be slightly displaced these were likely to have caused poor or maybe no electrical contact varying between the samples. Again, corrections were no more possible, and conclusive data on the proper function of LDD-LD operation are therefore lacking. The measurements suggest however that 10 Gb/s operation will be readily feasible after appropriate corrections.

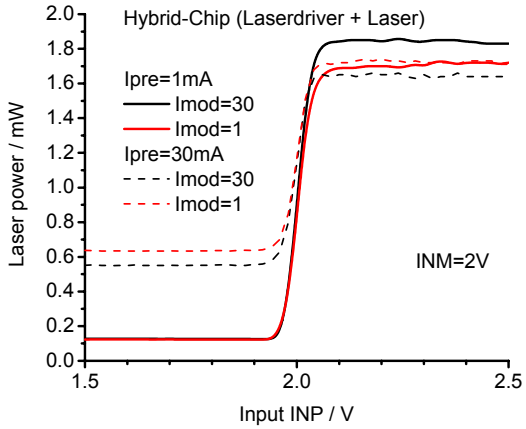


Fig. 41: Results of DC measurement of flip-chipped LDD-LD chip

Despite these deficiencies RF measurements were conducted. Fig. 42 shows a small-signal frequency curve indicating a 3 dB cut-off between 9-10 GHz. This result basically proves 10 Gb/s modulation capability of the flip-chipped LDD-LD combination. The reason for the dip at around 2 GHz remained unclear but may be attributed to the bump alignment issue as well.

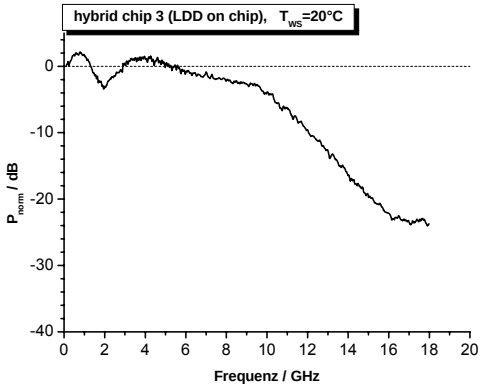


Fig. 42: Small signal RF response of one of the LDD-LD samples

Large-signal measurements carried out at 10 Gb/s revealed still distorted eye patterns with insufficient extinction ratio at 10 Gb/s. A corresponding eye diagram at 2.5 Gb/s is displayed for comparison.

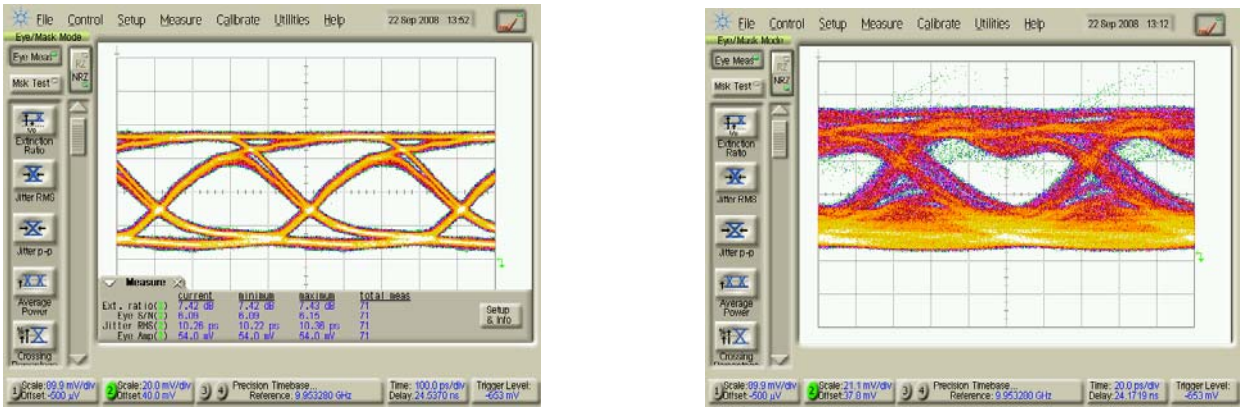


Fig. 43: Measured eye diagrams at 2.5 Gb/s (left) and 10 Gb/s and (right)

4.3.4 Thermal simulation

In the designed Mephisto demonstrator heat is generated by the four laser diode drivers and the four laser diodes flip-chipped on SiOB, as well as by the four thermo-optical heaters that are to control the VOAs on the SOI chip. Heat generated in LDDs and LDs must be effectively conducted to the SiOB substrate to avoid over-heating. Furthermore, the LDs and the AWG require accurate temperature tuning, and even the VOAs are sensitive to temperature gradients. For the laser driver chips alone results have been reported in the previous section already. Here this study was extended to the entire demonstrator device. Steady-state thermal analysis was performed to estimate the temperature distribution and to compare different assembly options (see fig. 44).

Finite element method (FEM) analysis software ANSYS Workbench was used to assemble the 3D model and to carry out the simulations. Simplified 3D-models were created for the laser, driver and AWG-MUX chips, the flip-chip solder bumps and the SiOB. Due to the very large number of flip-chip bumps the detailed models of bump structures were replaced by simplified sub-models having the same height and equal effective thermal conductivity as the detailed models. Demonstrator models were built with and without epoxy underfill. Constant temperature of 25°C was assigned at the bottom surface of the SiOB, and all the other surfaces were assumed to be adiabatic. Typical power dissipations under normal operating conditions of the demonstrator were assigned to the main heat sources of the chips.

According to the simulations the use of underfill reduces the maximum temperature on the demonstrator from 52.6°C to 46.3°C. The simulations show that the mutual heating of the neighbouring laser and driver chips is negligible. Furthermore, the temperature changes on the area of the AWG-MUX chip, which is most sensitive to non-uniform temperature distribution, also appear to be negligible. The designed flip-chip solder bumps apparently provide sufficient thermal connection between the chips and the SiOB.

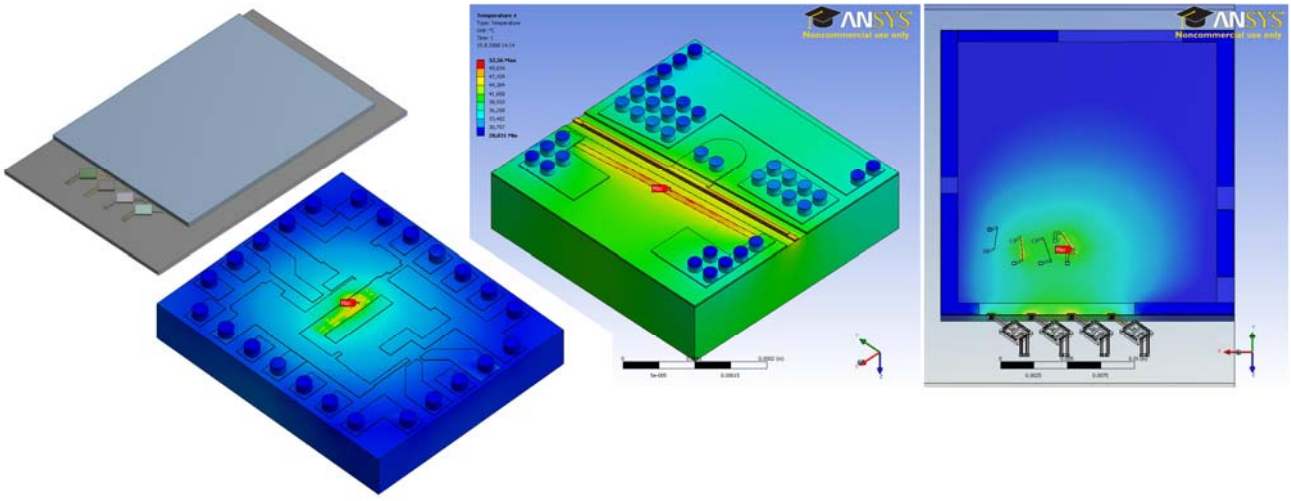


Fig. 44: Thermal simulation of the demonstrator without underfill. From left to right: Overview of the simulated 3D structure, LDD, LD, and AWG-MUX chip.

4.3.5 Hermetic sealing

Hermetic packaging is needed to prevent the moisture from penetrating into the device package and from degrading the device performance. In Mephisto local hermetic sealing was developed primarily as a generic enabling technology for future applications. The effort was focused on sealing technologies that do not inherently require planarisation and on two example applications.

The first application example is a module where laser and driver chips are hybridly integrated on top of an SOI waveguide chip, as originally planned in Mephisto. Both RF lines and SOI waveguides should pass once under the hermetic sealing ring to provide the necessary electrical and optical contacts to the sealed cavity. The second application example involves lasers hybridly integrated on the non-optical SiOB. Here it was assumed that an appropriate method for coupling light out of the hermetic cavity would be separately developed.

Different methods for hermetic packaging were reviewed. Many of the available methods are suitable also for the two application examples considered here. Ideally the packaging method should be

universally useable for a wide range of applications, and it should be independent of preceding process steps and design variations. A safe process, high bonding yield and suitability for industrial production are naturally also preferred. The advantages and disadvantages of methods such as fusion bonding, plasma activated bonding, anodic bonding, eutectic bonding using metal solders (e.g. Au/Si or Au/Sn), thermo-compression bonding, glass frit bonding, epoxy, polymers and adhesives were evaluated.

For the first target application glass frit sealing appeared as the most promising solution, and it was chosen for experimental studies. After the comparison of available glass frit materials and preforms some preforms were procured and used to bond unpatterned glass lids on top of silicon chips. The cavity walls were formed by the sealing glass. Tests were carried out on top of functional SOI rib waveguides (4 µm thick) and 10 Gb/s RF lines, as well as on dummy silicon chips with similar topography. The waveguides and RF lines were covered with oxide layers, which are ideal for glass frit sealing. Sealing was done at normal pressure and atmosphere, while the sealing temperatures and forces were varied. No gross leaks were found for samples sealed with the optimised temperature profile. In fine-leak tests all the samples were within the specified He leak limit, although one sample was exactly at the limit. All the smallest preforms and some of the larger ones also passed the shear strength tests. The measured loss caused by one hermetic sealing seam in a waveguide was 0.2±0.1 dB and almost within the measurement accuracy. Finally, glass frit sealing caused significant performance degradation to the RF lines. This was mainly due to the change of impedance when the glass frit material is positioned on top of the RF line, which causes reflections. This could be explained by simulations (fig. 45), and the reflections can be minimised with proper design.

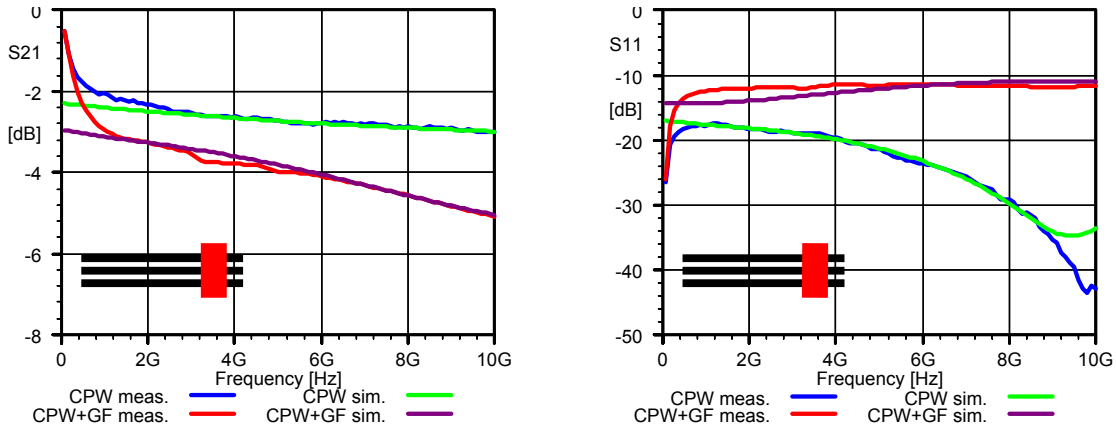


Fig. 45: Measured and simulated insertion (S21) and return (S11) losses of CPW-type RF lines with and without one wide sealing seam.

For the second target application the most promising technology was metal sealing which also supported the commercial goals of project partner Intexys. The metal soldering experiments were carried out using Indium thermo-compression at 125−180°C and Au/Sn fusion at 300−400°C, which represent extreme (low/high) temperatures for metallic sealing. Experiments were done using wafer-to-wafer sealing. Above 156°C the intermetallics between Indium and gold layers form in seconds, but in a few minutes the same result is achieved in as low temperature as 125°C. The success of the thermo-compression process depends on the flatness of the surfaces. When any particles or scratches were avoided a reproducible leakage rate below $<10^{-8}$ tm·cm^3/s was measured.

With Au/Sn soldering a two-step approach was used. First, reflow was applied to reshape the preform or deposited layer into a homogeneous ring. The sealing was done in a second step with the two pieces in contact. The amount of material and the temperature cycles were optimised to get a wetting angle of < 90° and a homogeneous sealing ring. A perfect spherical shape could be obtained under formic acid vapours. The impact of temperature ramps on alignment was also studied.

Finally, some leakage measurements were performed before and after thermal shocks (0°C to 100°C). Whereas some failure caused by the thermal mismatch occurred when Au/Sn was used to seal silicon and quartz no failures were observed for the Indium sealing ring, thanks to its ductile nature.

5. Final remarks

Although the project could not be completed as planned due to exceptional circumstances it has been very substantial in tackling the various issues involved in hybrid integration technology. By pursuing self-aligned flip-chip assembly approach in the later project phase an innovative way of integration was paved. In the future this may be extended to vision controlled flip-chip assembly as substitution for the self-aligned method but with otherwise utilizing the same processes and device structures developed in Mephisto.

The partners will build on these experiences in other European (e.g. FP-7 projects APACHE, BOOM) and national projects where similar technologies as addressed in Mephisto will be applied.

Regarding the commercial exploitation of project results several very promising initiatives are being underway. VTT aims to commercialize the SOI waveguide platform, partially developed in MEPHISTO, with the help of its industrial partners and the Micronova clean room fabrication facility. A spin-off company is currently being set up in Micronova for the commercial production of microsystems .The commercialisation of HHI's proprietary CSDFB laser diode in cooperation with a new start-up company appears to be on a good way. Okmetic's work done in Mephisto has significantly contributed to strengthening the company's competitiveness in the area of SOI materials. The new processes developed helped introduce some 200 SOI products and improved the manufacturability of SOI products with buried cavities. In September 2008 Okmetic made a decision for a major investment to increase wafer capacity.

More details may be found in the following summary description of the dissemination and use plan:

6. Final plan for using and disseminating the knowledge

6.1. Dissemination of knowledge: Publications/presentations

Results achieved in the MEPHISTO have been disseminated mainly via conferences/workshops/publications in journals. A list is given in the following:

1. N. Grote: Presentation of the MEPHISTO project, Photonics Europe, April 28, 2004, Strasbourg

2. N. Grote, M. Moehrle, K. Janiak, J. Kreissl*: Laser Diodes for Hybrid Optical Board Technology,* Proceedings Intern Symp. OPTRO 2005, May 9-12, 2005, Paris; to be published

3. K. Solehmainen, T. Aalto, J. Dekker, M. Kapulainen, and M. Harjanne, P. Heimala: *Development of multi-step processing in silicon-on-insulator for optical waveguide applications*, EOS Topical meeting OPTICAL MICROSYSTEMS, Capri, Italy, September 15-18, Book of Abstracts, p. 111, 2005 (poster)

4. G. Przyrembel, B. Kuhlow, T. Aalto, P. Heimala, K. Solehmainen: *Design and fabrication of AWG based 8-channel DWDM multiplexers on silicon-on-insulator*, EOS Topical meeting OPTICAL MICROSYSTEMS, Capri, Italy, September 15-18, Book of Abstracts, p. 81, 2005 (oral presentation)

5. M. Möhrle, A. Sigmund, A. Suna, L. Mörl, W. Fürst, A. Dounia, W.-D. Molzow: *High Single-Mode Yield, Tapered 1.55 µm DFB Lasers for CWDM Applications*, Proc. ECOC 2005, Glasgow (Scotland), September 25.-29, 2005

6. G. Przyrembel, B. Kuhlow, K. Solehmainen, T. Aalto and P. Heimala: *AWG Based DWDM Multiplexers Combined with Attenuators on SOI,* Proc. ECOC 2006, Cannes (France), September 24.-28, 2006

7. K. Solehmainen, T. Aalto, J. Dekker, M. Kapulainen, M. Harjanne and P. Heimala: *Development of multi-step processing in silicon-on-insulator for optical waveguide applications*, Journal of Optics A: Pure and Applied Optics, vol 8, pp. S455-S460 (2006)

8. M. Möhrle, W. Brinker, L. Mörl, A. Sigmund and N. Grote: *Low-cost, enhanced performance DFB Lasers*, SPIE/EPIC Workshop on Photonic Components for Broadband Communication, 28-29 June 2006, Stockholm, Sweden, Proc. of SPIE, Vol.6350, 63500P1-6

9. S. Bernabé: *Advanced packaging concepts for low-cost optoelectronic devices*, SPIE/EPIC Workshop on Photonic Components for Broadband Communication, 28-29 June 2006, Stockholm, Sweden, Proc. of SPIE, Vol.6350-8

10. N. Grote, M. Möhrle, N. Keil, L. Mörl: *Laser Devices for Hybrid Optical Integration,* 4th Sino-German Joint Symposium on Opto- and Microelectronic Devices and Circuits (SODC 2006), Duisburg, Germany, Sept. 3-8, 2006, Symp. Digest, p.127-130

11. L. Mörl, M. Möhrle, W. Brinker, A. Sigmund and N. Grote: *Tapered 1550 nm DFB Lasers with Low Feedback Sensitivity,* Proc. ECOC 2006, Cannes (France), September 24-28, 2006, Vol.1, p.31-32

12. K. Solehmainen, M. Kapulainen, M. Harjanne, and T. Aalto: *Adiabatic and Multimode Interference Couplers on Silicon-on-Insulator*, Photonics Technology Letters vol. 18, No. 21, pp. 2287-2289 (2006),

13. Timo Aalto, Mikko Harjanne, Markku Kapulainen, Kimmo Solehmainen, Päivi Heimala, Mikael Mulot, and Sanna Arpiainen: *Photonic integrated circuits based on silicon waveguides*, 1st International Optence Workshop on Silicon Photonics, 10.11.2006, Mainz, Germany

14. G. Przyrembel, B. Kuhlow, K. Solehmainen, T. Aalto, P. Heimala, *Design and fabrication of arrayed waveguide grating multiplexers on silicon-on-insulator platforms*, Optical Engineering, vol 46, pp. 094602/1-7, 2007

15. M. Möhrle, A. Sigmund, L. Mörl and N. Grote, Modified InP based DFB laser structures, European Semiconductor Laser Workshop 2007 (ESLW 2007), Berlin, September 14-15, 2007

16. T. Aalto: Presentation of the MEPHISTO project in the Concertation meeting - Photonic integrated circuits / integration of photonic technologies, organized by the European Coordination Action OPERA 2015 for EC-funded photonics projects, Brussels, Belgium, Sept 2007, *Hybrid integration of SOI waveguide components, laser diodes and ICs: Challenges and novel device structures*

17. M. Möhrle, A. Sigmund, N. Keil, C. Zawadzki and N. Grote, Laser diodes for hybrid integration, Europ. Semiconductor Laser Workshop ESLW 08, Eindhoven, September 19-20, 2008, abstract booklet p. 12

18. N. Grote, Recent advances in laser diodes for telecom-/datacom applications, Asia-Pacific Optical Communications (APOC 2007), Wuhan (China), November 1-5, 2007

19. T. Aalto, M. Harjanne, M. Kapulainen, S. Ylinen, J. Ollila, V. Vilokkinen, L. Mörl, M. Möhrle, R. Hamelin, *Integration of InP-based optoelectronics with silicon waveguides*, Proceedings of SPIE (invited presentation in Photonics West, San Jose, USA, 24-29 January, 2009), vol 7218, pp. 72180O-72180O-14, 20

6.2 Scientific and commercial exploitation

Due to exceptional circumstances (bankruptcy of a key partner) the MEPHISTO project had to be terminated prematurely and could therefore not be successfully completed. Especially the simultaneous flip-chip based assembly of optical SOI, electronic Si, and InP LD chips to demonstrate a multiplexed 4-channel DWDM transmitter with an aggregated 40 Gb/s transmission rate was not accomplished, and hence exploitation of results related to integration technology is essentially baseless.

Nevertheless, the project as a whole has led to results and achievements that have been and will be exploited by the partners in different ways:

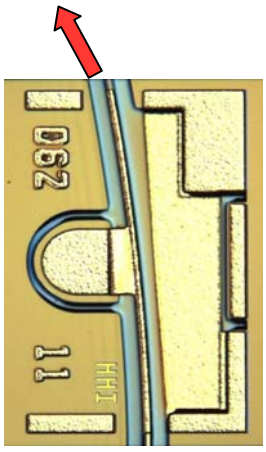
An innovative DFB laser structure (referred to as CSDFB) has been introduced and demonstrated by partner **Fraunhofer-HHI** that simultaneously offers the following advantages:

- low beam divergence
- high slope efficiency
- high single-mode yield even without antireflection facet coating
- high single-mode stability particularly at low operation temperature (down to – 40°C).
- superior feedback sensitivity as compared to conventional DFB designs

In the end these features lead to lower device costs because of high SM yield, potential elimination of an optical isolator, and easier mounting thanks to the taper structure inherently involved. These combined features are highly attractive for any DFB laser application not only in the telecom/datacom arena but also for sensors & instrumentation (e. g. gas analysis) and related applications.

For this invention an European patent (EP1677396B1, January 2007) and a German utility patent (DE 20320771) have been granted.

The CSDFB laser has been and is being used by HHI as a key device in various national R&D projects (COMAN, Berlin Access, TOSA, MiniWDM) in which HHI is participating in collaboration with different industrial partners to target marketable products. In particular, HHI is now using this device as the preferred laser source in the frame of their polymer PLC based hybrid integration technology.



HHI's patented DFB laser diode

CSDFB samples have been provided to different companies for testing. One of those companies has found this laser to exhibit excellent properties for analogue transmitter applications as well, and considers its use in respective products.

Recently, HHI has entered into a business partnership with a newly founded US-German company. Among the components to be marketed is the CSDFB laser aiming at 1490 nm, 2.5 Gb/s PON applications with a potential demand in the multi-million range. Currently TO packaging is being adapted, and device samples are to be shipped shortly to potential customers for testing purposes.

The experience and results achieved in the project are a profound basis and of great value for the FP-7 projects APACHE and Boom in which HHI is participating.

Together with some other projects carried out in parallel, the MEPHISTO project supported **VTT** in the development of a generic technology platform based on SOI waveguides. The SOI waveguide processes developed in MEPHISTO have been used as a basis for other projects that have involved the European space agency as well as several European companies. These projects would not have been possible without the Mephisto project.

The exploitable knowledge consists of design expertise (incl. in-house mask design software), fabrication expertise (incl. clean room process recipies), and characterisation expertise. The elementary building blocks of the platform that were developed in Mephisto are low-loss single-mode waveguides and the following components based on them: 1xN splitters, NxN couplers, and thermo-optical phase modulators. In MEPHISTO these were used as parts of more complicated circuit elements, namely AWGs, symmetric and asymmetric MZIs, thermo-optical switches and thermo-optical VOAs. In present and future projects these building blocks can be developed further and used in many more ways. A hybrid integration method similar to that studied in Mephisto was successfully developed by VTT in parallel projects and can be used to assemble optical modules on the SOI platform. VTT aims to commercialise the SOI waveguide platform, partially developed in MEPHISTO, with the help of its industrial partners and the Micronova clean room fabrication facility. A spin-off company is currently being set up in Micronova for the commercial production of microsystems developed at VTT. This company can act as a commercialisation path for any future products that are at least partially based on the R&D work carried out in the MEPHISTO project

Okmetic Oyj was able to develop new techniques and processes with both grinding and polishing, which led to significant SOI active layer uniformity improvement. These new processes helped to introduce some 200 SOI products and improve the manufacturability of SOI products with buried cavities (C-SOI). Process yield improved and production costs were cut down, which improved competitiveness. Due to improved quality market acceptance was good, and with increasing demand Okmetic made a decision in September 2008 to invest 15 M€ to MEMS wafer capacity increase and to certain new processes. Major part of the investment is in SOI production line.

As a summary benefits Okmetic gained from the Mephisto project were:

- enhanced competitiveness in SOI products
- improved quality enabling penetration to new customers and end-products
- 200 mm SOI product introduction
- C-SOI quality improvement and widened design rules
- greatly increased production volumes

Freescale Halbleiter Deutschland GmbH, in MEPHISTO having developed low- impedance SiGe BICMOS based 10Gb/s laser driver circuits, initially intended to enter the emerging 10Gb/s optical communication market but did not see real market opportunities during the recent “down turn” period

of that market. However Freescale might reconsider in case of a strongly growing demand from potential customers for laser driver chips at 10 Gb/s or higher. Licensing could be another option for exploitation.

Intexys Photonics SA having filed bankruptcy in 2008 was meanwhile acquired by the US company Photonera. Nothing is known as to whether the work carried out by Intexys in the MEPHISTO project will be used in one way or another by this company.