SUBTLE

SUB KT LOW ENERGY TRANSISTORS AND SENSORS

Information Society Technologies – IST

Specific Targeted Research Project – STREP

SUBTLE

SUB KT LOW ENERGY TRANSISTORS

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Annual report

Third year activity report

Project coordinator:	Lukas Worschech
Project coordinator organisation:	University of Wuerzburg
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Publishable Executive Summary

0.1 Project summary and objectives

With increasing miniaturization of semiconductor electronics an increasing fraction of the power to the circuit is converted into nondeterministic signals that add to the ambient noise. In commonly used device concepts noise degrades the performance. Interestingly, there are cases where noise, instead of degrading the device performances, can lead to enhanced signal to noise ratios, if principles of Stochastic Resonance (SR) are used. The partners of the present proposal undertake a coordinated effort including groups working on device theory, nanofabrication and device characterization to investigate the feasibility and potential of SR–nanoelectronic semiconductor devices. Using e.g. special FET like devices with tailored internal feedback the nonlinear dynamic transport properties in this regime will be explored for sensing and switching of sub thermal signals with the help of stochastic resonance-like dynamics. Within the proposal several key devices like “residence time detectors” and “electrochemical capacitance feedback transistors” will be realized and investigated for the first time. Concepts of integrated nanoscale circuits with efficient readout schemes, enhanced signal resolution in a noisy environment and stochastic resonance enhanced detection will be tested. By utilizing nonlinear transport in nanosystems the proposal has the potential to open a new window for electronic applications covering stochastic resonance phenomena, sub thermal switching and on chip noise control applications.

It is the main objective of the SUBTLE project to evaluate the potential of nanoelectronic SR devices by physics and device modeling, nanodevice fabrication techniques as well as static and dynamic device characterization. The scientific approach of SUBTLE is based on the application of two effects in miniaturized electronics, which one usually tries to avoid in device design: back-action of the channel on the gate and noise induced switching. In order to make use of them and even to obtain signal gain, we will realize new types of transistors and circuits, which should allow exploiting noise enhanced switching by means of stochastic resonance phenomena (SR) and device intrinsic capacitance couplings associated with the electrochemical capacitance (EC) of low dimensional systems[1]. Recently proposed detection schemes will be applied in nanoelectronic semiconductor devices[2]. In particular, three key properties will be addressed within the frame of the project:

- Subthermal signal resolution
- Noise activated switching
- Noise enhanced signal processing

The goal of the project includes the realization of three nanoelectronic key devices, which are based on SR and EC for enhanced switching in order to resolve sub thermal signals hidden by thermal noise if classical amplification schemes are applied:

- Electrochemical capacitance induced feedback transistors (FBFETs)
- Noise activated nonlinear devices (NADs)
- Noise enhanced signal processing nodes (NESNs)

These devices will be realized on the basis of high resolution nanofabrication and low dimensional, high mobility carrier systems aligned either vertically or laterally in GaAs and Si based semiconductor heterostructures.

0.2 Work performed in year 3

0.2.1 Major achievements

Major progress was made in all tasks according to our work plan. However, the following achievements should be highlighted:

- Light-controlled morph gates and noise enhanced as well as noise induced universal logic gates as an artificial neuron node was realized (UWUERZ, UNIPG, VTT)
- Submicron Resonant Tunneling diodes were implemented on light detection with a minimum detectability of a Signal-to-Noise Ratio (SNR) of just 0.001 (UWUERZ, UNIPG)
- Demonstration of 150 MHz pattern generator (XENOS)
- Demonstration of mesoscopic capacitors operating as an ideal detector with a Heisenberg efficiency of one (UNIGE)
- We have investigated extensions of the fluctuation-dissipation theorem to non-equilibrium transport and derived relations (UNIGE)
- Realization of magnetic-field asymmetry of nonlinear transport in narrow channels with asymmetric hybrid confinement (UWUERZ, UNIGE)
- Device limits on noise-activated nonlinear detectors (NANDs) have been tested as electro-magnetic sensors. Within a nonlinear stochastic resonance process ultra small Signal-to-Noise Ratios (SNRs) have been detected. (UNIPG, UWUERZ)
- Demonstration of coupled quantum dot FETs (LU)
- Submicron Resonant Tunneling Diodes (RTDs) have been realized as universal and reconfigurable logic gates in a artificial neuron node (UWUERZ, UNIPG, VTT)
- Demonstration of power gain in three-terminal junctions up to 1.5GHz. (UWUERZ)
- Realization of memory diodes based on HfO_2-InGaAs/InP (LU)
- Demonstration and exploration on coupled electron and hole transport in a single 22 nm-thick double-gated Si quantum well (VTT)
- Exploration on the bistable effect in electron-hole (EH) bilayer system as a function external gate biases, drive voltage and temperature (VTT)
- Demonstration on three-terminal ballistic junctions on silicon on insulator wafers (LU)

0.2.2 Plan for use and dissemination of the knowledge

In the third year, main efforts of the project were dedicated to optimize the devices and structures, developed in the framework of SUBTLE during year 1 and 2. The main focus hereby was to put on their relevance for possible future applications. Also the modeling of the internal physical processes was a field of intense efforts. In both strategic directions, experimental work and basic theoretical understanding, the state of the art was pushed significantly forwards. Therefore, the knowledge management was obliged to find a balance between the protection of intellectual property and dissemination of results via publication in journals, conference presentations, PhD thesis and other public domain routes.

Dissemination of results

A significant diffusion of the SUBTLE work has been realized via the SUBTLE website where the number of visitors is increased steadily during the third year to an average of 500 unique visitors per month. Specific attention has also been devoted to the dissemination of results toward specific groups. We have targeted the physics students with a number of introductory seminars in different places. As an example we mention UNIPG, that has organized a set of “lunch seminars” called “A pranzo con la Fisica” and opened to the participation of both undergratuated and graduated students. A total of 7 seminars have been realized with a participation of more than 400 students/researchers. To the large publich we have devoted few initiatives in the mass media like interviews at public radios and magazines (L. Gammaitoni has been interviewed by Radio24, see http://www.nipslab.org/files/file/090510-moebius-cut.mp3 and by “"IL" Intelligence in Lifestyle on the September 2009 issue”, see http://www.ilsole24ore.com/dossier/Tempo%20libero%20e%20Cultura/IL/). All partners of the consortium were very active in dissemination of their results in high ranked scientific journals as well as in the participation of conferences. This is also demonstrated by a large number of invited talks and tutorials at major conferences and workshops (see also deliverable report 6.3).

Exploitation activities

For the commercial exploitation of the new high speed SUBTLE pattern controller, first contacts have been initiated. Especially tool supplier for applications that need to process large exposure areas show interest in a high speed direct write tool. Meetings with possible customers have already taken place (but may not be further disclosed here due to NDA bindings). As well, solutions for high speed electron optic columns have been investigated. Here, especially columns with electrostatic deflection systems are suitable to support the high writing speed of the new pattern controller. Contacts to 3 companies have been initiated or expanded: Hitachi High Technology HHT, A&D and Novelx.
Based on the patent of the SUBTLE sensor (WO/2009/106595), already different industrial partners were contact for exploitation of different applications.

0.3 Consortium details

Consortium

No	Participating Institution	Short Name	Country
1	Julius Maximilians Universität Würzburg	UWUERZ	Germany
2	Technical Research Centre Finland	VTT	Finland
3	Lund University	LU	Sweden
4	University of Geneva	UNIGE	Switzerland
5	Dipartimento di Fisica Universita degli Studi Perugia	UNIPG	Italy
6	XENOS Semiconductor Technologies GmbH	XENOS	Germany

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Project Web-site: http://subtle.fisica.unipg.it/SUBTLE

Project Logo: SUBTLE
SUB KT LOW ENERGY TRANSISTORS AND SENSORS

We held 4 meetings during year 3:

- in Brussels, Belgium, December, 11th - 12th 2008
- in Malta, February 5th - 6th 2009
- in Perugia, Italy, Mai 11th - 12th 2009
- in Wuerzburg, Germany September 21st – 22nd 2009

Section 1- Project Objectives and Major Achievements During the Reporting Period

1. Overview of objectives and state-of-the-art

1.1 Project objectives

Small signal to noise ratios in nanoelectronic circuits limit the signal processing capabilities if deterministic and stochastic signals are amplified none selectively and equally. On the other hand, coupling schemes of nonlinear dynamical systems summarized as **stochastic resonance** (SR) have received a lot of attention as a novel approach to improve the signal resolution at low switching voltages. The goal of the proposed work is to realize nanoelectronic devices exploiting noise enhanced switching and to introduce sub thermal signal resolution in nanoelectronic circuits.

It is the main objective of the SUBTLE proposal to evaluate the potential of nanoelectronic SR devices by a coordinated effort of leading European groups including physics and device modeling, nanodevice fabrication techniques as well as static and dynamic device characterization. The scientific approach of SUBTLE is based on the application of two effects in miniaturized electronics, which one usually tries to avoid in device design: back-action of the channel on the gate and noise induced switching. In order to make use of them and even to obtain signal gain, we will realize new types of transistors and circuits, which should allow exploiting noise enhanced switching by means of stochastic resonance phenomena (SR) and device intrinsic capacitance couplings associated with the electrochemical capacitance (EC) of low dimensional systems. The proposal includes the realization of a number of nanoelectronic key devices, which are based on SR and EC for enhanced switching in order to resolve sub thermal signals hidden by thermal noise if classical amplification schemes are applied. The devices are characterized by the following features:

- **they are nonlinear**
- **they take advantage of (ambient) noise instead of trying to avoid it**
- **they can be integrated**

The technological objectives will result in the first implementations of SR in semiconductor nanostructures for switches and sensors. Internal couplings will allow the tuning of nanoelectronic field effect transistors (FETs) controlled by low dimensional gates in such a manner that steep thresholds and bistable switching without external feedback occur. The technology will focus on the realization of nanoelectronic devices in GaAs and Si with on-chip integration of tunable noise sources.

The approaches of the proposal are based on high resolution nanofabrication and use low dimensional, high mobility carrier systems aligned either vertically or laterally in GaAs and Si based semiconductor heterostructures. For subthermal signal sensing and switching the following devices and circuits will be studied experimentally as well as theoretically:

(A) Feedback transistors (FBFETs) with steep threshold and multi-stable EC switching. The FBFET advantages include subthermal thresholds, large scale integration potential and possibility to reduce the number of interconnects.

(B) Combined with on chip noise sources the FBFETs form the basic switching elements to observe SR effects. FB design will be optimized and the maximum signal to noise ratio studied.

(C) Starting from theoretical descriptions of the physics and device characteristics of single SR devices stochastic resonance nodes (SRNs) will be investigated.

(D) Integrated SR nodes will be realized based on interconnected bistable FBFETs. Neuron nodes for sub-thermal signal processing and the potential for self-optimized switching will be studied.

Recently proposed detection schemes will be applied in nanoelectronic semiconductor devices[3,4,5]. In particular, three key properties will be addressed within the frame of the project:

- Subthermal signal resolution
- Noise activated switching
- Noise enhanced signal processing

These properties will be investigated using the following devices and circuits:

- Electrochemical capacitance induced feedback transistors (**FBFETs**)
- Noise activated nonlinear devices (**NADs**)
- Noise enhanced signal processing nodes (**NESNs**)

1.2 Comparison of project objectives with state of the art

A. Electrochemical capacitance induced feedback transistors (FBFET)

A fundamental approach in SUBTLE is to exploit intrinsic feedback in nanoelectronic structures to reach ultra-steep thresholds and bistable switching. These features together with noise are exploited for sensing and switching applications. We have demonstrated within the first years, that such nanoelectronic properties are indeed feasible and even dominating properties for proper designs and layouts of nanojunctions. In the SUBTLE consortium, we studied both fundamental physical effects in this interesting field of nonlinear mesoscopic transport as well as very applied topics. Compared, to feedback effects controlled by external couplings, our devices are very compact.

B. Noise Activated Nonlinear Devices (NADs)

After three years of activity with the SUBTLE project is not an exaggeration to say that the field of Noise Activated Nonlinear Devices has gained a significant reputation both in fundamental and applied research. Within the aim of the project we have developed two brand new concept devices that are now in the process of patenting. These are the magnetic field sensor based on the exploitation of Y – branched nanojunctions and the visible light sensor based on the novel resonant tunneling diode (split RTD) configurations. In both cases the detection principle is based on the monitoring of statistical residence time differences, a phenomenon where the presence of noise plays a fundamental role. An interesting side-outcome of the research conducted within SUBTLE is the general acknowledgement of the positive role of noise also in the raising field of micro energy harvesting. Random vibrations and statistical fluctuations are now investigated as a potential source of energy to power small scale electronic devices. The first results, based on the combination of noise and nonlinearity appear very promising.

C. Noise enhanced signal processing nodes (NESNs)

Starting from the second term we have focussed our attention on the study of a conceptually new class of stochastic logic gates that can represent a significant step toward an increased miniaturization of new signal processing nodes. In line with the objectives defined in the project, in the first period we started to approach the problem of the role of noise in standard logic gates. In the second term we focused on the design of logic gates that can be reliably operated in the presence of a significant amount of noise. Specifically we considered the so-called universal logic gates as a class of potentially interesting devices. In this third period we moved into the design and realization of a new class of noise tolerant universal logic gates. Universal logic gates, as those based on NAND and NOR binary functions, are bistable devices whose single output can switch between two physically distinguishable states as a function of the combinatory logic of two binary inputs. Moreover their functional logic can be combined in order to reproduce all the basic logic operations required in modern computers. We have realized and tested the "split RTD"-based logic gate. We have introduced a novel operating scheme showing that this device can be operated as a universal logic gate with an exceptional robustness in the presence of large amount of noise.

D. Nanotechnology

GaAs bilayers and SR devices:

Bilayers in GaAs were studied in many different groups world wide. For instance, in a tunnel coupled GaAs/AlGaAs electron bilayer system transport measurements of 1D quantum Hall (QH) edge channels with lithographically defined quantum point contacts (QPCs) was performed. However, the electron densities in both systems was varied by a top-gate and Landau level mixing was observed in the QH regime[6].

Si bilayers and SR devices:

Field induced 2D bi-layers in Si have been realized with SiO_2-Si-SiO_2 heterostructures, which have been fabricated utilizing bonded SOI[7] and SIMOX (separation by implanted oxygen) SOI[8]. The goals of this project require separate contacts to both layers. In the case of electron-electron bi-layers this requires buried depletion gates, which complicates device fabrication and may degrade electronic properties of the devices. Utilization of depletion gates can be circumvented by relying on field induced 2D electron-hole system. Previous studies on electron-hole bi-layers have been focused on III-V based systems.[9,10,11,12] In Si-based devices the bi-layer is formed solely by external top and back gates (at high push-pull double-gate bias). The contacts to the electron and hole systems are self-aligned with respect to the top gate by introducing n and p-type dopants to different regions of the SOI film. This kind of structure and a field induced electron-hole bi-layer in 22 nm-thick Si well has been experimentally demonstrated in SUBTLE during the first period (2007). Note that in 2007 a similar device was explored by the NTT-group, but they were not able to demonstrate electron-hole bilayer in the component.[13] Our devices exhibit the desired bilayer and we demonstrated the first 2D electron-hole drag measurement in indirect gap semiconductor within SUBTLE during the second period (2008).[14] The NTT-group was motivated by our work and demonstrated the drag effect in their SIMOX-based system.[15] However, due to the fact that the SIMOX material suffers from relatively strong elastic scattering arising from the implanted buried oxide the NTT-group is limited study relatively thick Si wells (~40 nm). During 2009 we have performed an extensive intra and inter-layer (drag) transport study in our ~20 nm thick system and we discovered novel effects in temperature dependency of the electron-hole drag. Furthermore, we have demonstrated a novel bistable electron-hole gating effect in the bilayer devices. Therefore, we conclude that the Si bilayer goals and also the obtained results are state-of-the-art.

High resolution electron beam lithography:

During the reporting period, no significant improvements for Gaussian beam lithography systems could be noticed. The new commercially available Vistec system reported in the last period has not seen any changes in it's 50 MHz writing speed (Vistec: "Evolution rather than Revolution").[16] Other commercially available systems still are limited to writing speeds in the range of 25 Mhz, e.g the JBX family from JEOL.[17] Work of tool suppliers in this field is still focussing on improvements of shaped beam lithography systems or parallel beam systems for mask writing. First massively parallel writing systems have been delivered a few months ago.[18] The achievable writing speed of 150 MHz (at internal worst case timing level) of our new high speed SUBTLE pattern generator thus still is a factor of 3 ahead of the fastest commercially available single beam Gaussian systems.

1.3 Objectives, work performed and major achievements in year 3

1.3.1 Synthesis of major achievements and fulfillment of recommendations / comments according to the review report N°2

In all tasks scheduled for the third project year, significant progress was made. In particular we want to highlight the following achievements:

- Light-controlled morph gates and noise enhanced as well as noise induced universal logic gates as an artificial neuron node was realized (UWUERZ, UNIPG, VTT)
- Submicron Resonant Tunneling diodes were implemented on light detection with a minimum detectability of a Signal-to-Noise Ratio (SNR) of just 0.001 (UWUERZ, UNIPG)
- Demonstration of 150 MHz pattern generator (XENOS)
- Demonstration of mesoscopic capacitors operating as an ideal detector with a Heisenberg efficiency of one (UNIGE)
- We have investigated extensions of the fluctuation-dissipation theorem to non-equilibrium transport and derived relations (UNIGE)
- Realization of magnetic-field asymmetry of nonlinear transport in narrow channels with asymmetric hybrid confinement (UWUERZ, UNIGE)
- Device limits on noise-activated nonlinear detectors (NANDs) have been tested as electro-magnetic sensors. Within a nonlinear stochastic resonance process ultra small Signal-to-Noise Ratios (SNRs) have been detected. (UNIPG, UWUERZ)
- Demonstration of coupled quantum dot FETs (LU)
- Submicron Resonant Tunneling Diodes (RTDs) have been realized as universal and reconfigurable logic gates in a artificial neuron node (UWUERZ, UNIPG, VTT)
- Demonstration of power gain in three-terminal junctions up to 1.5GHz. (UWUERZ)
- Realization of memory diodes based on HfO_2-InGaAs/InP (LU)
- Demonstration and exploration on coupled electron and hole transport in a single 22 nm-thick double-gated Si quantum well (VTT)
- Exploration on the bistable effect in electron-hole (EH) bilayer system as a function external gate biases, drive voltage and temperature (VTT)
- Demonstration on three-terminal ballistic junctions on silicon on insulator wafers (LU)

Recommendation and comments of the reviewers were considered by following efforts:

- Reviewers asked to consider publication of SUBTLE results in electrical engineering journals and also result dissemination to a broader public.
  - SUBTLE efforts: We submitted several manuscripts to IEEE journals. Some of them are already accepted and published. Reprints are included in report of D6.3. Interviews for public reporting were given. SUBTLE results are reported in journals with a broader readership.
- Reviewers encouraged to consider an increase of collaboration between the two technological nodes:
  - SUBTLE efforts: We combined the III-V resonant tunneling technology with the noise source technology developed in the VTT laboratories, e.g. within logic stochastic resonance. Also light controlled morph gates were found. Measurement techniques were discussed and experiences shared to strengthen the interaction. E.g. to control and test bistable switching by temperature series was first performed with III-V FBFETs and was now also demonstrated in detail with bistable Si switches.
- Reviewers recommend to perform more student exchanges:
  - SUBTLE efforts: A student from UNIPG spent two weeks at UWUERZ and performed experiments together with students from UWUERZ on noise

triggered logic switching. The experimental data was then analyzed and modeled. Worth to mention, an abstract on our SUBTLE ideas published within an international student exchange programme, fascinated students from the USA so much, that we could win a student from MIT to join for several months at UWUERZ the SUBTLE work. A postpod from UNIGE visited the group in LU. During this time, he had the opportunity to visit the laboratories and discussed with the members of the group about their experimental and theoretical work on optical and electronic properties of nanowire devices and spin transport properties and charge detection in quantum dots and gave a seminar on "Correlated transport in capacitively coupled conductors". To model the experimental results on a light controlled logic stochastic resonance a student from UWUERZ was at UNIPG and was introduced into the modeling of nonlinear stochastic resonance modeling. Many results of this efforts are presented in the result section in our reports.

- Interaction with other EU projects was acknowledged and encouraged to be extended.
  - SUBTLE effort: Technological as well as informal interactions between established routes were continued (e.g. Node). Also partners from FACETS (FACETS-ITN) were contacted and exchange of knowledge was initiated.
- The reviewers advised to improve the website of the project.
  - SUBTLE effort: Several tasks in our project website were changed. New. informations were included, projects objectives and results explained, highlights presented. List of papers is now included in the website.

In the following, the objectives, the work performed and the major achievements of each work package are described.

1.3.2 WP1: Theory of electrical switching & sensing

The statistics of large deviations can be derived from a generating function which possesses certain symmetries. These symmetries imply relations between non-linear transport coefficients and higher order noise correlations. These connections are known as fluctuation relations. We propose a test of the simplest fluctuation relation in electrical conductors in close proximity to each other. The charging energy (Coulomb interaction) is sensitive to occupation of states in both conductors and leads to a strong interaction. We examine the generation of currents in a unbiased conductor due to the charge fluctuations in a conductor supporting a current.

1.3.3 WP2: Technologies for subthermal switching devices

Gain with sub-KT resolution and bistable switching in FBFETs were demonstrated. Bistable switching was reached in III-V and Si based technological routes. We also used the technology to implemented contacts, to design narrow contacts to our nanoelectronic transistors. In this way, we have been able to solve a fundamental problem in 2DEG coupled contacts of large coupling capacitors, which usually limits such structures to be operated only at low frequencies. We reached GHz operation with power gain. To strengthen the applied technologies, an objective in this WP was dedicated to the demonstration of the XENOS designed new pattern generator, with the possibility of implementation SUBTLE device designs and ultra-fast writing speeds. This is also demonstrated now.

1.3.4 WP3: EC feedback and single SR devices

Here different types of coupling between nanoelectronic transistors are studied. A major goal in the last year, was to study coupled quantum dots. In addition, we also expanded our studies on last year reported RTD nanostructures as tuneable on chip noise source. A basic goal for application of such kind of amplifiers is to demonstrate both inverted as well as non-inverted switching. This is done with maximum transconductance exceeding the thermal limit of classical transistors.

1.3.5 WP4: SR multiterminal nodes

Here we report on a noise-induced transition of universal logic gates. By counting of signal spikes, an operation strategy usually applied for detectors and known as Geiger mode since its first demonstrated within the famous gold foil experiment in 1909, we demonstrate for signal-to-noise ratios (SNR) smaller than one stable universal gate operation. By decreasing the SNR further, instead of destroying the logic output, noise-controlled morphologic logics of artificial neurons is found, which have the potential to pave the way for artificial logic networks with dynamic functions and noise-regulated logic architectures.

1.3.6 WP5: Sensors & enhanced switching

Two different noise activated nanoscale sensors have been designed, built and tested in this project: the Y-branch magnetic field sensors and the RTD light sensor. In both cases all the work has been successfully performed within the project thanks to a fruitful collaboration among the participating groups. The Y-branch sensor has been the object of a patent activity between UNIPG and UWUERZ. Signal detection tests have been performed on single devices and in networked devices on the presence of different amount of external noises in order to measure the sensor performances.
A novel approach in light detection strategy based on the receiver operating characteristic (ROC) was experimentally and theoretically tested in the two level system of a double barrier resonant tunneling diode. It is shown that within a dynamical Geiger mode analysis counting of noise-activated spike like signal trains lead to a maximum probability of detection. This neuron like sensory action exhibit a maximum probability of detection for Signal-To-Noise Ratios (SNR) much smaller than one. Further investigations even lead to a pronounced probability by decreasing the SNR. This can be associated to a nonlinear stochastic resonance process.

1.4 Summary List of Deliverable and Milestone Reports

All deliverables were submitted in time. Also all milestones were achieved. In the following table the number, title, lead participant and other information of our contractual deliverables are listed.

Del. No.[19]	Deliverable title	Delivery date[20]	Lead participant	Na-ture[21]	Dissemi-nation level[22]	sub-mitted
D1.2	Report on capacitance effects in coupled quantum wires	M30	UNIGE	R	CO	**X**
D1.3	Report on charging and large deviation statistics.	M36	UNIGE	R	CO	**X**
D2.4	Report on 100MHz EBL writing speed: full	M36	XENOS	R	CO	**X**

	integration of the high speed in lithography systems's algorithmus					
D3.3	Report on coupled quantum dot FETs	M36	LU	R	CO	**X**
D4.3	Report on advanced designs of multiterminal SR nodes and scheme of adaptive feedback of on-chip noise generator	M36	VTT	R	CO	**X**
D5.3	Report: Signal detection tests on single and networked prototypes and nanoelectronic SR Sensor	M36	UNIPG	R	CO	**X**
D6.3	Submission of a dissemination and use plan	M12,24,36	UWUERZ	R	CO	**X**
D6.4	Submission of technology implementation plan	M36	UWUERZ	R	CO	**X**
D6.5	Submission of annual technical progress reports	M12,24,36	LU	R	CO	**X**
D6.6	Submission of final project report	M36	UWUERZ	R	CO	**X**

[1] D. Sanchez, M. Büttiker, "Magnetic-field asymmetry of nonlinear mesoscopic transport", Phys. Rev. Lett. 93, 106802 (2004)

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[15] *K. Takashina et al. "Electrons and holes in a 40 nm thick silicon slab at cryogenic temperatures", Appl. Phys. Lett.* ***94****, 142104 (2009).*

[16] *http://www.vistec-semi.com/*

[17] *http://www.jeol.com/PRODUCTS/SemiconductorEquipment/ElectronBeamLithography/tabid/99/Default.aspx*

[18] *http://www.mapperlithography.com/press-en-2009.html#20090721*

[19] *Deliverable numbers in order of delivery dates: D1 - Dn*

[20] *Month in which the deliverables will be available. Month 0 marking the start of the project, and all delivery dates being relative to this start date.*

[21] *Please indicate the nature of the deliverable using one of the following codes:*

- ***R*** *= Report*
- ***P*** *= Prototype*
- ***D*** *= Demonstrator*
- ***O*** *= Other*

[22] *Please indicate the dissemination level using one of the following codes:*

- ***PU*** *= Public*
- ***PP*** *= Restricted to other programme participants (including the Commission Services).*
- ***RE*** *= Restricted to a group specified by the consortium (including the Commission Services).*
- ***CO*** *= Confidential, only for members of the consortium (including the Commission Services).*

1.5 Deviations from Work Programme and Corrective Actions

The project work is according to our work programme.

Section 2- Workpackage progress of the period

2. WP1 - Theory and Modeling

2.1 Objectives and starting point of work at beginning of reporting period

Within the first and second period, all deliverables and milestones were reached. As a consequence, the objectives at the beginning of the third year were defined by our work plan as principle understanding of the role of capacitance and interactions on the large deviation statistics.

2.2 Progress towards objectives

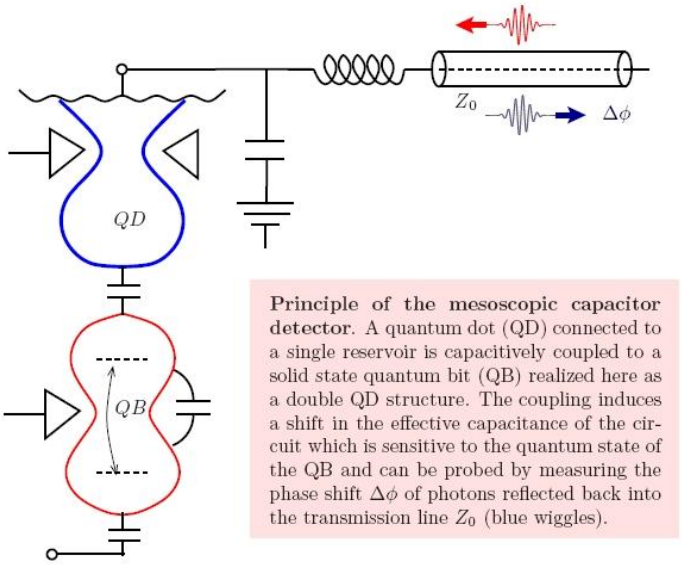
Mesoscopic capacitors can be used as charge detectors. We have discussed the effect of interaction and magnetic field on the rectification properties of two terminal conductors and have been able to connect them to fluctuation properties (noise) of such conductors. We have developed a theory for two-particle effects based on single electron emitters (non-linear capacitors).

2.2.1 Task 1.1 – Models of optimized SR in NADs and NESN

This task was devoted to optimize Stochastic Resonance principles in Nonlinear Noise Activated Detectors (NADs) and (NESN) and has been successfully implemented during the first and second year. Related efforts on this task have been successfully demonstrated in Task T4.4, T5.3 and T5.4.

2.2. 2 Task 1.2 – Modeling of many-body effects in electrochemical capacitance

In the first two years of the project we have investigated the effect of interactions on the properties of small mesoscopic capacitors. In this third year we have investigated the use of a capacitor as a detector of charge. Current mesoscopic experiments use single electron transistors and quantum point contacts for this task. For experiments in GHz range instead of using two or three terminal detector using simply a capacitor might be sufficient. Instead of a dc current, we then measure the phase of a microwave reflected from the capacitor.



Principle of the mesoscopic capacitor detector. A quantum dot (QD) connected to a single reservoir is capacitively coupled to a solid state quantum bit (QB) realized here as a double QD structure. The coupling induces a shift in the effective capacitance of the circuit which is sensitive to the quantum state of the QB and can be probed by measuring the phase shift $\Delta\phi$ of photons reflected back into the transmission line Z_0 (blue wiggles).

Fig. 2-1: Mesoscopic charge detector coupled to a qubit and coupled via a tank circuit (LC) to a transmission line.

The figure of merit of a quantum detector is the Heisenberg efficiency. A bad detector delivers no information and nevertheless dephases the qubit: Its Heisenberg efficiency is zero. A good detector provides a maximum of information and dephases the qubit only as much as demanded by the Heisenberg uncertainty relation: its Heisenberg efficiency is one. In our work [23] we demonstrate that a mesoscopic capacitor can have a Heisenberg efficiency of one: it can be operated as an ideal detector.

2.2.3 Task 1.3 – Role of electrochemical capacitance in non-linear transport

Progress is reported under 2.2.4 and 2.2.5.

2.2.4 Task 1.4 – Modeling of magnetic field symmetry of non-linear transport

In previous work we have shown that a typical mesoscopic sample exhibits a rectification coefficient (second order conductance) that is not even in magnetic field. This prediction has been concerned in many experiments some of them carried within the project SUBTLE (UWUERZ).

Measurement on magnetic-field asymmetry of nonlinear transport in narrow channels

The investigated devices are based on a modulation doped GaAs/AlGaAs heterostructure with a two-dimensional electron gas located 80 nm below the surface. The carrier density and the mobility of the unconstrained 2DEG determined from Hall measurements conducted at 4.2 K in the dark were $n \approx 4 \times 10^{11}\ cm^{-2}$ and $\mu \approx 10^{6}\, cm^{2}/Vs$, respectively. An electron microscope image of the examined structure is shown in Fig. 2-2(a). A 250 nm wide, bend shaped trench cutting through the 2DEG was etched into the structure. Directly adjacent to the trench a 200 nm wide metallic (Cr-Au) gate was evaporated on top of the sample surface. The minimum distance between the metallic top gate and the etched trench is 70 nm. Combinations of etched channels with metallic gates for realization of hybrid confinements in quantum wires were recently also reported by Kothari et al. [24]. By applying a negative voltage V_{tg} to the top gate with the source of the 2DEG serving as common ground, the 2DEG beneath the gate is depleted. In etched quantum wires transmission rates a few

percent smaller than unity were observed and associated with the etched side walls[25]. Metallic gate electrodes, however, are known to cause predominantly specular scattering[26]. As a result of these different gates, two unequal boundaries arise and realise a deterministic inplane asymmetry of the constriction formed between the etched channel and the negatively biased top gate.

We have investigated the two-terminal conductance G of such structures by immersing them into liquid He at a bath temperature of 4.2K. The current I_d through the constriction was determined from the voltage drop at a resistance R = 10 kΩ connected in series to the drain contact. The magnetic field was directed perpendicular to the sample plane. A sketch of the structure and the test setup is show in Fig. 2-2 b). Positively biased, more electrons move from the source to the drain. Thus an electron (green hemisphere) moving towards the constriction is magnetically deflected towards the constriction boundary defined by the top-gate for a magnetic field pointing upwards (blue arrow). As mentioned before, metallic top gates cause dominantly specular scattering. Thus the electron can pass more likely into the drain (blue hemisphere). On the other hand, a reversal of the magnetic field direction (red arrow) would guide the same electron towards the rough boundary edge. Due to backscattering its trajectory is guided back to the source (red hemisphere) which in turn reduces the two-terminal conductance.

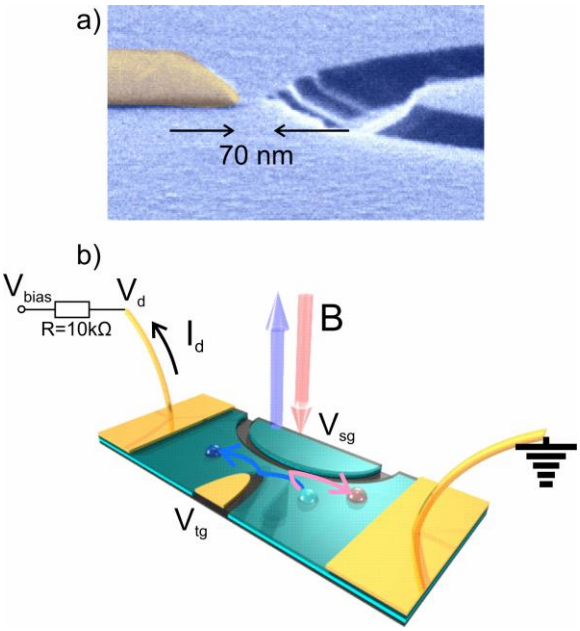


Fig. 2-2: (a) Electron microscope image of the studied asymmetric constriction. One can see on the left side the metal-surface depletion gate and on the right side the etched side gate. These two gates define the dimension of the quantum wire. (b) Schematic picture of the electron motion by different applied magnetic fields. One can see the magnetically deflection of the electrons towards the constriction depending on the magnetic field direction.

Fig. 2-3 shows the experimentally detected conductance as a function of the top-gate voltage V_{tg} of such a hybrid constriction. For these measurements we applied a bias voltage V_{bias} of $200mV$. In order to test functional dependences of G_{AS} on the drain voltages and the magnetic field strength, the conductance as a function of V_{tg} and V_{bias} was tested for different magnetic field strengths swept between 0 and $\pm 1T$. For positive top-gate voltages and values of V_{tg} down to about -1.5 V, the conductance remains almost constant associated with the open state of the device. For a zero magnetic field the conductance is

approximately $20\,e^2/h$. By sweeping down the top-gate voltage from -1.2V to -1.9V the value of the conductance decreases to about $11\,e^2/h$ due to the electrostatic definition of the hybrid constriction. For values of the top-gate voltage V_{tg} smaller than -1.9V, as indicated by an arrow V_{def} in the Fig. 2-3, electron transport takes place only through the hybrid constriction. If one compares now the curve from an applied magnetic field of $0T$ with the curves of the magnetic field of $\pm 0.5T$ and $\pm 1T$ one can see first a decrease of the conductance from $20.3\,e^2/h$ to $12.3\,e^2/h$ and $7.9\,e^2/h$, respectively, caused by the magnetic depopulation of the channel. More interestingly, the reduction of the conductance due to the magnetic field is not equal for different signs of the magnetic field. E.g. for $V_{tg} = -2.0V$ and B=+$0.5T$, the conductance is $8.8\,e^2/h$. A change of the magnetic field direction with B=-$0.5T$ leads to G=$8.2\,e^2/h$. For a magnetic field of +$1T$ the value decreased to $6.6\,e^2/h$ and for -$1T$ to $6.1\,e^2/h$.

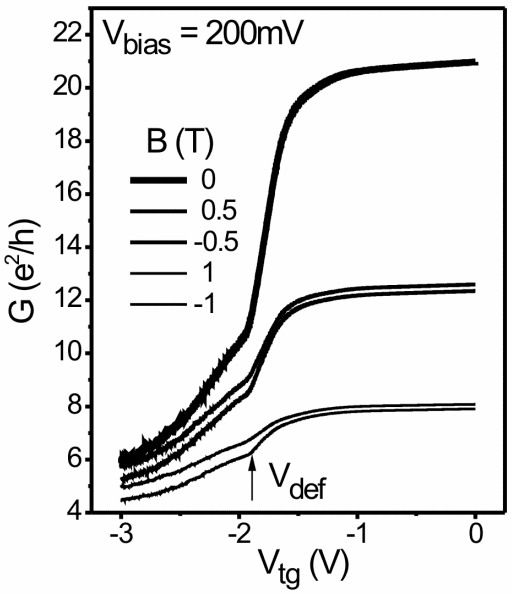


Fig. 2-3: Conductance G versus top-gate voltage V_{tg}. For V_{tg}<1.9V, the channel in the hybrid constriction is defined and G differs significantly when the magnetic field direction is changed.

In Fig. 2-4 a) G_{AS} is plotted for a top-gate voltage V_{tg}=-2V and a side-gate voltage V_{sg}=0V as a function of V_d for different magnetic-field strengths. Also the data determined for a reference structure fabricated without a metallic top-gate, but solely defined by etching of two trenches into the GaAs/AlGaAs heterostructure forming a 100 nm wide side-gated quantum wire are presented. The maximum asymmetric conductance of the reference structure is $|G_{AS}| = 19\times10^{-3}e^2/h$ and attributed to an unintended inplane asymmetry of the etched side-walls[27]. If one compares the reference value with the corresponding value determined for the constriction with an intended asymmetry for the same magnetic field strength (0.8 T), one can see that $|G_{AS}| > 0.3\,e^2/h$ of the constriction with the hybrid confinement is significantly larger. Interestingly, $|G_{AS}|$ decreases for a critically large voltage $V_d = V_c \sim 30-70\,mV$. $|G_{AS}|$ was also found to be a function of the magnetic field strength. In Fig. 2-4b the dependence of the maximum asymmetric conductance $|G_{AS}|$ versus B is

shown. $|G_{AS}|$ increases linearly with B up to 0.2T and for values larger than $B = B_c = 0.4T$ it remains almost constant.

The large conductance asymmetry is attributed to unequal backscattering of electrons at the different side walls. For modelling of G_{AS} the role of backscattering in quantum wires on the conductance was considered. According to Hartmann et al. the asymmetric conductance can be written as $G_{AS} = 2e^2\, p/\left(h\left(1+\Gamma_{2D}/2\Gamma_{1D}\right)\right)$, where p is a dimensionless parameter accounting for the difference in backscattering rates at the boundaries by $2p\Gamma_{1D}$ [27]. To estimate p, one can take into account that for a critical magnetic field $B = B_c = 0.4\ T$ all electrons moving from source to the drain are deflected dominantly towards one side, i.e. the magnetic length $l_B = \sqrt{\hbar e / B}$ is half of the geometrical width of the constriction. Therefore, $p = 1$ provided that the electrons travel only in one direction, i.e. the voltage $V_d >> 2E_F / e \sim 22\ mV$. Having in mind that a randomization of electron trajectories will take place for an excess energy of electrons in the channel larger than the phonon energy $E_{Ph} \sim 37\ mV$ (LO), G_{AS} will be reduced for $V_d < 2E_{Ph}/e \sim 74\ mV$ [28].

Thus an upper bound for the drain voltage up to which G_{AS} will increase is set as $V_c = 74\ mV$. As a result $p = BV_d / B_c V_c$. The scattering rate was determined from the linear conductance as $\Gamma_{1D}/\Gamma_{2D} \sim 6\%$. In Fig. 2-4 b) the red line is calculated from this model. It is worth to mention that the asymmetric conductance is the dominating effect for small magnetic fields in non linear transport as compared to small bias voltages where G is a symmetric function in B. This principally implies the potential to detected small magnetic fields with a two-terminal asymmetric constriction. In Fig. 2-4 c) the two-terminal voltage V_d is plotted as a function of B for a bias voltage of 200 mV. As indicated by the line the slope of the curve for $B = 0T$ is 9 mV/T.

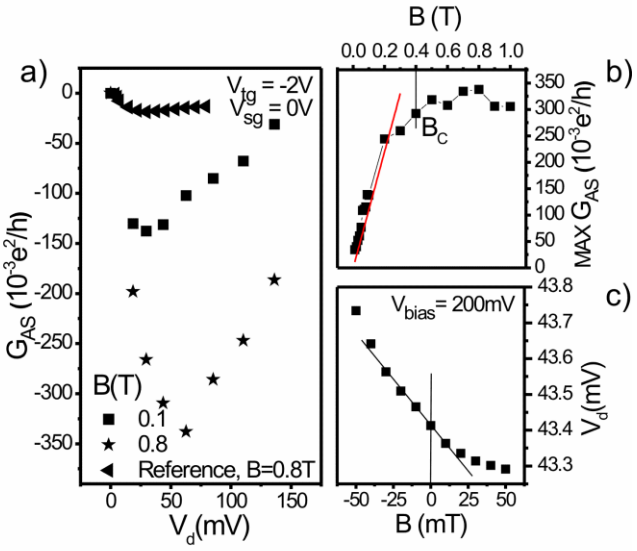


Fig. 2-4: (a)G_{AS} as a function of the probe-voltage V_d for different magnetic fields is compared with the asymmetric conductance reference from D. Hartmann et al. One can see a higher value of the asymmetric conductance with asymmetric side walls than symmetric side walls. (b) The maximum of the asymmetric conductance MAX $|G_{AS}|$ versus B increases linear and saturates for $B>B_C=0.4T$. (c) Probe-voltage V_d versus magnetic field strength. The asymmetry is the dominating magnetic field effect for small B.

Fluctuation relations without micro-reversibility for two-terminal conductors

We have investigated extensions of the fluctuation-dissipation theorem to non-equilibrium transport and derived relations which hold even if the Onsager relations fail. In the original work we have exemplified this connection for electrical Mach-Zehnder interferometers. In a more recent work we have illustrated the connection between rectification (the second order conductance coefficient) and noise for a two terminal conductor subject to a magnetic field. Theory predicts a term in the second order coefficient that is proportional to the magnetic field B and the interaction strength (capacitance). Our fluctuation relations imply that in the noise there should be a term that is linear in temperature, linear in magnetic field and linear in voltage. As a consequence the equilibrium Nyquist-Johnson noise is not the minimal noise. Rather an asymmetric dependence of the noise on voltage should be observed. Experiments which illustrate this behavior are currently under way by a group in Kyoto headed by Kensuke Kobayashi.

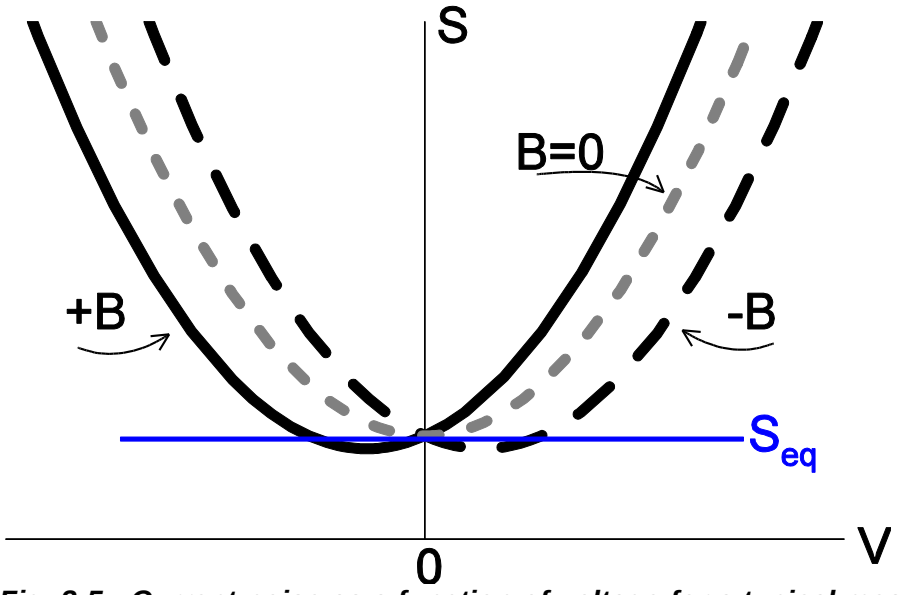


Fig. 2-5 : Current noise as a function of voltage for a typical mesoscopic conductor. In the absence of a magnetic field the noise is a symmetric function of voltage with the Nyquist-Johnson noise at its minimum. In the presence of a magnetic field B the minimal noise occurs at some finite voltage which depends on the interaction (capacitance) of the sample. After Ref. [29***].***

2.2.5 Task 1.5 – Shot noise in non-linear regime of multiterminal structures

We have investigated the effect of Coulomb interaction on the transport of two nearby conductors. One of the conductors can act as a driver and induce a current in the other nearby conductor even if this conductor is unbiased. The current in the driven system is termed the “drag” current.
This system is interesting because the appearance of a current demonstrates the breaking of detailed balance. Nevertheless as we show, the two conductors obey non-equilibrium fluctuation relations. The model is illustrated in the figure below. It consists of two quantum dots which are capacitively coupled. The minimal set of states which need to be taken into account are also illustrated in this figure. In contrast to the old ideas on Coulomb drag here the current is induced through energy transfer. The drag current can be in the direction or against the direction of the driver current. In Ref. [30] the fluctuation relations are verified numerically.

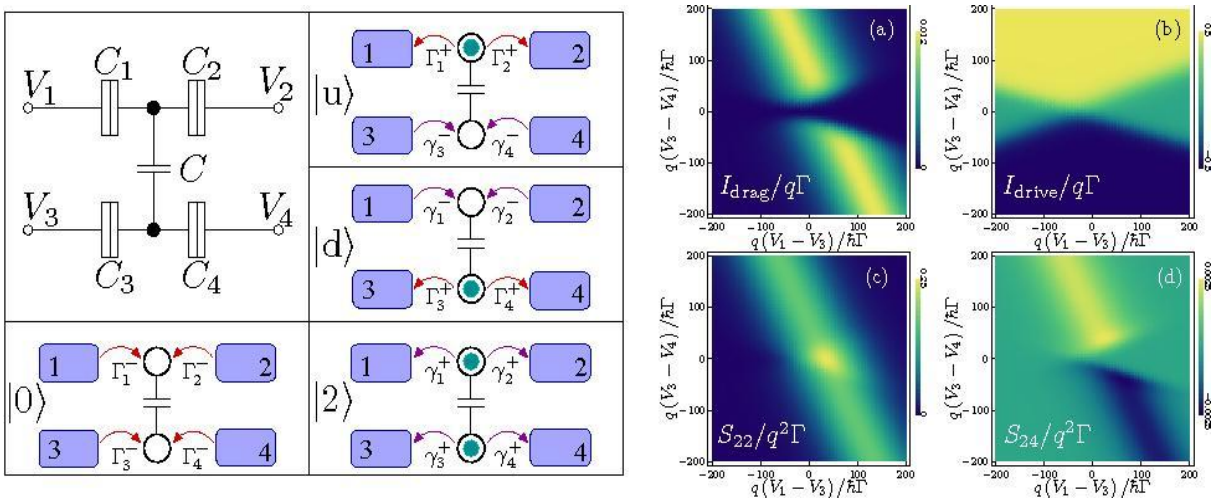


Fig. 2-6 : Left: Coulomb coupled quantum dots. The minimal set of states. Right: The four panels give the drag current, the driver current, the auto-correlation of the current fluctuations of dragged system and the cross-correlations as a function the voltage across the driver $V_2 - V_4$ and the voltage between the left two contacts of the quantum dots, $V_1 - V_3$.

2.3 Deviations from work programme and corrective actions

There are presently no deviations from the work programme.

2.4 List of deliverables

Del. No	Deliverable title	Lead partici-pant	Due date	Delivery date	Estimated person-months	Used person-months
D1.2	Report on capacitance effects in coupled quantum wires	UNIGE	M30	M30	15	16
D1.3	Report on charging and large deviation statistics	UNIGE	M36	M36	14	16

The reports were delivered in time.

2.5 List of milestones

There are no attainable milestones in the third year.

[23] *"Universal detector efficiency of a mesoscopic capacitor", Simon E. Nigg and Markus Buttiker, Phys. Rev. Lett. 102, 236801 (2009).*
[24] *H. Kothari, A. Ramamoorthy, R. Akis, S. M. Goodnick, D. K. Ferry, J. L. Reno, J. P. Bird, J. of Appl. Phys. 103, 013701 (2008).*
[25] *L. Worschech, F. Beuscher, A. Forchel, Appl. Phys. Lett. 75, 578 (1999).*
[26] *H. van Houten, B. J. Wees, J. E. Mooij, C. W. J. Beenakker, J. G. Williamson, and C. T. Foxon, Europhys. Lett. 5, 721 (1988).*
[27] *D. Hartmann, L. Worschech, A. Forchel, Phys. Rev. Lett.* ***78****, 113306 (2008).*
[28] *R. I. Hornsey, A. M. Marsh, J. R. A. Cleaver, H. Ahmed, Phys. Rev. B 51, 7010 (1995).*
[29] *"Fluctuation relations without micro-reversibility in non-linear transport", Heidi Forster and Markus Buttiker, AIP Conference Proceedings 1129, 20th International Conference on Noise and Fluctuations, M. Macucci and G. Basso, eds. (Melville, New York, 2009). p. 443 arXiv:0903.1431*
[30] *"Mesoscopic Coulomb drag, broken detailed balance and fluctuation relations'", Rafael Sanchez, Rosa Lopez, David Sanchez, Markus Buttiker, (unpublished). arXiv:0910.3300*

3. WP2 – Technologies for subthermal switching device

3.1 Objectives and starting point of work at beginning of reporting period

This WP deals with the SUBTLE device technologies. Already major contributions were reached within the first two years of SUBTLE. Gain and bistable switching in FBFETs were demonstrated. Bistable switching was reached in III-V and Si based technological routes. New contacts of bilayers were demonstrated. Within the third year of SUBTLE, we used the contact technology also to design principally narrow contacts to our nanoelectronic transistors. In this way, we have been able to solve a fundamental problem in 2DEG coupled contacts of large coupling capacitors, which usually limits such structures to be operated only at low frequencies. To strengthen the applied technologies, an objective in this WP was dedicated to the demonstration of the XENOS designed new pattern generator, with the possibility of implementation SUBTLE device designs and ultra-fast writing speeds.

3.2 Progress towards objectives

3.2.1 Task 2.1 – Realization of vertically coupled 2DEGs in GaAs and Si

Within the first and second period major achievements have been successfully reached:

- ***Progress in GaAs based molecular beam epitaxy (MBE) growth***
  - GaAs/AlGaAs heterostructures with two quantum wells (QW) only separated by a thin AlGaAs barrier with a thickness less than 10nm have been fabricated with independent electric contacts applying selective etching techniques
- ***Progress in Si-based bi-layer device fabrication***
  - First observation of bistable switching in Si bilayers
  - Full transport measurements with Si e-h-bilayers showed first EH drag resistance effects in a single nanostructure

3.2.2 Task 2.2 – Patterning technology of laterally coupled conductors

<u>Patterning of narrow contacts for power gain in laterally coupled conductors</u>

Here, we report on the alternating current (ac) and direct current (dc) characterization of TTJs and their suitability as amplifiers for ac signals in the gigahertz range. The TTJs are based on a modulation-doped heterostructure with a shallow 2DEG, which is situated approximately 33 nm below the surface. By applying mask techniques and wet chemical etching, TTJs with gold contacts only about 1 µm away from the central branch of the TTJs were fabricated. Clear transistor characteristics with maximum transconductance values exceeding 100 µA/V are demonstrated. For the ac characterization, the scattering parameters of the device are analyzed and power gain up to 1.5 GHz is observed. We relate the gigahertz power gain to the implementation of the narrow gold contacts, which control the quantum capacitance of the electron reservoirs. The TTJs were based on a modulation-doped GaAs/AlGaAs heterostructure, which was grown by molecular beam epitaxy. In Fig. 3-1 (a) a schematic cross section of the layer sequence is shown. On a semi-insulating GaAs substrate, a 200 nm thick GaAs buffer followed by a superlattice was deposited. The superlattice consists of ten periods of an alternating sequence of 25 nm thick $Al_{0.3}Ga_{0.7}As$

and 10 nm thick GaAs layers. On top of this, 1 µm GaAs followed by a 30 nm thick Si-doped $Al_{0.3}Ga_{0.7}As$ layer were grown. 3 nm of Si-doped GaAs caps the $Al_{0.3}Ga_{0.7}As$ layer and completes the heterostructure. Close to the heterostructure interface, a 2DEG is formed and, therefore, the 2DEG is situated approximately 33 nm below the surface. For the Si oping, the concentrations were $2x10^{18}$ and $3x10^{18}$ cm^{-3} in the $Al_{0.3}Ga_{0.7}As$ layer and in the GaAs layer, respectively. The TTJ consists of a narrow channel connecting two electron reservoirs—drain and source—with a gate branch monolithically attached to the center of the channel. Fig. 3-1 (b) shows a scanning-electron microscope (SEM) image of the TTJ. For the lateral structuring of the TTJs, the upper layers of the heterostructure were locally removed by applying mask techniques and wet chemical etching. The etched regions between the conducting parts of the device provide a good insulation. To improve the high-frequency operation of the TTJ, narrow gold contacts were designed on top of the structured TTJ. For the definition of the gold contacts, high resolution electron-beam lithography was used. The narrow gold contacts are less than 1 µm apart from the branching point, i.e., the gate branch. Due to this reduced size of the electron reservoirs, the quantum capacitance decreases and the impact on the transport properties is controlled.

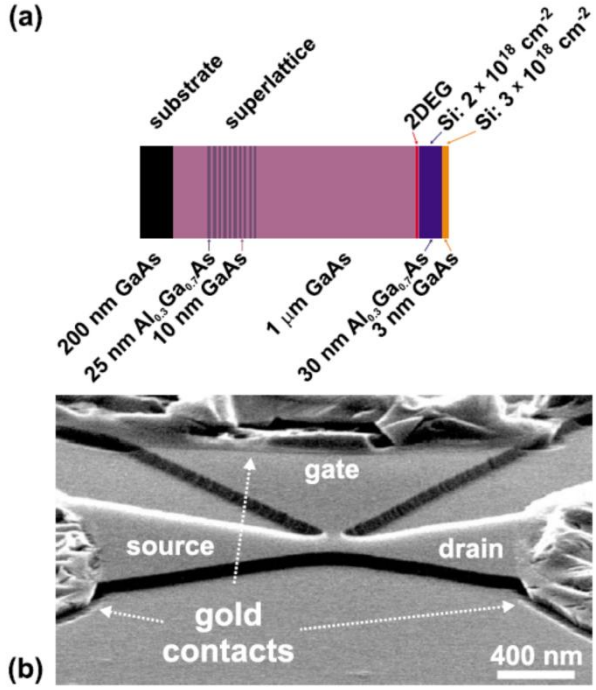


Fig. 3-1: (a) Schematic cross section of the layer sequence grown by molecular-beam epitaxy. (b) SEM image of the three-terminal junction with narrow gold contacts.

The dc characteristics of the TTJs were determined by measuring the device currents. The corresponding electric setup together with a sketch of the device currents and applied voltages is shown in the inset of Fig. 3-2 (a) The drain voltage V_d and the gate voltage V_g were applied to the drain contact and the gate branch, respectively, with the source connected to ground. All measurements were performed in the dark at room temperature. In Fig. 3-2 (a), the transfer characteristics of the TTJ are shown for V_d=0.3, 0.7, 1.1, and 1.5 V. For V_g<−0.75 V, a small drain current is detected and, with increasing V_g, I_d increases monotonically. For V_d=1.5 V, gate voltages larger than −0.15 V lead to drain currents exceeding 44.8 µA. With decreasing V_d, the maximum drain current and the slope of the I_d-V_g curves decrease. In addition, the OFF-state drain current $I_{d,OFF}$ of the device, which is equal to the minimum drain current in the transfer characteristics, is reduced for smaller drain voltages. The inset of Fig. 3-2 (b) displays the OFF-state drain current versus the drain voltage. For small V_d, $I_{d,OFF}$ is in the range of 6 µA and increases linearly with a slope of 2.3 µA/V. This linear increase leads to a maximum of $I_{d,OFF}$=11.3 µA/V at V_d=2.0 V. Fig. 3-2 (b) shows the output characteristics of the device for V_g ranging from −0.8 to 0 V in steps of 0.2 V. For V_g=0, sweeping up V_d results in a continuous increase of I_d. At the saturation point

V_d=0.9 V, a saturation current of 49.7 µA is reached. Drain voltages beyond this saturation point lead to a linear increase of I_d with an average slope of 3.3 µA/V. For smaller gate voltages, the saturation current is reduced and the saturation point is shifted toward lower values of V_d. For gate voltages below −0.8 V, the linear increase of I_d is suppressed for drain voltages smaller than the saturation point, which corresponds to a cutoff of the channel. However, an OFF-state drain current in the order of a few microamperes is observed. Both transfer and output characteristics reveal clear transistor-like behavior, which is in good agreement with recent findings. [31, 32] The origin of the OFF-state drain current can be attributed to the formation of a parallel conduction path in the channel which cannot be electrically controlled by the gate voltage. [33] Hence, a nonzero OFF-state drain current is observed even for gate voltages smaller than the threshold voltage. The higher the drain voltage the more current flows and $I_{d,OFF}$ is increasing linearly with V_d. The ac properties of a device are determined by its cutoff frequency f_T of the device. With increasing g_{max}, f_T is pushed toward higher values and the high-frequency performance is improved. Thus in TTJs, the ac performance should benefit from an enhancement of the switching properties, i.e., especially from a large transconductance. Fig. 3-3 (a) shows the transconductance of the TTJ versus the drain voltage. For small V_d, the transconductance of the TTJ is close to zero. With increasing drain voltage, g_{max} increases linearly until V_d=0.75 V is reached. For drain voltages larger than this value, the transconductance has a constant value of 105 µA/V. To determine the cutoff frequency of the device, the scattering parameters (*s* parameters) were analyzed. For this purpose, a network analyzer (HP 8510C) was used together with a high-frequency signal generator (HP 83650B) and an *s*-parameter-test set (HP 8517B). The device was contacted by micro probes (Picoprobe), which are suitable for ac signals up to 50 GHz. The applied voltages were kept constant to V_g=−0.5 V and V_d=1.5 V, which allows to operate the

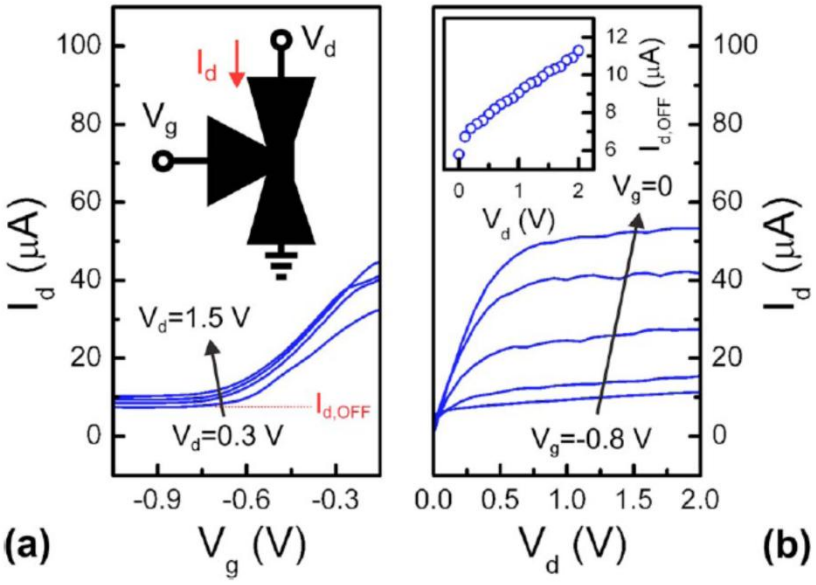


Fig. 3-2: (a) Transfer characteristics of a three-terminal junction for drain voltages V_d ranging from 0.3 to 1.5 V at room temperature. Inset: Schematic view of a three-terminal junction together with the electric setup. (b) Output characteristics of the three-terminal junction for gate voltages V_g ranging from −0.8 to 0 V at room temperature. Inset: OFF-state drain current $I_{d,OFF}$ vs drain voltage V_d.

TTJ at the point of maximum transconductance. Based on the measured s parameters, the maximum-available-power gain G_A was calculated and the result is displayed in Fig. 3-3 (c) for a frequency range from f =0.5 to 2.5 GHz. For frequencies smaller than 1.5 GHz, G_A is larger than 0 dB, i.e., the ratio of the available power at the load to the available power at the power source is larger than 1. With increasing frequency, G_A decreases and reaches a value

of 0 dB for f =1.5 GHz, which corresponds to the cutoff frequency of the device. Our ac measurements show that the TTJ can be operated as amplifier with power gain up to 1.5 GHz. For small device dimensions, the occurrence of the quantum capacitances of the contacts has to be taken into account. Based on a classical approach for field-effect transistors, Fig. 3-3(b) shows an electric equivalent circuit with the quantum capacitances C_{qs} and C_{qg} of the source and the gate, respectively. The cutoff frequency is given by $f_T=g_m/(2\pi C_{qs})A$, with $A=[C_{qs}^2/C_g^2+C_{qs}^2/C_{qg}^2+2C_{qs}^2/(C_gC_{qg})+2C_{qs}/C_g+2C_{qs}/C_{qg}]^{1/2}$ characterizing by the capacitive coupling in the TTJ. It should be pointed out that with respect to the large size of the gate contact, the influence of C_{qg} on f_T can be neglected. For the given device design, C_{qs}=8 fF is found. A cutoff frequency in the order 1.5 GHz is related to a gate capacitance in the range of 20 fF. Such a large gate capacitance is attributed to the device geometry and a dynamic component of Cg recently observed in similar structures. [32,33]

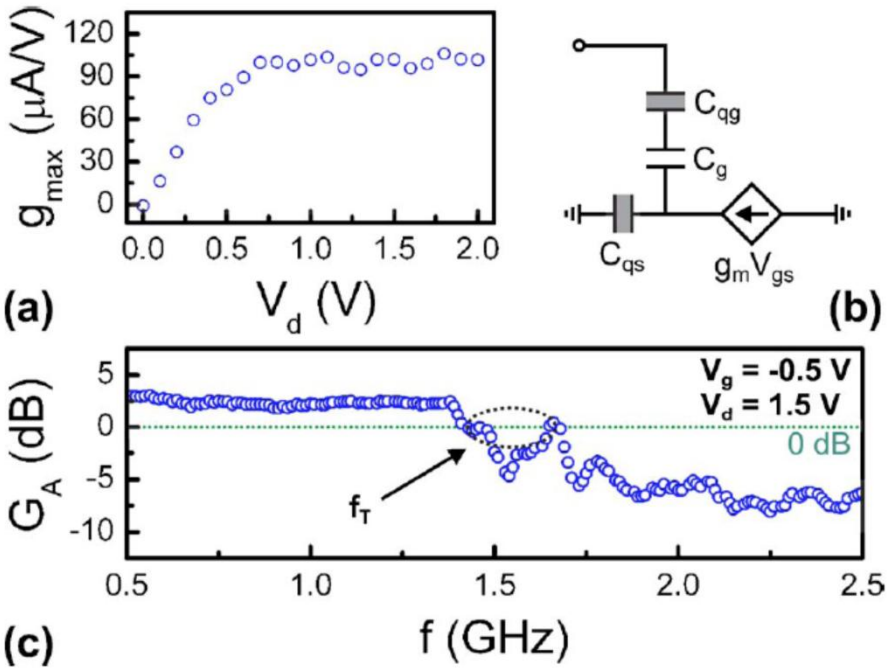


Fig. 3-3: (a) Maximum transconductance g_{max} vs drain voltage V_d at room temperature. (b) Electric equivalent circuit of the TTJ. (c) Maximum-available-power gain G_A vs. frequency f.

<u>Processing technology on HfO_2-InGaAs/InP</u>

InP and related compounds are key semiconductor materials for radio frequency (RF) electronics, as well as 1.3 and 1.5 μm spectral region optical fiber communications. Particularly, modulation doped $In_{0.75}Ga_{0.25}As$/InP two-dimensional electron gas (2DEG) is a very advanced material system. It has interesting electron transport properties, such as small electron effective mass, high electron mobility, large effective g-factor, and strong spin-orbit coupling strength, which makes it very promising in future nanoelectronics and spintronics. However, the processing technology is far from mature, which results in the fact that InP-based nanodevice properties fall far behind those of GaAs-based devices. For instance, to date, most gate-defined quantum dots are realized in traditional GaAs/AlGaAs system. The top gating technology is very difficult in InGaAs/InP because the metal-InP Schottky barrier height (SBH) is too small (typically < 0.5 eV), which results in large gate leakage current. Although in high-electron-mobility transistor (HEMT) technologies people introduce InAlAs layers to increase the SBH, it is still one of the unsolved major technology difficulties. Furthermore, InAlAs is easily oxidized and the gate recess process is rather complex. Thus, we have tried another approach, where a high-k dielectric thin film is incorporated onto the InGaAs/InP to reduce the gate leakage and improve the gating efficiency. Little report in this field can be found in the literature, since it is technologically hard. However, after tremendous

efforts, we have successfully developed a processing technology of making nanodevices on InGaAs/InP by gating through a high-k HfO_2 thin film.

The 2DEG used here is a metal-organic vapor phase epitaxial (MOVPE) $In_{0.75}Ga_{0.25}As$/InP heterostructure. The layer sequence is as follows: semi-insulating InP substrate, 50 nm undoped buffer layer, 9 nm thick InGaAs quantum well, 20 nm thick undoped InP barrier, 1 nm thick Si-doped InP layer, and finally a 20 nm thick undoped InP capping layer. This material has an electron mobility of 6.77 m^2/Vs, an electron sheet concentration of 4.2×10^{15} m^{-2} and a mean free path of 725 nm at 300 mK, determined from Hall measurements in dark. The wafer is cut into 3 mm$\times$4 mm pieces for device processing.

The fabrication of devices begins with mesas. On the semi-insulating substrate, the purpose of fabricating mesas is to create electrically separate islands for device isolation. Mesas can be made by lithography and etching, and their design should be as small as possible, provided that there are enough areas for ohmic contacts and fine structures. Small mesas offer a larger device packaging density, a higher operation speed and a smaller gate line leakage. From an industrial point of view, photolithography is ideal for mesa fabrication. However, since the present study involves very small samples (3 mm$\times$4 mm), electron beam lithography (EBL) is more convenient. A double layer negative resist ma-N 2403 was used in the EBL with the consideration that it has a large endurance time in strong acids as well as a decent adhesion to the samples. In order to save exposure time, an extremely large beam step size was used, i.e., 0.5 μm, along with an aperture of 120 μm. The optimal dose was 80 μC/cm^2. Although the step size was large, the proximity effect connected all the exposed points together, keeping the exposed resist as a continuous film protecting the mesa surface during etching. Dry etching is generally more anisotropic than wet etching and thus provides sharper mesa edges. This is, however, a disadvantage rather than an advantage in the present case, since steep mesa edges could prevent the top gate metal lines from climbing up to the mesa surfaces. Therefore, wet etching was utilized to define mesas. In the presented experiments, attempts were made to use a bromine-based etchant. In 5 min, the etching depth was found to be $\geqslant$200 nm, down to the semi-insulating substrate. The rake angle at the mesa edge was about 45 ^{o} for all crystal directions.

The ohmic contacts were made by EBL and thermal evaporation followed by lift-off. The EBL procedures were similar to the previous ones, with the exception of a change to a double layer positive resist ZEP 520A to save the exposure time. We use Au/Ge for ohmic contact metals on n-InP. The eutectic temperature of the AuGe alloy is 361 ^{o}C and, thus, the annealing temperature should be within the same range. 20 nm Au/60 nm Ge/120 nm Au were grown on InGaAs/InP and annealed at 370 ^{o}C for 2 min. At room temperature, the typical ohmic contact resistance of the materials was a few kΩ, and the resistance between two neighboring mesas was on the order of 10^8 Ω.

The most crucial part is the growth of HfO_2 layer. The HfO_2 is deposited in Savannah 100 atomic layer deposition (ALD) system from precursor hafniumtetrakis(dimethylamide) $Hf[N(CH_3)_2]_4$ and water vapor. When HfO_2 is directly grown onto InGaAs/InP, a parasitic accumulation layer (PAL) will form at the HfO_2-III-V interface. The physical origin of the PAL can be ascribed to the InP native oxide, and is currently under our investigation. Previously, we have developed a technique based on sulphur passivation, which is carried out before growth. This surface pretreatment is very important to get rid of the PAL between InGaAs/InP and HfO_2. The growth temperature is 300 ^{o}C, because at lower growth temperatures the sulphur passivation will be destroyed. Based on that, we have fabricated single quantum dot (QD) devices and observed single electron charging and studied spintronics at 300 mK. However, we also found that the effect of sulphur passivation of the InGaAs/InP surface is short-lived, namely degrading with time, resulting in a short device lifetime. Because the growth is carried out at 300 ^{o}C, patterning of the HfO_2 films is difficult. So, if the sulphur passivation effect degrades, the PAL will reappear and during bonding, the gate bond wires

can penetrate the thin HfO_2 film and connect to the PAL. Electrons can leak into InGaAs/InP while applying negative gate voltages.

Recently, however, we have solved this technology problem by a cross-linked (CL) PMMA bridge technique. On mesas with ohmic contacts, HfO_2 is grown at 100 ^oC, where a lift-off technique is used to pattern HfO_2. Under our conditions, 250 ALD cycles yield a film of about 30 nm thickness. The dielectric properties of the HfO_2 films are similar to those grown at 300 ^oC, but with a higher breakdown field due to the amorphous nature. The permittivity k is estimated to be 16.6. Then, by using very high dose (30000 $\mu C/cm^2$) EBL, PMMA 950A6 resist is locally cross-linked at the HfO_2 edges (see Fig. 3-4), serving as bridges. Finally, the top gates are fabricated by single pixel line EBL and thermal evaporation of 50 nm Ti/Au, and the subsequent lift-off in Remover 1165. Here, the gate bonding pads are placed outside of the HfO_2 area, and the PMMA bridges avoid any electrical contact between the gates and the PAL. Therefore, in the current technology, sulphur passivation is not needed to remove the InP native oxide and the PAL, and the devices are long-lived. Compared with the commonly used air bridge technique, PMMA bridges are easier to fabricate and mechanically much more stable.

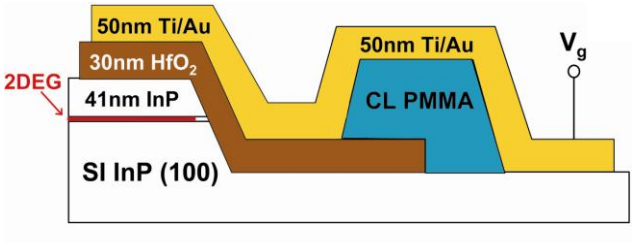


Fig. 3-4: A schematic diagram of the device. InGaAs/InP, HfO_2, Ti/Au and cross-linked PMMA are indicated by different colors. Static negative gate voltage V_g is applied to Ti/Au to deplete the 2DEG beneath.

Summarily, our processing technology of making gate-defined quantum devices on HfO_2-InGaAs/InP has been much more improved, compared to previous sulphur passivation based techniques. As a result, we have realized very stable coupled quantum dot FETs (field-effect transistors) with negligible charge rearrangement during measurements, which will be shown later in this report.

Memory diodes based on HfO_2-InGaAs/InP

The HfO_2 thin films are currently being intensively studied worldwide. We have shown that a PAL will form at the HfO_2-III-V interface if no sulphur passivation is carried out. This effect, however, can find its applications in memory devices. In the following we demonstrate our room temperature memory diodes based on it.

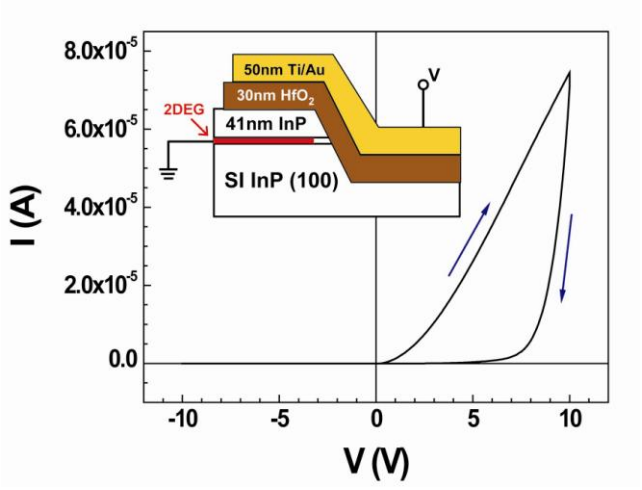


Fig. 3-5: I-V curve of the memory diode, where the 2DEG is grounded through the ohmic contact, and voltage V is applied to the top metal layer. Rectification and hysteresis effects are seen. Inset: schematic diagram of the device (cross-section). The 2DEG is marked with

The diode structures are illustrated in the inset of Fig. 3-5. It is achieved by four steps of EBL. Standard mesas (height > 200 nm, reaching the semi-insulating substrate) are etched in a Br-based solution, followed by the rapid thermal annealing of Au/Ge ohmic contacts. A lift-off technique is used to pattern HfO_2 films, where ZEP 520A resist is employed. The growth temperature is selected to be 100 ^oC, just below the glass transition temperature of ZEP 520A polymer ($T_g \approx 105$ ^oC). During the low temperature ALD, the purge time is elongated to 60-80 s to ensure a complete decomposition process of the precursors. Finally, 50 nm Ti/Au is thermally evaporated onto the HfO_2. The active area of the device, defined by the overlapping area of Ti/Au on top of the HfO_2 and semiconductor, is ~40 μm^2. Fig. 3-5 shows the I-V curve of the diode measured by Keithley 4200 semiconductor characterization system. The 2DEG is grounded and voltage V is applied to Ti/Au. At room temperature, rectification behavior with huge hysteresis at forward bias is observed. The current rectification effect, however, cannot be quantitatively explained by the thermionic emission and tunnelling model of a normal Schottky junction. We now propose a model to relate the PAL at the HfO_2-InGaAs/InP interface to the I-V curve in Fig. 3-5.

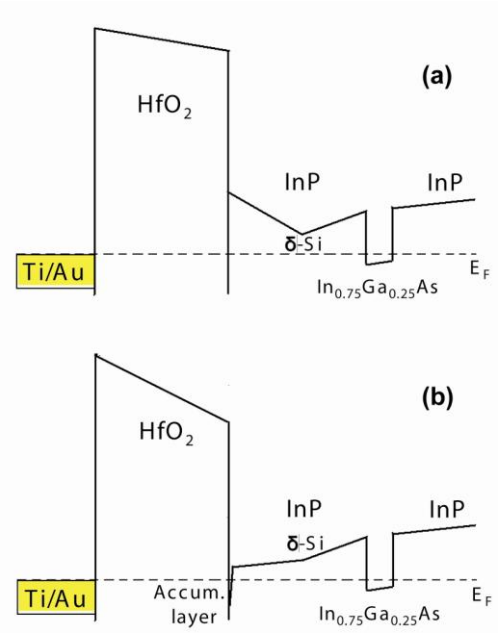


Fig. 3-6 : **A schematic drawing of the band diagram of the metal-HfO_2-semiconductor diodes under no bias. (a) Without and (b) with Fermi level pinning at the PAL at the high-k-InP interface.**

Fig. 3-6 is the thermal equilibrium band diagram of the devices, where (a) and (b) represent the cases without and with the PAL, respectively. In Fig. 3-6 (a), there is no Fermi level pinning at the HfO_2-InP interface and, therefore, the current is small under both forward and reverse bias conditions, corresponding to the case where the InP native oxide is removed. In Fig. 3-6 (b), a PAL is present at the HfO_2-InP interface, resulting in Fermi level pinning at this layer. The HfO_2 barrier from InP side is dragged down. Thus, at forward bias, the effective barrier height for the electron transport is much smaller than that in Fig. 3-6 (a). On the other hand, at reverse bias, the barrier height is basically unchanged compared with Fig. 3-6 (a). Therefore, the rectification can find its explanation in the PAL. In Fig. 3-5, the sweep begins from -10 V. While above the threshold (~1 V), electrons are injected from the semiconductor 2DEG to the metal. Some electrons are trapped at the HfO_2-InP interface PAL. During the backward sweep, the trapped electrons show Coulomb repulsion effect on the electron transport, resulting in a low state current. When it comes to the voltage beyond ~-1.5V, the PAL is depleted. Therefore, when it returns to forward bias, the current will be at the high state.

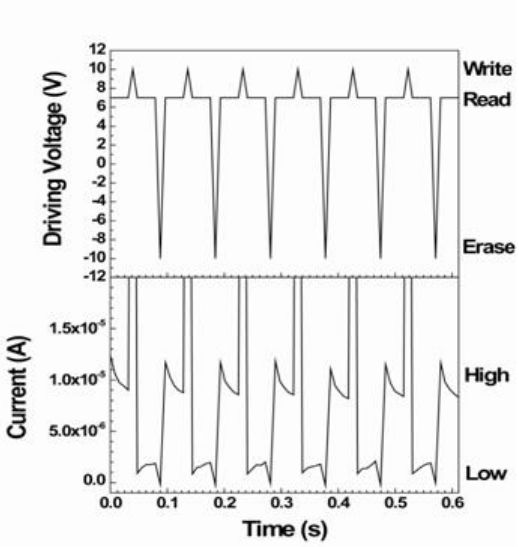


Fig. 3-7: **Time dependence of the driving voltage and the current, showing memory effect of the Ti/Au-HfO_2-InGaAs/InP diodes. The driving voltage has three levels: write at 10 V, erase at -10 V, and read at 7 V. The information is represented by two levels of the current, as indicated by "high" and "low" in the lower graph.**

Memory operation can be realized by charging/discharging of the PAL. Fig. 3-7 shows the room temperature raw data measured by Keithley 4200 without any signal processing, and the circuit configuration is unchanged. According to Fig. 3-5, a pattern consisting of write (10 V) and erase (-10 V) pulses with intermediate readings (7 V) is applied to the Ti/Au electrode of the diode. The lower curve in Fig. 3-7 represents the readout of the device, where the low and high current states are around 1.8×10^{-6} A and 9×10^{-6} A, respectively, yielding a bit separation I_{ON}/I_{OFF} of ~7.2. The mechanism of the memory diode can be explained as follows. During the write pulses, electrons are injected from the semiconductor into Ti/Au, and some of them are captured by the HfO_2-InP interface traps. Due to the Coulomb scattering effect, upon reading, the currents will be at the low state. On the other hand, the erase pulses can effectively remove the trapped electrons and the currents will consequently return to their high states while reading. Conclusively, Fig. 3-7 illustrates the simplest device principle of a memory diode utilizing the PAL.

3.2.3 Task 2.3 – E-beam pattern controller

The realization on the system level of the 100 Mhz e-beam pattern controller presented in the last reports has been finished. The implementation of the design with a latest generation XILINX Virtex FPGA showed a securely sustainable writing speed of 150 MHz during the functional tests, thus correlating to the expected writing speed from design, synthesis and simulation data. Our design therefore still is a factor of 3 ahead of the fastest commercially available systems.
For the pattern controller system, a final printed circuit board for the system's backplane has been designed and produced and the overall system including now scan logic, DAC board with galvanic isolation, system backplane, and separate power supplies for analog and digital parts of the system has finally been set up.
During the testing, problems with the stability of the system were found that could be traced back to problems with the mounting and soldering of the 688 ball grid pins of the Virtex FPGA device on the 8-layer printed circuit board of the scan logic.

The firmware of the Digital Signal Processor (DSP) on the scan logic board has been realized during the reporting period, including the hardware layer routines for the communication with the FPGA, multitasking scheduler and timer, vectorizer for the exposure shapes and USB communication stack for the communication with the lithography design software ecp.

The lithography design software has been adapted to support the new pattern controller and as well new features of the design software for the SUBTLE devices realized within in the workpackages 3 and 4 have been made available here.

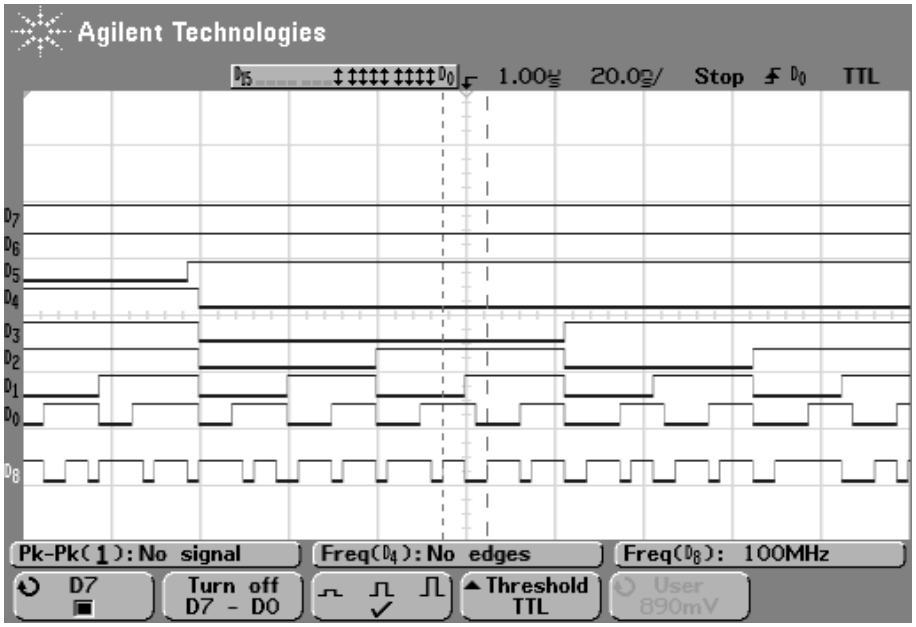


Fig. 3-8: Logic analyser screenshot showing 100 Mhz pixel frequency (D8)

Fig. 3-8 shows a screenshot of the digital part of X-deflection signals for a single lithography linescan with increment of 1 pixel at 100 MHz. D0 to D7 show the lower bits of the addressing word, D8 shows the actual writing frequency (the clock line going to the digital-to-analog converter).
Fig. 3-9 shows the design of an exposure test shape within the lithography design software: a rectangle with 1 million exposure pixels (from scan position 20000/20000 to 30000/30000 with an exposure increment of 10 pixels in order to get higher voltage levels for proper display).

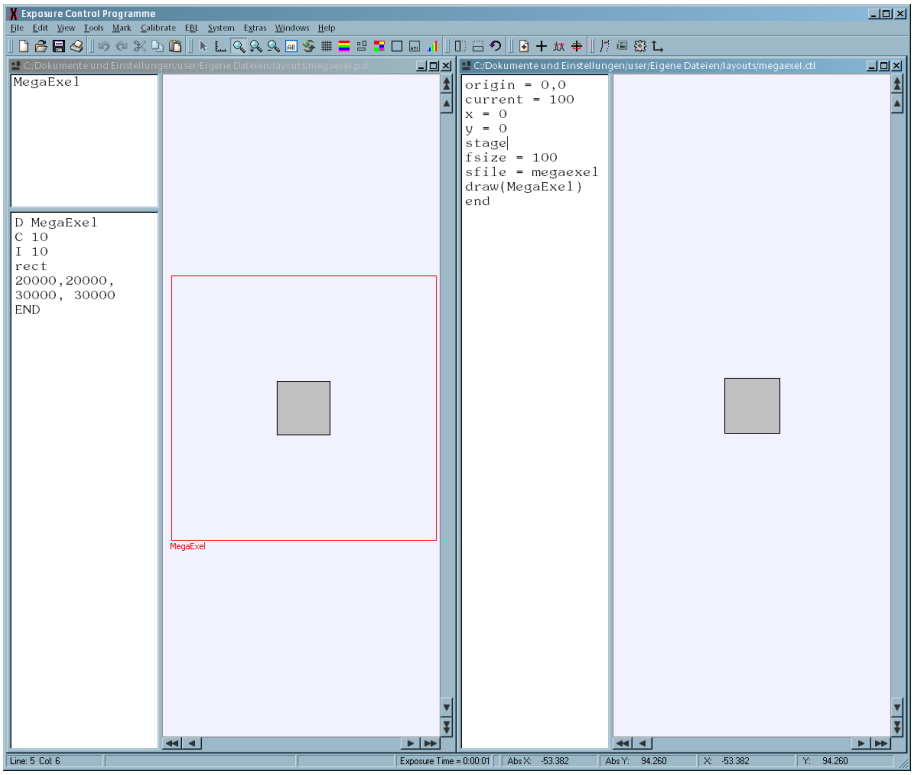


Fig. 3-9: exposure test shape design with 1 million exposure pixels

The resulting lithography exposure deflection signals in X-meander scan mode are shown in Fig. 3-10 and Fig. 3-11 (Ch. 1 is X-deflection, Ch. 2 Y-deflection).

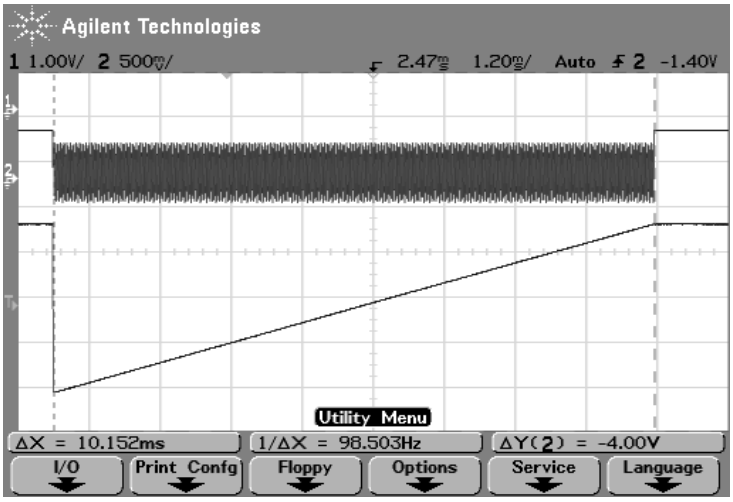


Fig. 3-10: Overall scan signals for a complete 1 Mpixel square.

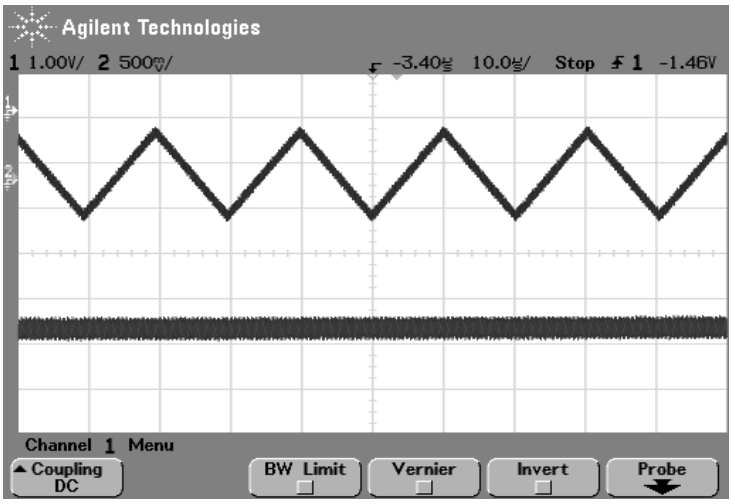


Fig. 3-11: Detail of scan signals for a single X-meander scan lines

It is shown here that a complete 1 Mpixel scan takes 10 ms as expected, a single line with 1000 pixel length 10 µs accordingly.
The combination of a SUBTLE device (see WP 4) created with the adapted SUBTLE CAD user interface of the lithography software (see Deliverable 2.3) and exposure with the new high-speed pattern controller is shown in Fig. 3-12. Fig. 3-11 displays the deflection signals as screenshot on the test-system, in Fig. 3-12.

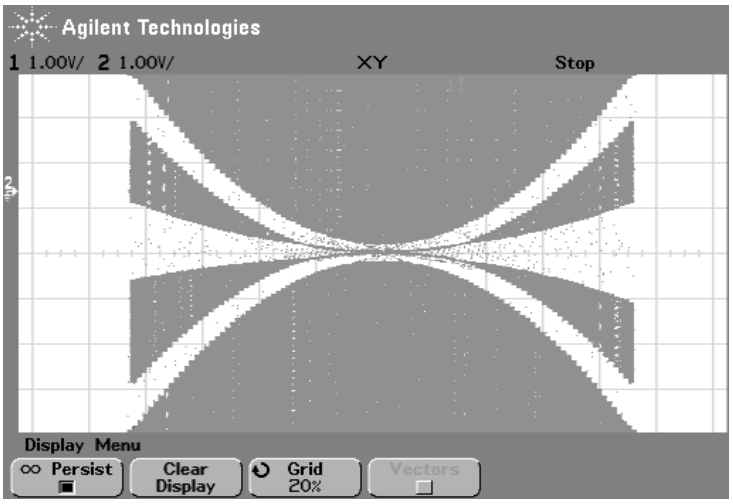


Fig. 3-12: Exposure of X-Wing with the high speed pattern controller at 100 MHz

3.3 Deviations from work programme and corrective actions

No deviations from work plan are required.

3.4 List of deliverables

WP Del. No	Deliverable title	Lead partici-pant	Due date	Delivery date	Estimated person-months	Used person-months
D2.4	Report on 100MHz EBL writing speed: full integration of the high speed into the lithography system's algorithms	XENOS	M36	M36	20	26,8

The report was delivered in time.

3.5 List of milestones

There are no attainable milestones in the third year.

[31] *H. Q. Xu, Appl. Phys. Lett.* ***80****, 853 (2002)*
[32] *C. R. Müller, L. Worschech, D. Spanheimer, and A. Forchel, IEEE Electron Device Lett.* ***27****, 208 (2006)*
[33] *C. R. Müller, L. Worschech, S. Höfling, and A. Forchel, IEEE Trans. Electron Devices* ***56****, 306 (2009)*

4. WP3 – EC feedback and single SR devices

4.1 Objectives and starting point of work at beginning of reporting period

The objectives here are engaged with single feedback FETs and double-dot FET structures. One deliverable is to report on coupled quantum dot FETs. We also expanded our studies on last year reported RTD nanostructures with tuneable on chip noise source. A basic goal for application of such kind of amplifiers is to demonstrate both inverted as well as non-inverted switching.

4.2 Progress towards objectives

This work package includes three tasks. All partners have contributed significantly for achieving the goals within the third year.

4.2.1 Task 3.1 – Transport and feedback in vertically coupled electron systems

Coupled electrons and hole transport in Si quantum well

Silicon-on-insulator (SOI) based double-gate SiO_2-Si-SiO_2 quantum well field-effect-transistors (FETs) [see Fig. 4-1 (a)] are being actively investigated [34,35]. The double-gate geometry provides means to effectively adjust the total carrier density inside the FET channel, which leads, e.g., to suppression of the fatal short channel effects and enhancement of the sub-threshold characteristics. The double-gate structure also enables adjustment of the width and position of the carrier distribution (or wave functions) inside the Si well. Carrier gas can be tuned to the middle of the well at symmetric double-gate voltage or pushed against either of the Si-SiO_2 interfaces by applying an asymmetric gate voltage, which has a relatively large effect on the carrier mobility [36,37]. The high dielectric strength of the SiO_2 also enables strongly asymmetric gate voltage that can overcome the energy gap of Si even in relatively thin Si wells. This leads to formation of a field induced electron-hole (EH) bilayer inside the device [see Fig. 4-1 (b)&(c)] analogously to the III-V system of Ref. [38], but without any heterostructure based energy barrier between the different layers.

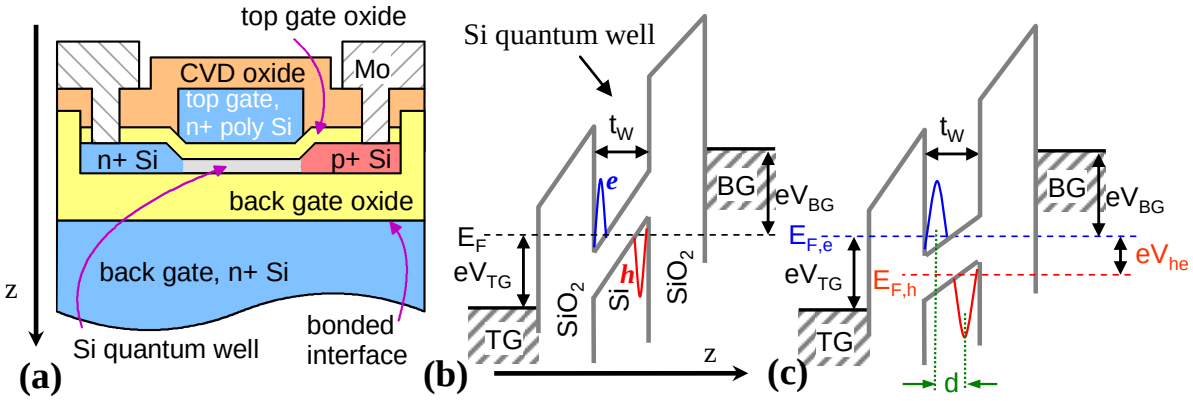


Fig. 4-1: (a) Schematic cross-section of a double gated Si quantum well FET geometry. The n+ and p+ regions make contact to electron and holes in the well, respectively. (b) Band diagram of the device channel at strong push-pull double gate bias. TG (BG) stands for top-gate (back-gate). The 2D electron and hole gases reside in the conduction and valence band, respectively. (c) Illustration of interlayer gating, which is obtained by applying an interlayer bias V_{he} between the layers. Finite V_{he} reduces the distance d between the different carrier gases and enhances the mobility. Here the well width t_W = 22 nm.

Our Si quantum well devices were fabricated on commercially available bonded SOI wafers. The fabrication process has been described in detail in deliverable D2.2. The quantum he well width t_W = 22 nm and the top (back) gate oxide thickness is t_{OX} = 50 nm (t_{BOX} = 83 nm). Our device has self-aligned n-type and p-type contact regions enabling simultaneous measurements on electrons and holes [see Fig. 4-1 (a)]. The contact between electron (hole) gas inside the Si well and p+ (n+) regions is a pn-junction with high isolation as demonstrated in Fig. 4-2. One effect of interest in our Si devices is the inter-layer friction, which has been a topical subject since the early drag experiments on electron-electron [39] and EH [40] bilayers (see Ref. [41] for a review). The room temperature transport properties in single and bilayer regime together with the drag effect of a 22 nm-thick double-gate Si well were reported in year 2008 SUBTLE report and also in Ref [42]. In 2009 we have performed an exhaustive transport studies between 4 – 300 K. The main focus has been on the EH bilayer regime. Fig. 4-3 (a) shows an optical micrograph of the Hall bar device explored in the transport experiments. Electronic setup is illustrated in Fig. 4-3 (b).

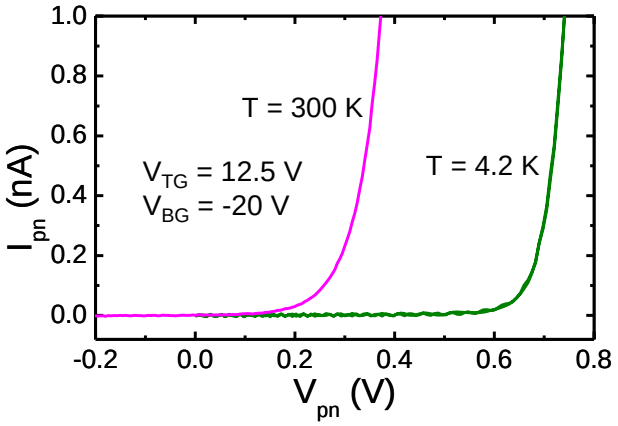


Fig. 4-2: Measured current between the p and n-type contacts as a function of the applied bias between the contacts in the EH bilayer gate bias regime at different temperatures. At 300 K (4.2 K) the layer-to-layer isolation is strong if V_{pn}=V_{he} < 200 mV (600 mV).

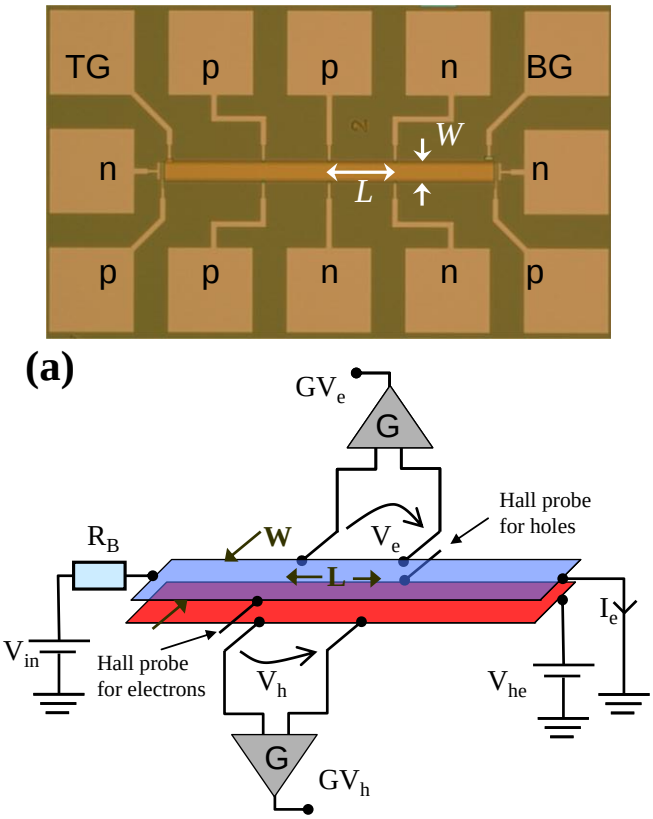


Fig. 4-3: (a) Optical microscope image of the lateral device geometry utilized in the experiments. Letters p and n on the Mo pads refer to the type of Si to which the particular pad is connected. The width of the channel W = 50 μm and the probe distance L = 200 μm. (b) Schematic illustration of the electrical setup for the transport experiments in the case when electron gas is connected to the excitation V_{in}. In the experiment the electron and hole layer voltages (V_e and V_h , respectively) are measured with low noise differential voltage amplifiers that have input impedance above 10^9 Ohm . The drive current I_e (or I_h) is measured with low noise current-voltage converter. Due to the large dynamic range of the sample resistance in the experiment we have typically set the biasing resistor R_B to zero.

The electronic properties were investigated in the linear response regime, when the EH system is described by a set of linear equations $V_i = (W/L)G_{ij}I_j$, where I_i and V_i are the current and the voltage of the different type of carriers [see Fig. 4-3 (b)] ($i,j = e$ for electrons and $i,j = h$ for holes). The elements G_{ij} define the conductance matrix and its inversion gives the resistance matrix with elements R_{ij}. The diagonal elements G_{ee} and G_{hh} as a function of the top (V_{TG}) and back gate (V_{BG}) voltages measured at 4.2 K are shown in Fig. 4-4. The bilayer regime is reached in the lower right corner of Fig. 4-4 (a). The behaviour of the Gee contours in this gate bias regime indicate that there are holes that can screen the back-gate field. However, the holes are under extreme localisation: at the lower right corner G_{hh} ~0.01e^2/h(R_{hh}~2.6MΩ). The situation can be improved by interlayer gating. By applying an interlayer voltage of V_{he}=0.5V not only the threshold of the individual layers shift but also the disorder is reduced [Fig. 4-4(b)]. This can be recognized by comparing $G_{ee}(V_{tg})$ of Fig. 4-4 (a) and (b): in the latter figure in the bilayer regime the change in V_{tg} required to jump from contour G_{ee} = 0.1 to G_{ee} = 5 has been significantly reduced in comparison with former figure. Note that the applied interlayer voltage introduces no leakage between the layers at 4.2 K (see Fig. 4-2). At this interlayer bias the leakage remain zero up to T~200K. Fig. 4-5 shows R_{ee}, R_{hh} and R_{he} as a function of temperature at different balanced carrier densities $n = n_e = n_h$. R_{ee} has an insulating behaviour when $n_e < 6\times10^{15}$ m^{-2}. The situation is not so clear cut for R_{hh}, which is due to the strong disorder of the hole system. Note that as the product of the Fermi wave vector and mean free path in a quasi 2D system is given by $k_F l = (h/e^2)G/\eta = (25812/\eta)R^{-1}$ (G and R are the sheet conductance and resistance, respectively, and η is a degeneracy factor) the hole system is not a good metallic conductor ($k_F l >> 1$) at any density of Fig. 4-5 [see also Fig. 4-4 (b)]. This makes the system at hand somewhat challenging from theoretical point of view. regime is reached in the lower right

corner of Fig. 4-4 (a). The behaviour of the

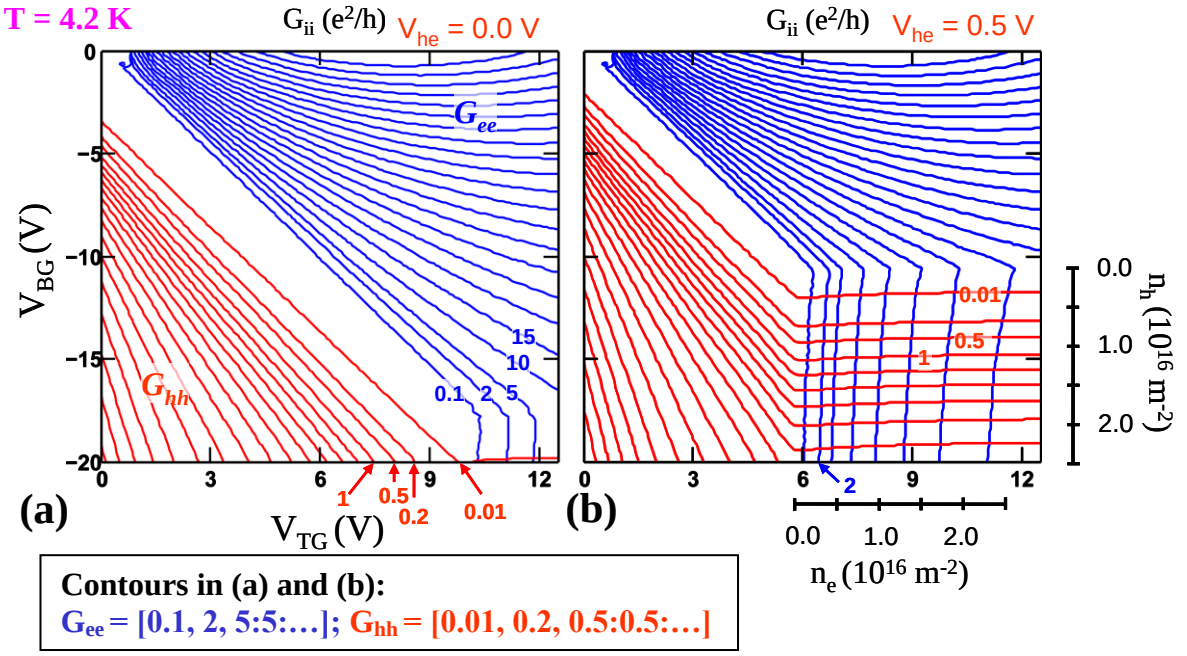


Fig. 4-4:* Contour plot of *experimental electron G_{ee} and hole G_{hh} conductivities at (a) V_{he} = 0 and (b) V_{he} = 0.5 V (T = 4.2 K). Blue (red) contours correspond to electrons (holes). Contours are in quantum units e^2/h. Contour spacing is given in the legend. Values of few contours are indicated. The extra outer axis in (b) show the electron n_e and hole n_h densities in the bilayer regime.

However, we note that still the drag resistance R_{he} follows *some* of the typical trends that have been observed in high mobility systems. For example, at any temperature *T* the drag resistance R_{he} decreases as a function of *n* and above $n \sim 6\times10^{15}$ m^{-2} R_{he} increases as a function of *T*. Furthermore, at the highest carrier densities between T ~ 20 – 100 K R_{he} follows roughly the T^2 power law, which is the expected temperature dependency for direct Coulomb interaction in metallic Fermi systems. Above 100 K R_{he} falls clearly behind from the T^2 trend. This deviation from the T^2 law is again an expected feature as at the elevated temperatures the thermal energy exceeds the Fermi level of the 2D carriers. Most striking feature in the R_{he} data is the saturation at low T at $n = 7.0\times10^{15}$ m^{-2} and the change in the temperature coefficient when $n < 7.0\times10^{15}$ m^{-2}. These effects can be linked to the R_{ee} temperature dependency: at $n_e \sim 6\times10^{15}$ m^{-2} starts to show insulating behaviour and this is reflected also in R_{he}.

In summary, we have demonstrated and explored coupled electron and hole transport in a single 22 nm-thick double-gated Si quantum well. This novel system is a strongly disordered indirect band gap electron-hole bilayer. Our device geometry provides good independent contacts to the electron and hole systems inside the well and interlayer gating up to 0.5 V (below 200 K) can be utilized to improve the transport properties of he bilayer system. In our previous work in SUBTLE we investigated room temperature transport properties of such Si well. Here we reported on detailed bilayer transport properties between 4.2 – 200 K. The temperature coefficient of the electron-hole drag resistance shows an intriguing behaviour as a function of the carrier density: at low densities the temperature coefficient can be negative. We link this effect to the disorder of the carrier system and, especially, to the insulating behaviour of the electron gas in this density regime. The theory for the system is lacking at the moment and pursue of the theoretical description of the disordered electron-hole bilayer system will be our next step.

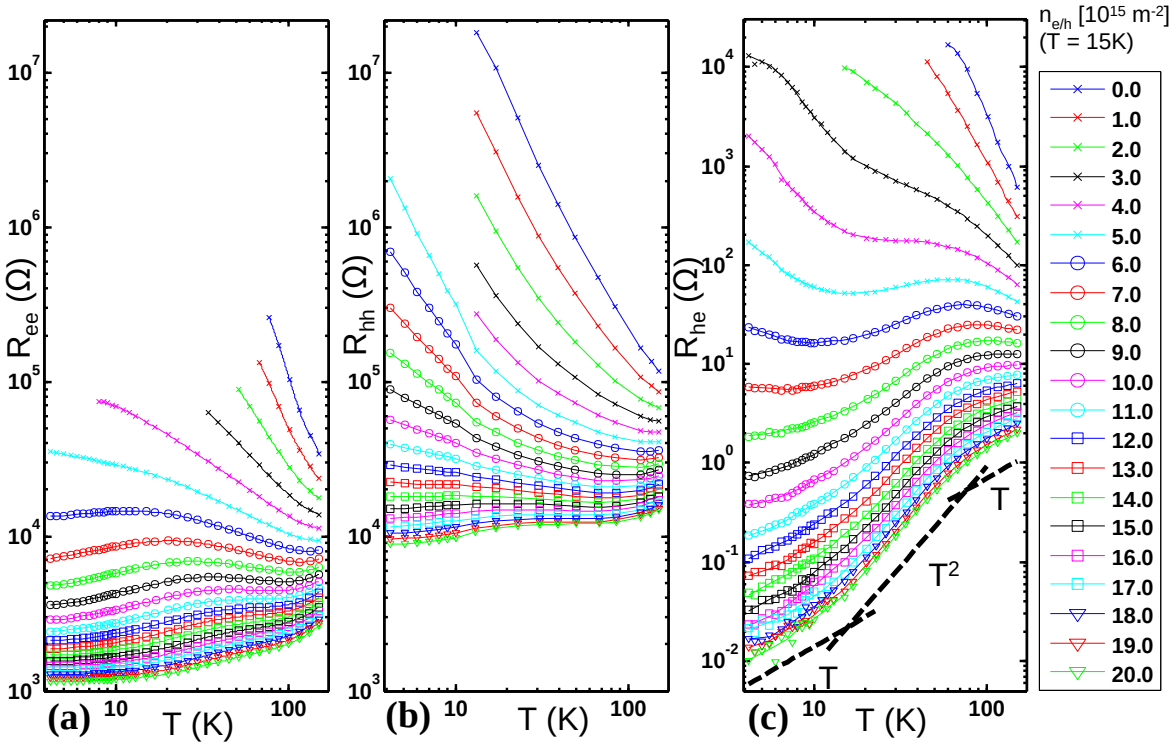


Fig. 4-5: (a) Electron layer sheet resistance, (b) hole layer sheet resistance and (c) the drag resistance as a function of temperature at different balanced carrier densities n_e=n_h. The carrier densities are indicated in the legend and they are measured at 15 K. The n_e=n_h=0 double gate voltage bias is obtained by extrapolation. Interlayer bias V_{he} = 0.5 V.

Coupled Resonant Tunneling Diodes (RTDs)

Here, we present studies on three-terminal RTD mesas with two drain contacts separated by a central trench. These TTRTDs operate with peak-to-valley (PTV) ratios up to 3.5 at room temperature. The TTRTDs are driven in a noise activated dynamically biased Geiger mode by exploiting the bistable switching in the region of NDR. In this regime nonlinear inverted or non-inverted sub-thermal gain is found.

The basis of the TTRTDs is an AlGaAs double barrier structure (DBS) grown by molecular beam epitaxy. A sketch of the layer sequence is illustrated in Fig. 4-6 (a), top part. On a 600 nm thick n-doped GaAs substrate, with a dopant concentration of n = $1*10^{18}$ cm^{-3}, a 100 nm thick GaAs layer with n = $1*10^{17}cm^{-3}$ was grown. 15 nm thick undoped GaAs buffer layers and 3 nm thick undoped $Al_{0.6}Ga_{0.4}As$ double barrier layers sandwich a 4 nm thick undoped GaAs quantum well. Then a 100 nm thick GaAs layer with n = $1*10^{17}$ cm^{-3} and another 200 nm GaAs layer with n = $1*10^{18}cm^{-3}$ form the top. Afterwards electron beam lithography and dry-chemical etching were applied to define the TTRTDs. An area dependent etching rate was exploited to implement the central trench. By a variation of the width in the etching mask, it was possible to realize central trenches which either cut through the double barrier or have a valley which lays on top of the DBS. The width of the trench is circa 100 ± 10 nm for RTD mesas diameters ranging from d = 1.8 µm down to 600 nm. Finally, gold contacts were vapor-deposited at the drain branches. The bottom of Fig. 4-6 (a) shows different electron microscopy images of TTRTDs. The current through each branch was determined by the voltage drops along load resistors R_{LB} and R_{RB} as depicted in Fig. 4-6 (b). However, different input-output characteristics of the TTRTDs were obtained and interpreted in terms of the depth of the central trench.

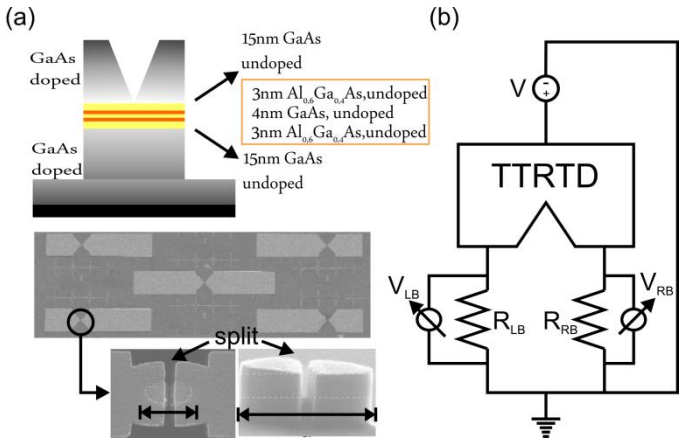


Fig. 4-6: (a) Top: Sketch of the layer sequence of the TTRTD with its two split separated drain contacts. Between the heavily doped GaAs drain and source contact layers and 15 nm thick GaAs buffer layers, 3 nm thick $Al_{0.6}Ga_{0.4}As$ double barriers sandwich a 4nm thick GaAs quantum well. Bottom: Electron microscopy images of TTRTDs. (b) Measurement circuit diagram

Fig. 4-7 shows the current voltage characteristics for two different TTRTDs with a diameter size d = 800 nm. For TTRTD N°1 in Fig. 4-7 (a) and TTRTD N°2 in Fig. 4-7(b) resistance ratios of $r_1=R_{RB}/R_{LB}=100\Omega/100\Omega=1$ (left part) and $r_2=R_{RB}/R_{LB}=1k\Omega/100\Omega=10$ (right part) were applied to analyze the depth of the central trench. A close inspection of TTRTD N°1 shows that the peak currents of the left branch I_{LB} and the right branch I_{RB} change, when the resistor ratio changes from r_1 to r_2. Obviously, the current in the right branch (RB) decreases as the resistor value increases from R_{RB} = 100 Ω to R_{RB} = 1000 Ω. This points toward the fact that for TTRTD N°1 the central trench stops before the double barrier structure (DBS) (see insert sketch). Both branches are thus connected to the same source and drain contacts. As a consequence, the current in each branch is approximately inversely proportional to the resistance. The total resistance in each branch can be described by R_{total}, where R_{total} is the sum of the intrinsic resistance R_{int} = 8.4 kΩ for the left and R_{int} = 13.0 kΩ for the right branch and the load resistance $R_{RB,LB}$, with $R_{total} = R_{int} + R_{RB}$.

On the contrary, TTRTD N°2 shows a different behavior. In this case the peak currents remain almost the same for a variation of r_1 (left) to r_2 (right). Instead, the peak voltage shifts due to a change of r_1 to r_2 with $V_{LB}(r_2) - V_{RB}(r_2) \approx 180$ mV. This indicates that the trench cuts through the DBS for TTRTD N°2. Both branches are thus only connected to the same source contact, but not to the same drain contact. Different branches behave therefore as independent RTDs. The peak voltage shift can be directly related to the load-line effect.

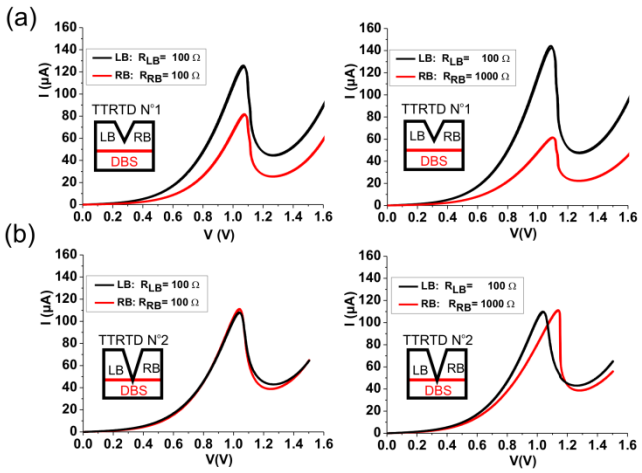


Fig. 4-7: Output current I versus input voltage V for the left (LB) and the right branches (RB) of TTRTDs with a diameter of d = 800 nm. (a) TTRTD N°1 with the central trench stopping before the double barrier structure (DBS). The peak current differ dependent on the resistance. Whereas the peak voltages of different branches are almost identical. (b) TTRTD N°2 with the central trench cutting through the DBS. The peak currents of the different branches are similar, but the peak voltages depend now on the serial resistance.

Such two different etching depth profiles of a TTRTD lead to different input-output responses, if biased as sketched in Fig. 4-8 (a). For this experiment, one branch is used as a control branch with voltage V_2. The voltage V_1 on the other branch was used to set the working point of the TTRTD. In Fig. 4-8 (b) the output-input characteristic of a TTRTD with diameter d= 800 nm is shown. In addition to the dc voltage V_1, a time dependent, sinusoidal signal with amplitude V_{AC} and frequency f is applied. By tuning of V_1, the TTRTD is set close to the threshold transition V_{up} from the low state (valley) to the high state (peak). In the starting configuration the periodic signal does not reach the transition value. The mean of the system output is <V>=V_L. By varying now the input voltage V_2 from 0 to 30 mV noise activated spikes are generated. This is demonstrated in Fig. 4-8 (c). Whenever the periodic signal touches the threshold value, a transition from V_L to V_H is initialized. It is also shown that for increasing input voltages V_2 the number of generated spikes increases significantly. Interestingly, the transconductance of the TTRTD, defined as $g = \frac{\partial < I >}{\partial V_2}$, with <I> the mean of the current, can reach values which are not directly limited by the inverse of the thermal energy with:

$$\frac{g_{\max}}{< I >} = \frac{\alpha}{\sigma} >> \frac{e}{kT}. \qquad (1)$$

σ denotes the standard deviation of the noise floor, which is caused by shot noise and was determined to be σ= 1.3 mV. α is a system dependent parameter.

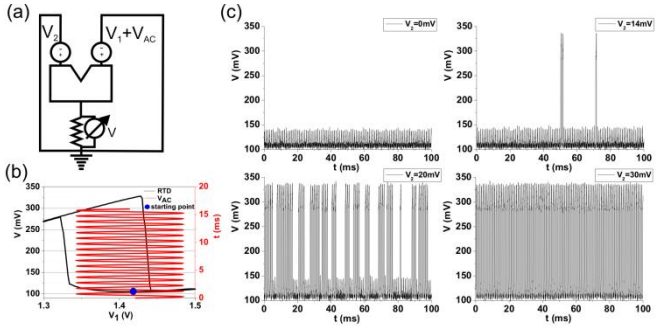


Fig. 4-8: (a) Measurement circuit diagram. The working point voltage V_1 and the time periodic signal with amplitude V_{AC} and frequency f is applied to one branch. The second branch is used as a control branch and the output voltage is measured over

the load resistor. (b) V_1 and the periodic signal are tuned so that the TTRTD is set close to the transition to the high state and spike-like signal trains can be generated. (c) Signals of TTRTD N°2 for different input voltages V_2. A significant increase of noise activated spikes is obtained for V_2 ranging from 14 mV to 20 mV.

In Fig. 4-9 the mean current <I> as a function of the input voltage V_2 (squares) of TTRTD N°1 in Fig. 4-9 (a) and TTRTD N°2 in Fig. 4-9 (b) is shown. For TTRTD N°1 the amplitude of the periodic signal is V_{AC} = 69 mV, the frequency is f=10kHz and the load resistor is R=500Ω. This TTRTD exhibits an inverted response to the input voltage V_2. Up to V_2 = - 4 mV the system output of the TTRTD is in the low state with a mean current output of <I>= 230 µA. However for input voltages exceeding V_2 = - 20 mV, a spike occurs in almost every cycle of the periodic forcing and the output current is <I>= 380 µA. Between these voltages, a nonlinear inverted transfer function occurs. In this intermediate case, noise activated spikes lead to absolute transconductance |g/<I>| (circle) values exceeding the thermal limit. For direct comparison, the thermal limit g_{Limit}/<I> ≈ 40 (1/V) (line) at RT is also shown in Fig. 4-9. The maximum transconductance of the TTRTD N°1 is |g/<I>| ≈ 82 (1/V). In Fig. 4-9 (b) the output-input characteristic of TTRTD N°2 is shown. With an amplitude of the periodic forcing V_{AC}= 41 mV, the frequency f= 10 kHz and a load resistor R = 1kΩ. This TTRTD shows a non-inverted characteristic. The absolute maximum transconductance value |g/<I>| (circle) was determined to |g/<I>| ≈ 82 (1/V).

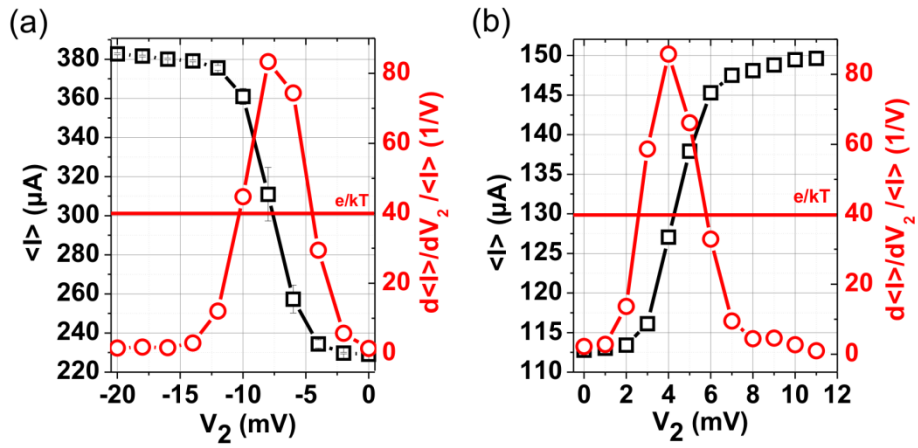


Fig. 4-9: Mean value <I> of the current (squares) and transconductance per <I> (circle) versus V_2. (a) For TTRTD N°1 <I> is an inverted function of the input voltage V_2 (squares). Also plotted is |g/<I>| (circle) and the thermal limit e/kT (line). TTRTD N°1 exhibits a maximum of |g/<I>| ≈ 82 (1/V). (b) Non-inverted <I> (V_2) characteristic of the TTRTD N°2 with a maximum of |g/<I>| ≈ 82 (1/V).

4.2.2 Task 3.2 – Tailored electrochemical capacitance feedback FETs

Bistable electron-hole gating

One of the objectives of the SUBTLE project was to explore different materials and systems that could be utilized in realization of bistable feed-back field-effect-transistors (FBFETs). Bilayer carrier systems in GaAs and Si represent one possible basis where bistable gating can occur. Memory effects were proposed to appear if these bilayer devices are operated by controlling the single layer drive current by inter-layer gating. Our preliminary results were reported in deliverable D3.2, where we experimentally demonstrated that the electron-hole (EH) bilayer system in Si quantum well (see Fig. 4-10) poses a bistable gating effect. The bistable switching occurred when the electron layer drive current was adjusted by the hole layer voltage close to depletion of the hole layer. During 2009 we have performed intensive experimental test to different devices. We have explored the bistable effect as a function

external gate biases, drive voltage and temperature. The main results are reported and discussed below.

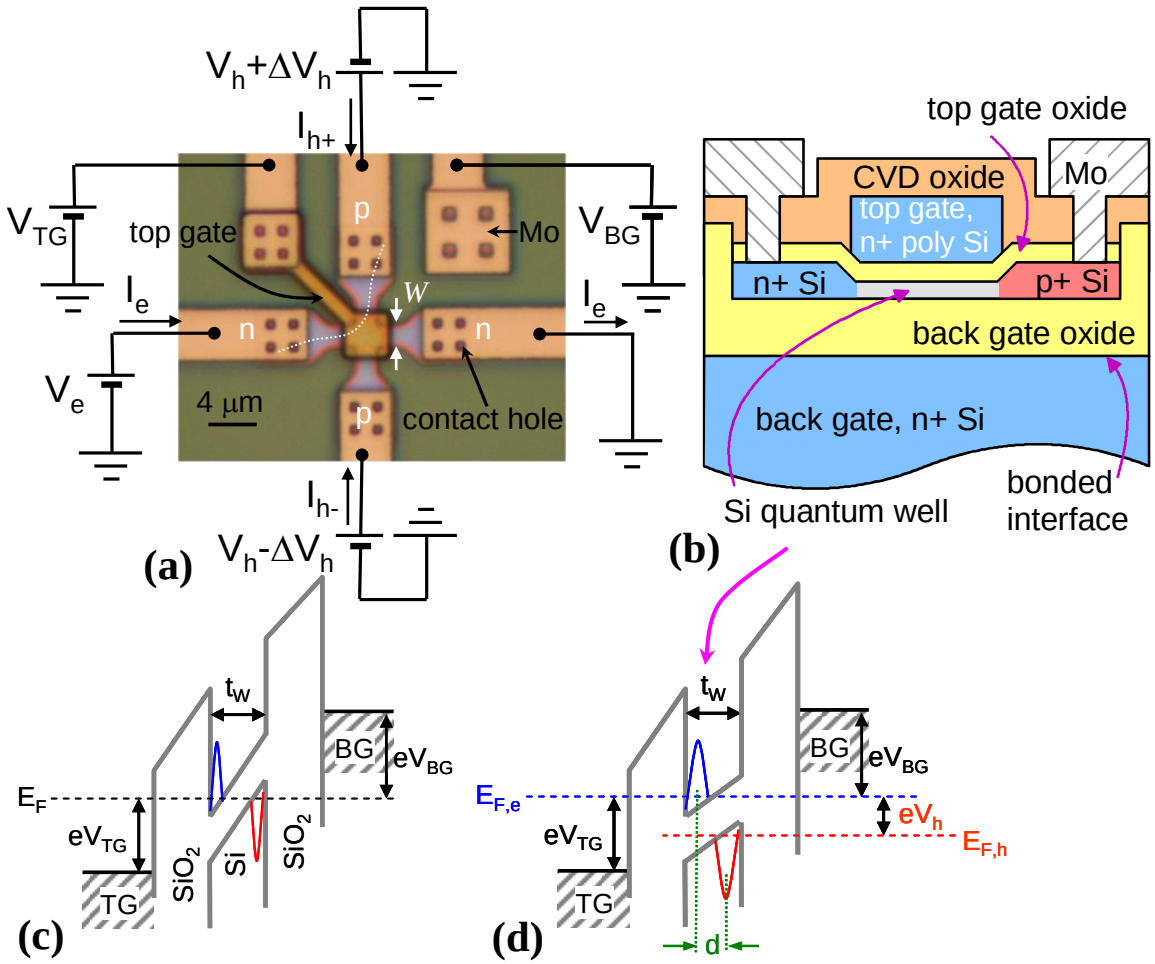


Fig. 4-10: (a) Optical micrograph of Si EH bilayer device with W = 2.0 μm and illustration of biasing in the experiments. The letters n and p on the Mo metal refer to the type of Si the particular Mo pad is connected to. (b) Schematic cross-section along the dashed line in (a). (c) Illustration of energy band diagram of the Si quantum well channel. Electrons (blue) and holes (red) are introduced into the channel by positive top gate (TG) voltage V_{TG} and negative back gate (BG) voltage V_{BG} together with inter-layer voltage V_{IL}. In the experiments the Si quantum well channel thickness t_W is ~20 nm. The top gate oxide thickness t_{OX} and buried (or back gate) oxide thickness t_{BOX} are 50 nm and 82 nm, respectively.

The EH Si structures were fabricated utilizing the methods described in D2.2 report. Optical micrograph of the sample geometry explored here is shown in Fig. 4-10 (a). Fig. 4-10 (b) shows a schematic cross-section of the device. Band diagrams at different interlayer voltages are depicted in Fig. 4-10 (c) and Fig. 4-10 (d). Fig. 4-10 (a) also shows the biasing scheme of the experiments. The electron layer bias is set to a constant value V_e while the hole layer bias V_h is adjusted in order to capacitively gate the electron layer. If the electron channel is driven into nonlinear regime and saturation then the effective V_h depends on the position along the electron layer. Note that positive V_h increases carriers in both layers and decreases the interlayer distance d. Negative V_h has the opposite effect. We add a small DC push-pull voltage V_h = 1 mV, which enables monitoring of the hole layer conductance G_{hh} by comparing the current components I_{h-} and I_{h+}. The conductance is given by $G_{hh} = I_h/V_h$, $I_h = (I_{h+} - I_{h-})$.

Fig. 4-11 (a) shows electron layer current and hole layer current (conductance) at drive bias of V_e = 1.0 V (T = 77 K) as a function of the external gate voltages. After extensive investigations we found that the bistability is observed only if the electron layer current switches between finite values. We could not observe any bistable switching close to $n_{e,h}$ ~ 0 threshold. The double gate bias region where the bistability is present is indicated in Fig. 4-11 (a). Fig. 4-11 (b) shows an example of the bistable EH switching, where $I_h \propto G_{hh} \propto n_h$ switches from zero to a positive value with simultaneous jump in I_e when V_h is swept up. If V_h is swept down we see the opposite behavior, but with I_e and (I_{h+} - I_h) down switch occurring at lower V_h bias giving a small hysteretic loop. The bistable effect in I_h is brought out more clearly in the data of deliverable D3.2. Here the main focus is on the electron layer current and as the measurements involve extremely large parameter space (gate voltages, layer voltages, temperature) the hole layer current is measured with less filtering, which reduces the measurements time but increases noise in the I_h data. Note that the leakage current (I_{h+} + I_h) between the electron and hole layers is negligible in the bias range of Fig. 4-11: finite inter-layer leakage appears above $V_h \approx 0.6$ V (see Fig. 4-2). The electron layer driving bias dependency of the EH switching at T = 77 K is shown in Fig. 4-12. The bistability is present above V_e ~0.825 V.

The temperature dependency of the bistable EH switching has been investigated in temperature range 77 – 300 K. Fig. 4-13 shows the main results of these measurements. The I_e-V_h curves at different temperatures are shown in Fig. 4-13 (a) and Fig. 4-13 (b) shows the temperature dependency of the bistable loop *L*. The loop shows a sudden drop at ~ 105 K and below T ~ 105 K it follows an thermally activated behavior

$$L \propto \exp\left(\frac{E_a}{k_B T}\right)$$

with activation energy E_a = 29 meV. The hole layer current I_h and conductance shows a similar behaviour with an activation energy of ~ 30 meV (not shown).

At this point we summarize our explorations on the bistable EH gating:

(a) Gating layer (hole) density switches from zero to a finite value at the switching bias.
(b) Bistability requires clearly finite electron (drive layer) density for on (high current) and off (low current) states.
(c) Bistability requires large electron layer driving bias.
(d) The bistability is clearly present below 105 K and shows a thermally activated behaviour with activation energy of 29 meV (V_e = 1.0 V).
(e) Above T ~105 K the activation behaviour is lost.

From item (b) it follows that we cannot obtain a very large on-off current ratio $I_{e,on}$ /$I_{e,off}$. One of our motivations to explore a massive parameter space (voltages and temperature) was to see whether this condition could be relaxed. However, in the light of the current data item (b) seems to be a fixed rule. Note that the data of Fig. 4-11 (b) suggests that the effect follows from a memory effect in the gating (hole) layer density (see also deliverable D3.2). The detailed physical mechanism of the observed bistable EH gating is not clear. However, note that the collisional broadening is relatively high in the EH bilayer.

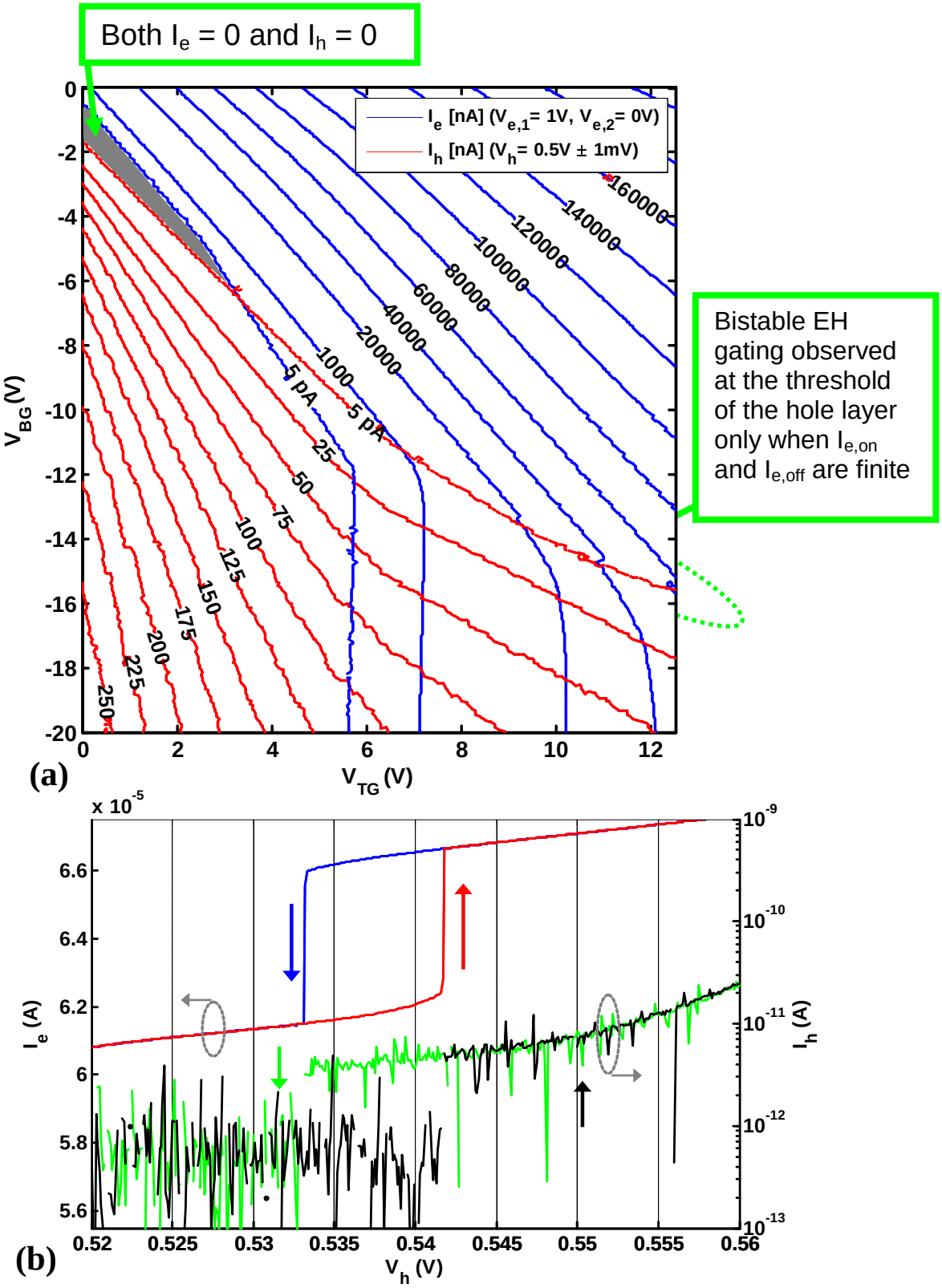


Fig. 4-11: (a) Contour plot of electron layer current I_e (red) and hole layer current I_h = I_{h+} - I_{h-} (blue). The drive bias for the electron layer is V_e = 1.0 V. (b) Electron layer current (left axis) and hole layer current I_h = I_{h+} - I_{h-} (right axis) as a function of gating hole layer voltage V_h at V_{TG}=12.3V, V_{BG}=-14.8V. The measurement configuration is depicted in Fig.4-10 (a). The temperature is 77 K and the channel width is W = 1.0 μm. The up and down arrows indicate the V_h sweeping direction.

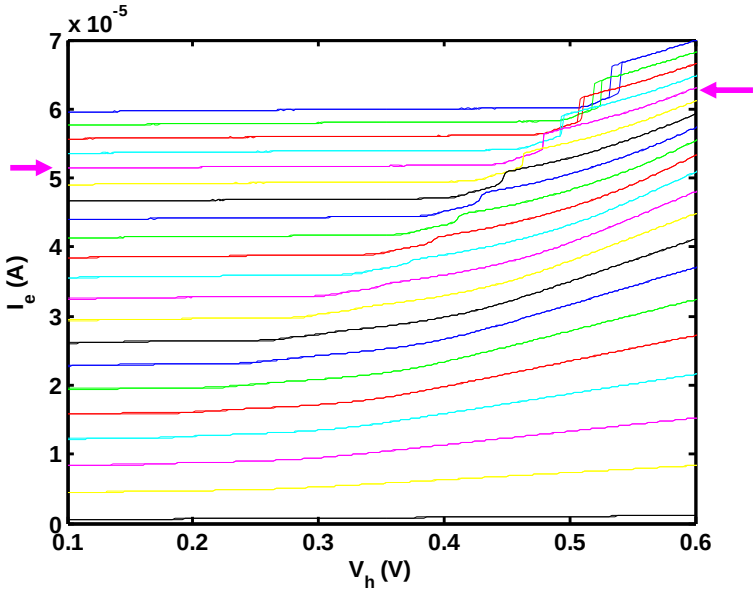


Fig. 4-12: Electron layer current as a function of gating hole layer voltage V_h at different driving bias V_e values. V_e = 0.05 - 1.0V (step 50 mV). Bistability disappears around V_e = 0.825 V (indicated by the arrows). The temperature is 77 K and the channel width is W = 1.0 μm.

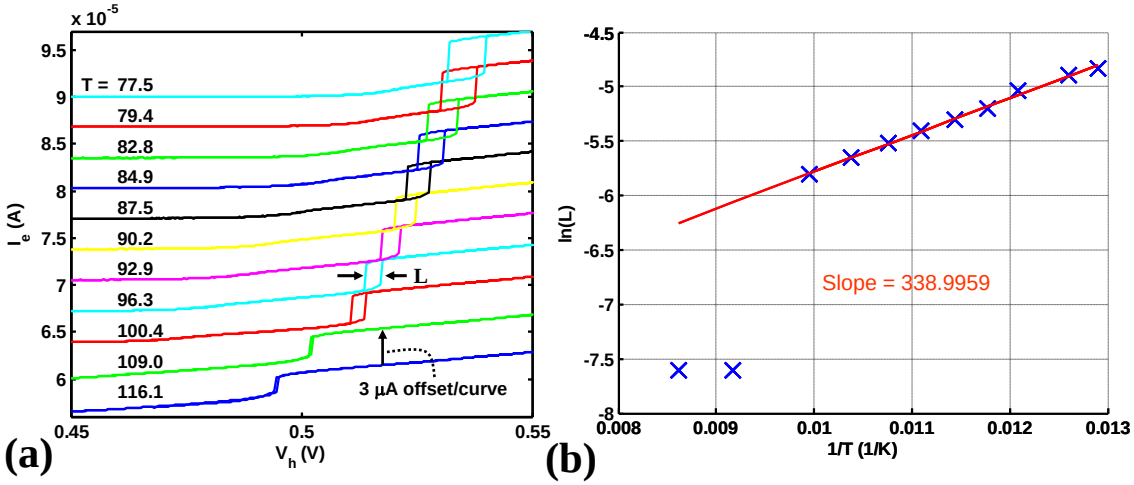


Fig. 4-13: (a) Electron layer current as a function of gating hole layer voltage V_h at different temperatures. V_e = 1.0 V. (b)Temperature dependency of the bistable loop voltage L. The fitted slope above 105 K gives an activation energy E_a = 29 meV.

On the other hand as shown in the transport studies in the linear response regime (see, e.g., Fig. 4-4) the interlayer gating strongly affects the disorder of coupled carrier system. The intralayer scattering is especially strong in the hole layer and at low hole densities the hole sub-system is actually in the limit of strong localization and activated transport. On the other hand positive interlayer bias V_h reduces the interaction with the SiO_2 layer and, therefore, creates delocalization. At same time the positive V_h increases the EH interaction by reducing interlayer distance. Furthermore, as shown in Fig. 4-5 (c) the EH drag resistance can have extremely large values at low carrier densities. It maybe that these three effects (delocalization, enhancement of EH interaction and drag) play an important role in the bistable EH switching. We are obviously dealing with a very complicated physical system and

we conclude that the intriguing bistable EH switching will require theoretical investigations that are beyond the scope of this project.

4.2.3 Task 3.3 – Novel nanodevices

Coupled quantum dot FETs with integrated charge detectors in InGaAs/InP 1: gating

Double quantum dots are regarded as artificial molecules. Depending on the interdot coupling, two QDs can form ionic-like or covalent-like bonds. For integrated nanoelectronic circuits, electrostatically coupled quantum dots can be used for logic gates, as well as for quantum dot cellular automata (QCA). Another interesting direction involves stochastic resonance studies. If the electron number on dot 1(2) is $N_{1(2)}$, the charge state of the system can be denoted (N_1, N_2). For isolated double dots, (M, N) and (M-1, N+1) form bistable states. Therefore, an appropriate noise level can help trigger the electron to jump back and forth between the two dots, and the position of the jumping electron can be sensed by integrated charge detectors. The stochastic resonance in double QDs is expected to be useful in weak signal detection as well as basic physics research. Moreover, double quantum dots are candidates for building-blocks in so-called quantum computation. In principle, any two-level quantum system can be used as a quantum bit (qubit). In the coupled double QDs, an electron spin on each dot is proposed to be a qubit. By temporarily coupling the two spins, entanglement of the qubits can be achieved. For certain tasks, a quantum computer is much more efficient than its conventional counterpart. Based on our technology development, coupled QD FETs with integrated charge sensors in InGaAs/InP have been successfully realized and measured at 300 mK.

Fig. 4-14 portrays a SEM image of a fabricated double quantum dot device together with the measurement circuits. The HfO_2 film was 30 nm thick and grown at 100 ^oC followed by lift-off. Six ohmic contacts were created from 200 nm of annealed Au/Ge and eight top gates of 50 nm Ti/Au. The diameter of the QDs was approximately 150 nm. A symmetric DC bias was applied to the source and drain of the double dot with the voltage on S_{QD} being $-V_{sd}/2$ and the voltage on D_{QD} being $V_{sd}/2$. The upper, left, left plunger, lower, right plunger and right gates of the double QD were applied with voltages V_u, V_l, V_{pl}, V_d, V_{pr} and V_r, respectively. Two quantum point contacts (QPCs) were also integrated into the device as charge sensors. The

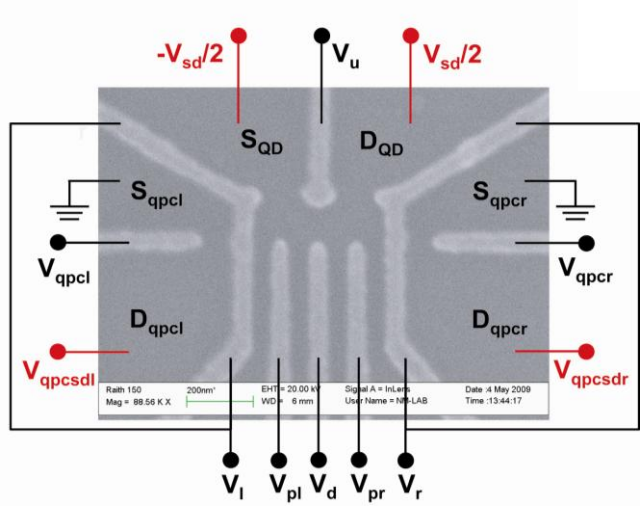


Fig. 4-14: A SEM image of the double quantum dot device. The scale bar is 200 nm. Two QPCs were fabricated near the dots, and served as charge sensors. The DC measurement circuits are also schematically drawn.

QPCs were coupled to the double QD via the left and right gates. In order to reduce the noise from the cross-talking effect, the QPCs had separate sources and drains from the double dot, in contrast with the commonly used design. The two ends of the left (right) gate were connected on chip. The other gate of the left (right) QPC was named the left (right) QPC gate and applied with voltage V_{QPCl} (V_{QPCr}). The source contacts of the QPCs were

grounded and the drain contacts were applied with a DC bias V_{QPCsdl} and V_{QPCsdr}. All of the following experiments were performed at 300 mK in a ^{3}He-based refrigerator.

Electrically, the devices were very stable and displayed good reproducibilities, allowing measurements for very large gate voltage ranges without any significant charge rearrangement (usually a measurement takes several hours or days). Fig. 4-15 shows a measured charge stability diagram of the device from Fig. 4-14 in the linear response regime. The device was measured at V_{sd}=50 μV, V_u=-1.63 V, V_l=-1.49 V, V_d=-1.93 V and V_r=-1.8 V, where the honeycomb was very clear. The two QPCs were temporarily not in use. The current through the double dot I_{sd} was plotted against two plunger gate voltages V_{pl} and V_{pr}. Typical hexagonal features were observed. Theoretically, for completely decoupled QDs (i.e., without quantum mechanical tunneling between the two dots), changing the voltage on one dot's plunger gate will not influence the charge on the other dot. Hexagons appear when the interdot coupling is increased. In the extreme case, the coupling is so large that the two smaller dots emerge into one big dot. The data in Fig. 4-15 represent an intermediate interdot coupling. The tunnel barriers are transparent enough to allow for a current, and are opaque enough for defining the number of electrons on each dot. Ideally, the only places where the current is not zero are at the triple points at the hexagon corners, where the electrons can tunnel through both QDs. These triple points are the only areas where three charge states, for instance, (M, N), (M+1, N) and (M, N+1), become degenerate. At the triple points, the electrochemical potentials of the two dots are both aligned to the Fermi level of the source and drain of the double dot, and we have $\mu_s=\mu_l(M+1, N)=\mu_r(M, N+1)=\mu_d$. In the stability diagram, the triple points ideally form square lattices. Nevertheless, with finite cross capacitances (i.e., the capacitance between one dot and the plunger gate of the other dot), the positions of the triple points move to lower $V_{pl(pr)}$ for increasing $V_{pr(pl)}$.

In Fig. 4-15 , the borders of the hexagons are also current peaks. At these boundaries, the electrochemical potential of one dot is aligned to the source or drain Fermi sea (μ_l to μ_s or μ_r to μ_d) while the other dot's electrochemical potential is misaligned to μ_s or μ_d. Transport can take place through co-tunneling via a virtual state. Co-tunneling processes are higher-order tunneling events requiring a finite tunnel coupling between the two dots. It is possible to extract information of the capacitances of the device from the geometry of the hexagon cell. Similarly to what was mentioned in the previous section, the plunger gate capacitances are related to the dimensions of the honeycomb cell through $C_{pl(pr)}=e/\Delta V_{pl(pr)}$.

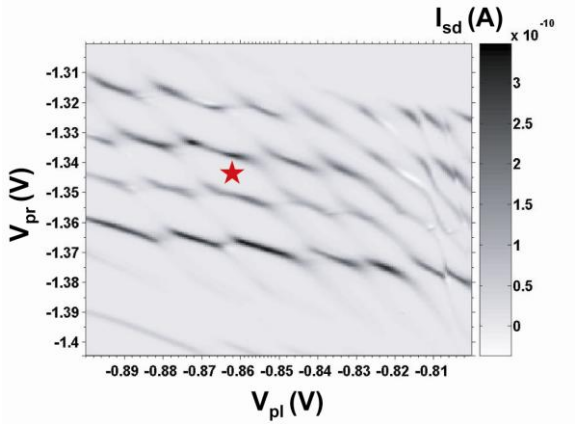


Fig. 4-15: An experimental stability diagram of the double dot device shown in Figure 5 measured at 300 mK. The source-drain current I_{sd} of the QDs is plotted at various plunger gate voltages V_{pl} and V_{pr}. The data was recorded in the linear response regime with V_{sd}=50 μV. Clear honeycomb structures were observed, and for the hexagon marked with a red star, $\Delta V_{pl} \approx 0.0185$ V and $\Delta V_{pr} \approx 0.014$ V.

For example, in Fig. 4-15 , from the size of the cell marked with a red star, one obtains $C_{pl} \approx$ 8.65 aF and $C_{pr} \approx$ 11.4 aF. These values may however be underestimated due to the double dot probably not being in the many-electron regime.

Since the 1990s, QPCs have been widely used to detect the charge states in quantum dots. At appropriate working points, typically between two quantized conductance plateaux, the conductance of a QPC sensitively depends on the electrostatic potential that the QPC feels.

Therefore, if a QPC is placed near a QD, it can noninvasively detect single electron events in the QD. Fig. 4-16 shows the curves used to determine the proper QPC working areas. In the left (right) figure, the source-drain current of the left (right) QPC $I_{QPCsdl(QPCsdr)}$ is plotted as a function of the left (right) QPC gate voltage $V_{QPCl(QPCr)}$. The curves are measured under the configuration V_{sd}=50 μV, V_{QPCsdl}=V_{QPCsdr}=100 μV, V_u=-1.75 V, V_l=-1.5 V, V_r=-1.67 V, V_d=-2.15 V, V_{pl}=-0.78 V and V_{pr}=-0.98 V. For the left-hand figure, V_{QPCr}=-1.7 V, and for the right-hand figure V_{QPCl}=-1.975 V. Generally speaking, the QPC current becomes reduced with a decreasing gate voltage. The QPC detectors should work at the points where the curves in Fig. 4-16 were relatively steep: -2.05 V <V_{QPCl}<-1.95 V and -1.77 V <V_{QPCr}<-1.67 V.

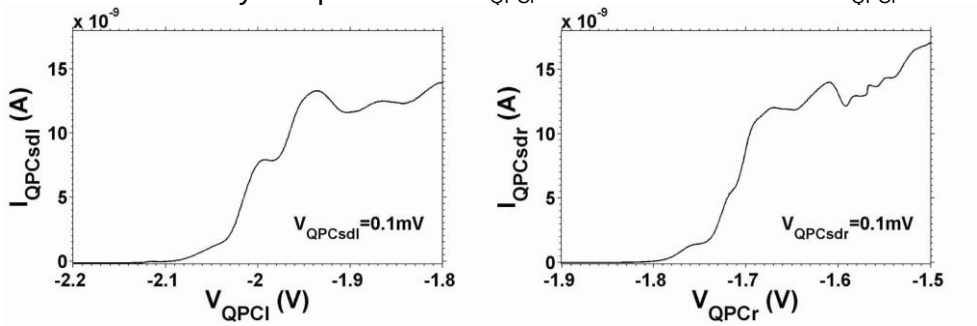


Fig. 4-16: Left: The DC current through the left QPC plotted against the changing voltage V_{QPCl} on the left QPC gate. Right: The DC current through the right QPC plotted against the changing voltage V_{QPCr} on the right QPC gate.

Fig. 4-17 presents the data of the charge-sensing measurement. The device operated at V_{sd} = 50 μV, V_{QPCsdl} = V_{QPCsdr} = 100 μV, V_u = -1.75 V, V_l = -1.5 V, V_r = -1.67 V, V_d = -2.15 V, V_{QPCl} =-1.975 V and V_{QPCr} = -1.7 V, in correspondence to the working points in Fig. 4-16. While selecting the operating point of the device, V_l and V_r should not be more positive than ~-1.5 V, otherwise the electrons can jump between the QPC parts and the QD parts. On the other hand, V_l and V_r cannot be too negative either, since a reasonably strong capacitive coupling between the QPCs and the QDs is required. The left part of Fig. 4-17 depicts the stability diagram of the double QD, where many hexagonal cells are seen. The middle figure is the signal from the left QPC, where the transconductance of the QPC $\partial I_{QPCsdl}/\partial V_{pl}$ is plotted. In this way, the influence from the QPC's (nearly) linear current background is subtracted, and the steps in I_{QPCsdl} corresponding to a change in the electron number in the double QD are reflected by the negative peaks in the transconductance plot. As a result, a very clear response is detected in the left QPC. The right part of figure plots the transconductance $\partial I_{QPCsdr}/\partial V_{pl}$ from the right QPC. The changes in the electron number on the coupled QD FETs can also be clearly detected by the right QPC.

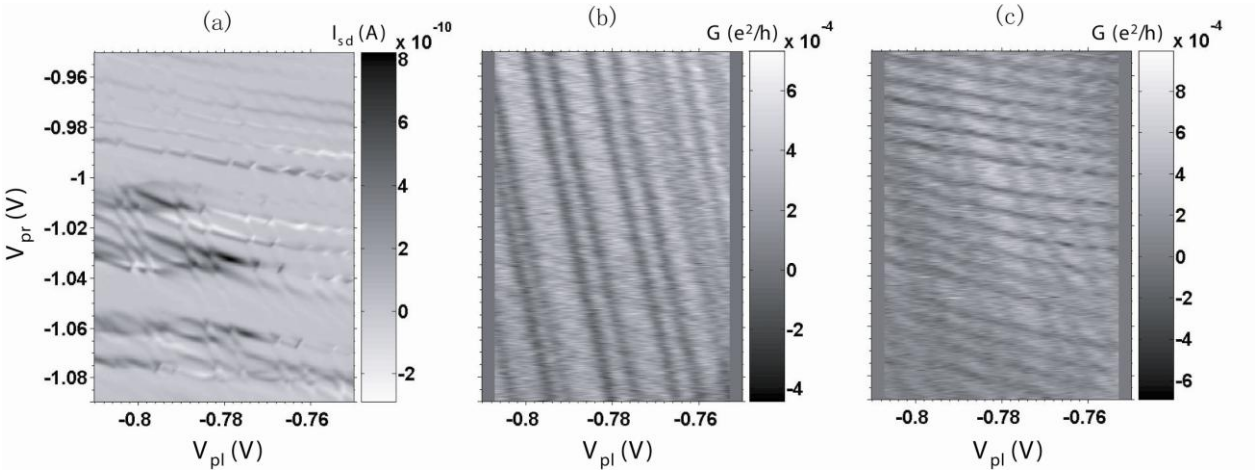


Fig. 4-17: Left: A charge stability diagram of the double dot. Middle: The left QPC charge-sensing signal. Right: The right QPC charge-sensing signal. The DC currents in the two QPCs are converted into transconductances with unit e^2/h. In this measurement, V_{pl} was swept while V_{pr} was stepped.

Coupled quantum dot FETs with integrated charge detectors in InGaAs/InP 2: gating + etching

Apart from the above-described technology route, the coupled quantum dot FETs with integrated charge detectors can also be realized by gating plus etching in InGaAs/InP. The material system used in our study has the same design as before, which is a HfO_2-$In_{0.75}Ga_{0.25}As$/InP heterojunction. The reason why we introduce etching in the technology is that the etched quantum devices have very well defined boundaries. Fig. 4-18 is the layout of a coupled QD FET made by this technology, where (a) is a SEM picture of the quantum dots and (b) is the corresponding schematic illustration. The devices are made by multi-step EBL. First, mesas with standard Au/Ge ohmic contacts were fabricated. Second, Ti/Au alignment markers were fabricated in order to align the structures in EBL. Third, quantum wires with integrated nearby QPC were chemically etched in a Br-based wet solution. The etching depth was about 100 nm, which reached the semi-insulating InP substrate. Fourth, HfO_2 isolation layer was grown at 100 ^oC by ALD followed by lift-off, which is the same technology described previously. The isolation layer covers the nanostructure part of the device. Finally, Ti/Au top gates (finger gates) aligned to the etched fine structures were achieved by EBL and thermal evaporation. Again, the cross-linked PMMA bridge technology was employed. In our devices, the finger gate pitch is around 80 nm. The QPC is intentionally not placed in the center position with respect to the double dot, since we want an asymmetric capacitive coupling of the QPC to the left and right dots, so that we can distinguish the charge states in the two dots. In Fig. 4-18 (b), it is seen that with the applied negative voltages on the gates, the 2DEG beneath is depleted (dashed line area), and coupled QD FETs are therefore formed (red dots).

The fabricated devices were measured systematically at low temperature in a dilution refrigerator. Spin physics and charge state sensing of few-electron single and double QDs were studied in detail. Fig. 4-19 shows the spin-1/2 Kondo effect in a single InGaAs/InP QD, where the single dot is formed by using the right-most 3 finger gates (see the SEM picture in Fig. 4-19). Other gates are not in use in this measurement. Fig. 4-19 (a) is the charge stability diagram of the QD measured with no applied magnetic field, where the channel differential conductance through the QD is plotted as a function of V_{sd} and the plunger gate

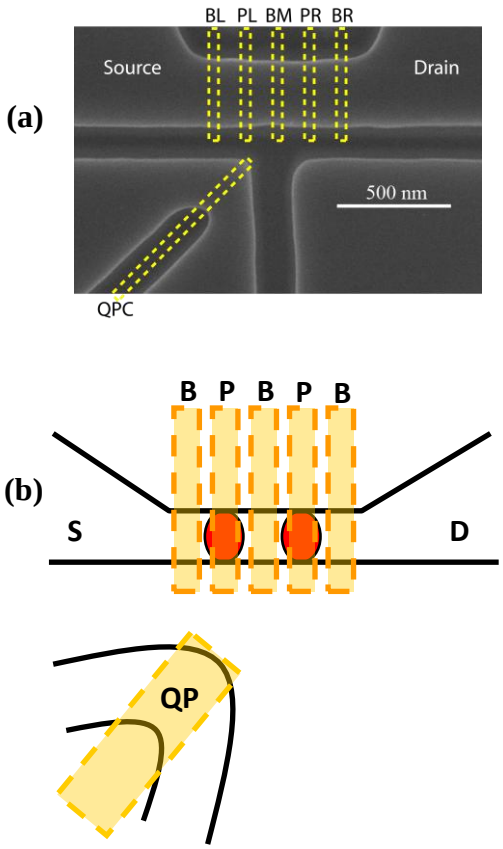


Fig. 4-18: (a) A scanning electron micrograph (SEM) image of the nanostructure part of the coupled QD FETs made in InGaAs/InP by gating + etching technology. The dashed lines correspond to the top Ti/Au gates. The scale bar is 500 nm. (b) A schematic diagram of the same device in (a), where the yellow parts are the finger gates whereas the red parts are the coupled QDs.

voltage. In the middle of the diamond, a clear line is observed. Fig. 4-19 (b) is the 1D plot at the cutline in Fig. 4-19 (a) (dashed line). A conductance peak is well resolved and the Kondo temperature is estimated to be 0.7 K. Fig. 4-19 (c) is the same diamond, but measured at a magnetic field of 3 T. Fig. 4-19 (d) is the 1D plot at the cutline in Fig. 4-19 (c), where the Kondo peak is seen to disappear at $V_{sd} = 0$ V (linear response regime). The Kondo effect in QDs is a higher-order tunneling event. An electron can tunnel through the dot via a classically forbidden virtual state. Therefore, we have a conductance peak in the Coulomb blockade regime. In the Kondo effect, the electron spin state in the dot is flipped after such a virtual intermediate state. While applying a magnetic field, due to Zeeman effect, the spin up and spin down states have different energies, and therefore the Kondo effect disappears at linear response regime.

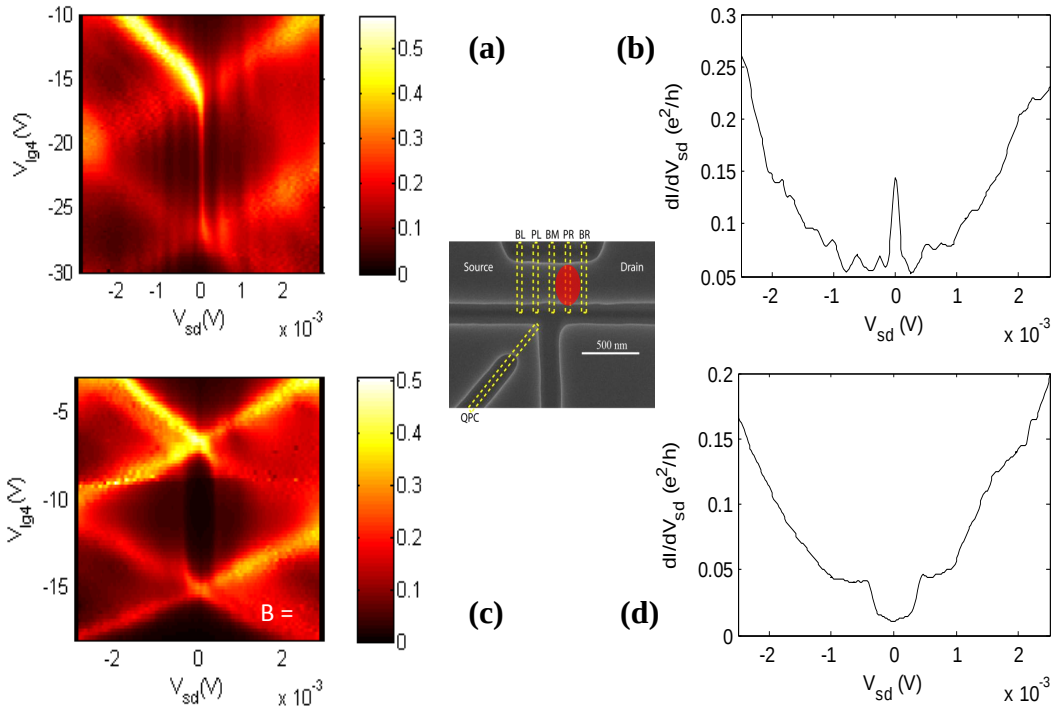


Fig. 4-19: (a) The stability diagram of the single QD with B=0T. (b) The plot at the cutline in (a). (c) The stability diagram of the dot at B=3T. (d) The plot at the cutline in (c). The SEM picture in the middle schematically shows the single dot formed by three gates.

Fig. 4-21 is the charge detection experiment of the coupled QD FET device. Fig. 4-21 (a) is the charge stability diagram of the QD, where the channel current through the double dot is plotted against two plunger gate voltages. Triple points are resolved, whereas at other areas the current is suppressed, indicating that the two dots are weakly coupled to each other. Fig. 4-21 (b) is the transfer properties of the QPC detector, showing the control of the QPC top gate voltage over the QPC current. The best working point is indicated by the arrow, where the transconductance is large. Tuning the device to work in this regime, nice detector signals can be achieved, which are demonstrated in Fig. 4-21 (c).

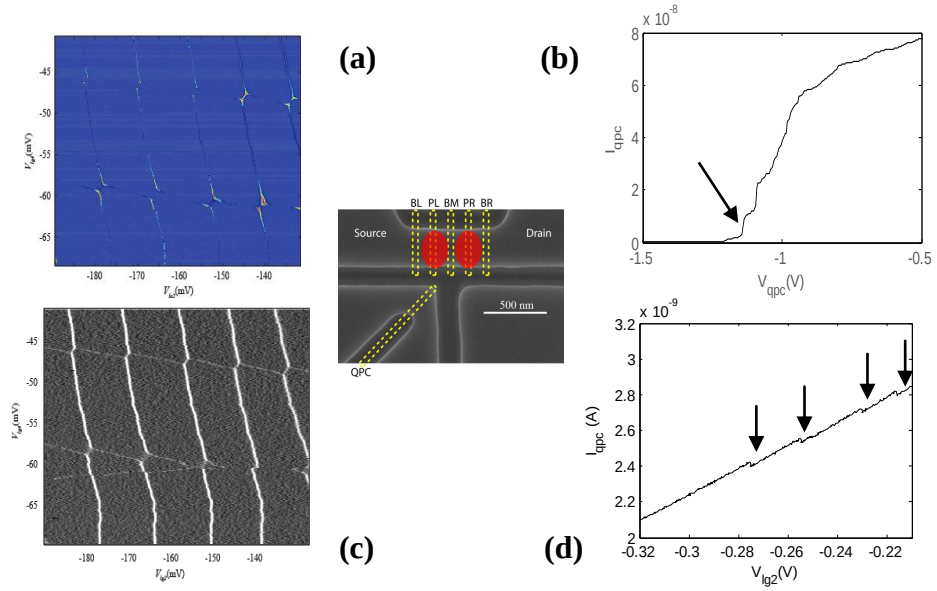


Fig. 4-20: (a) The stability diagram of the double QD. (b) The working point of the detector. (c) The corresponding detector signal. (d) The current jump in the QPC current. The SEM picture in the middle schematically shows the ***double dot formed by five gates.***

Very clear honeycomb structure is detected. The (nearly) vertical lines, corresponding to the change of charge states in the left dot, are much stronger than the (nearly) horizontal lines, which are corresponding to the change of charge states in the right dot. This is a result of the asymmetric capacitive coupling of the QPC to the two dots, just as the original design. Fig. 4-21 (d) is the current of the QPC plotted as a function of one of the plunger gate voltages, showing examples of the current jumps in the QPC. The jumps are indicated by arrows, each corresponding to the adding of one electron onto the dot by changing the plunger gate voltage. Finally, we show that we have managed to tune the coupled QD FET into the so-called few-electron regime, namely the dots can be completely empty of electrons. The left graph in Fig. 4-21 is the detector signal of the QPC showing that the dots are emptied, because decreasing the plunger gate voltages does not lead to new lines in the graph. The right graph in Fig. 4-21 is also the detector signal, where the QPC current is plotted instead of the transconductance. Here, four charge states (0, 0), (0, 1), (1, 0), (1, 1) are indicated by different colors, corresponding to four levels of the QPC current. When the coupled QD FET is working in the few-electron regime, not only the physics is simpler and clearer, but also device properties like the power consumption and speed are much more improved.

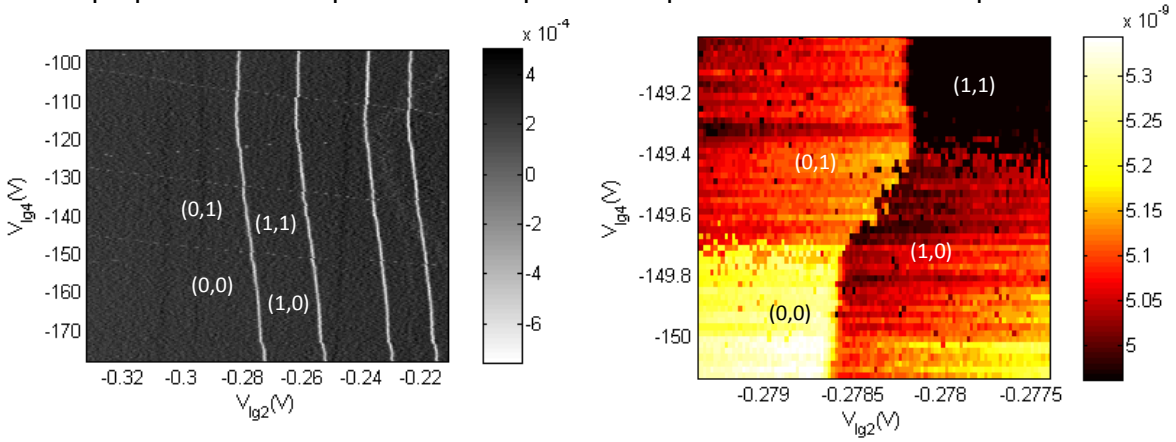


Fig. 4-21: Left: the detector signal of the coupled QD FET showing that it is in the few-electron regime. Right: four charge states detected by the QPC.

Three-terminal ballistic junctions on silicon on insulator wafers

Three-terminal ballistic junctions (TBJs) and derived structures are emerging nanoelectronic devices. In a TBJ, the voltage output V_C from the central branch is a nonlinear function of the voltage inputs V_L and V_R applied to the left and right branches. Based on the nonlinearity, rectification devices, frequency mixers, phase sensitive detectors and logic gates can be realized. The fabricated nanodevices or circuits are small, simple and ballistic. Most importantly, the devices can work at room temperature, which is very promising for applications. The TBJs have been realized in III-V semiconductor 2DEGs such as GaAs/AlGaAs, InGaAs/InP and nanowires and nanotubes. However, no report on silicon-based TBJs has appear. In the following we report our attempt to make TBJs functioning at room temperature on commercial silicon on insulator (SOI) wafers.

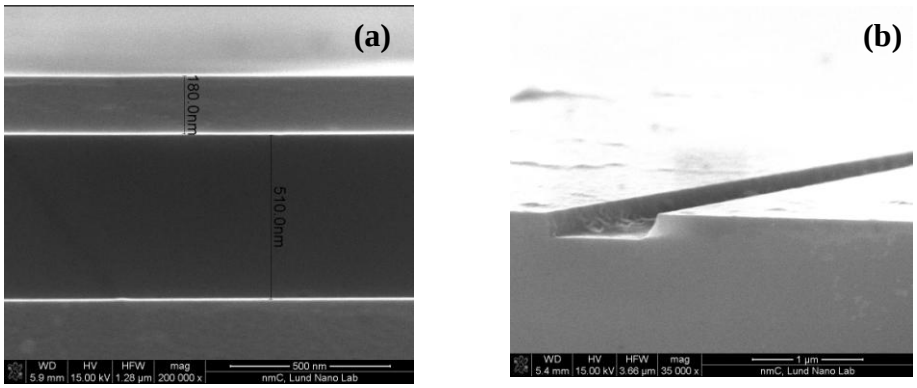


Fig. 4-22: **(a) A SEM image of the cross-section of the SOI wafer with about 180 nm silicon layer after the thinning. (b) A SEM image of the etched trench by ICP-RIE,**

Our SOI wafers are fabricated by wafer bonding, and the silicon layer originally is 500 nm. We use thermal oxidization method to thin down the silicon layer. Fig. 4-22 (a) is a cross-sectional SEM image of the SOI wafer where the top silicon layer, SiO_2 layer and the Si substrate are clearly resolved. In this picture the silicon layer is reduced to 180 nm. The TBJ devices showed thereinafter, however, are made on SOI wafers with even thinner top layer of 100 nm. Our processing technology is as follows. First, the SOI wafer is deposited with Cr, which is made by EBL, thermal evaporation and lift-off. The Cr patter serves as etching masks in the ICP-RIE dry etching procedure. The Cr etching mask is much better than the resist mask such as ZEP 520A in terms of the protection of the unetched areas. The etching depth is down to the insulation layer. A typical example of the etched trenches is shown in Fig. 4-22 (b). After etching, not only the mesa is fabricated, the fine structures are achieved

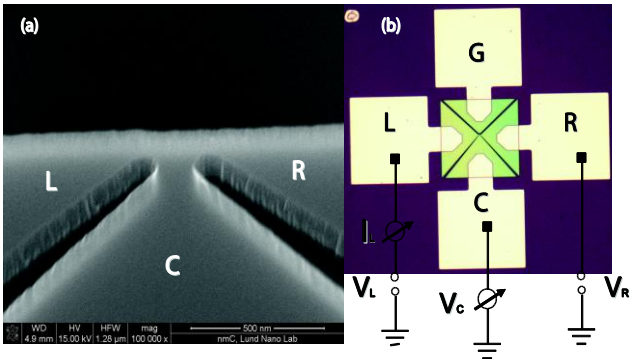


Fig. 4-23: **(a) A SEM (b) optical image of the as-made TBJ device on SOI wafer.**

as well. Then, the Cr mask is removed in a standard Cr-removing chemical solution. The solution has little damage over SOI wafers. The second EBL step is used to fabricate Al ohmic contact to the mesa. The Al bonding pads are about 100 μm × 100 μm big and annealed at around 400 °C.

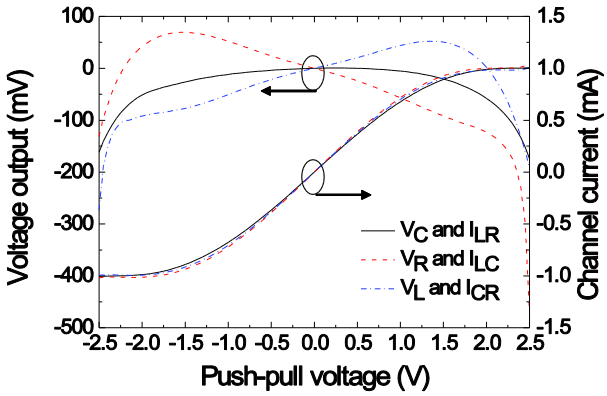


Fig. 4-24: **The voltage outputs and channel currents of the TBJ under push-pull operation mode for both symmetric and asymmetric inputs.**

Fig. 4-23 (a) is a SEM picture of the nanostructure part of the TBJ, where the left, central and right branches are seen. The scale bar is 500 nm. Fig. 4-23 (b) is an optical image of the ready-made TBJ device, where L, C, R and G denote the left, central, right and gate bonding pads, respectively. The gate however is not in use in the measurement. The definitions of V_L, V_R, V_C and I_L are schematically demonstrated. Fig. 4-24 is the measurement results of the device shown in Fig. 4-23. The measurements are carried out in the so-called push-pull fashion, where V_R=-V_L is required. The solid curves are the output V_C and channel current I_{LR} as functions of the push-pull voltage (namely V_L). A clear down-bending behavior in the V_C curve is seen, which is the signature of the ballistic transport in the junction. Note that on silicon the mean free path is in the order of a few 10 nm, which is smaller than our device junction dimension. However, the mean free path is normally measured at thermal equilibrium whereas in our measurements the device is working at several volts. Therefore, the bias-induced elongated mean free path is expected to be longer or comparable to the junction size, and that is why the ballistic transport is observed in our experiment. The current I_{LR} increases linearly with the push-pull voltage and finally saturates. That can be explained by the gap theory of rectification in ballistic three-terminal conductors proposed by our project partner UNIGE. To prove that the experimental findings are indeed coming from the TBJ, the same type of measurement is carried out by using V_L or V_R as the voltage outputs and the rest two branches as the push-pull voltage inputs, see the dashed lines in Fig. 4-24. As expected, the current curves are almost unchanged while the voltage curves become asymmetric. The measured data show that we have successfully realized TBJs working at room temperature on SOI wafers, and are indicating the promising future of the application of TBJs in silicon-based nanoelectronics.

4.3 Deviations from work programme and corrective actions

No deviations of relevance from the work programme are necessary.

4.4 List of deliverables

WP Del. No	Deliverable title	Lead partici-pant	Due date	Delivery date	Estimated person-months	Used person-months
D3.3	Report on coupled quantum dot FETs	LU	M36	M36	30	16,7

The report was delivered in time.

4.5 List of milestones

There are no attainable milestones in the third year.

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[42] M. Prunnila, S. J. Laakso, J. M. Kivioja, and J. Ahopelto, Appl. Phys. Lett. **93**, 112113 (2008).

5. WP4 – Multi-terminal nodes

5.1 Objectives and starting point of work at beginning of reporting period

The objective of WP4 is related to integration aspects of SUBTLE devices as on chip noise sources and multi-terminal nodes with sub-KT switching properties.

5.2 Progress towards objectives

FBFETS were fabricated both in Si and III-V based devices. The technology of noise sources on the basis of tunneling junction was tested on large scale and different aperture diameters. Due to the excellent properties of the FBFETs with RTDs as onchip noise source main efforts were put towards the realization of logic gates with noise tuning operated at room temperature. Logic stochastic resonance is demonstrated.

5.2.1 Task 4.1 – Multiple input bistable feedback FET nodes

This task has been successfully performed within the first two periods.

5.2.2 Task 4.2 – Advanced design and layouts

Results were also reported last year. Applications are described in task 4.4 and WP5.

5.2.3 Task 4.3 – Tunable on-chip noise sources

AlO tunnel junction components

We have proposed a noise source scheme that utilizes metallic tunnel junctions. It is well known that the shadow angle evaporation fabrication process suffers from poor yield and, therefore, we have investigated an alternative fabrication processes for the tunnel junctions. We have developed a simple high yield process that we refer as contact hole tunnel junction (CH-TJ) process. The process is fully CMOS compatible and it has been demonstrated for 6” wafers. The preliminary results were obtained and reported during 2008. During 2009 we have further developed the process and explored different material combinations and process parameters. The process starts with bottom Al sputtering and patterning. Then a dielectric layer (PECVD oxide, nitride or possibly an ALD layer) is deposited and contact holes are opened using UV-lithography and plasma etching. The wafer is loaded back to Al sputtering chamber and the native oxide is removed with Argon plasma. AlO tunnel junction is formed by applying a 2 - 100 mbar oxygen pressure, which is followed by top Al deposition. The tunnel barrier thickness is controlled by the oxidation pressure, time, and temperature. Finally, the top electrode is patterned.

Fig. 5-1 (a) and (b) shows a schematic cross-section of our CH-TJ structure and a SEM image of a fabricated device, respectively. Fig. 5-1 (c)-(d) show TEM cross-sections. The electronic properties of the junctions were investigated, e.g., by measuring the room temperature junction resistances across the 6” wafers by an auto-prober. One example of the outcome of such measurement is shown in Fig. 5-2. This data shows that our process can produce tunnel junctions with high yield. Note that for many applications the local deviation is key figure of merit. All local deviations in Fig. 5-2 are below 2 %. We have fabricated junctions with characteristic resistance between 100 and 20000 Ohm-um2. Both SiN and

SiO2 dielectric have been tested. These dielectrics give similar results. However, SiN has been shown to have better electrical properties; resonators that utilize SiN capacitor dielectrics show significantly higher Q-values. The minimum junction area is limited by the lithography and the thickness of dielectric. With Canon i-line stepper and standard 1.4 um photo resist the process is reliable down to 700 nm junction diameter. The yield degrades strongly (almost all junctions show infinite resistance) when diameter is reduced down to 600 nm. This is due to lithography. By selecting a thinner resist and iterating focus, exposure and development parameters we should be able to produce junctions with ~400 nm diameter with standard UV-lithography defined junctions. Further down-scaling of the junctions should be relatively straightforward with e-beam lithography based process.

CH-TJ junctions can be used as a noise source as demonstrated in SUBTLE. They can be used as an on chip noise source for many devices. However, If the device, to which the noise is fed into, does not tolerate the fabrication process of CH-TJ components one can utilize, e.g., flip-chip bonding in the integration. Wire bonding is also one alternative, but one should note that it is difficult to reduce the bonding wire inductance below 1 nH and this limits the band width. In addition of the noise sources the fabricated CH-TJ devices have many applications in various fields, which include, e.g., primary thermometry, NIS bolometers, NIS refrigerators, and quantum information. Therefore, the technology developed in this project will be further investigated and developed for these applications at VTT.

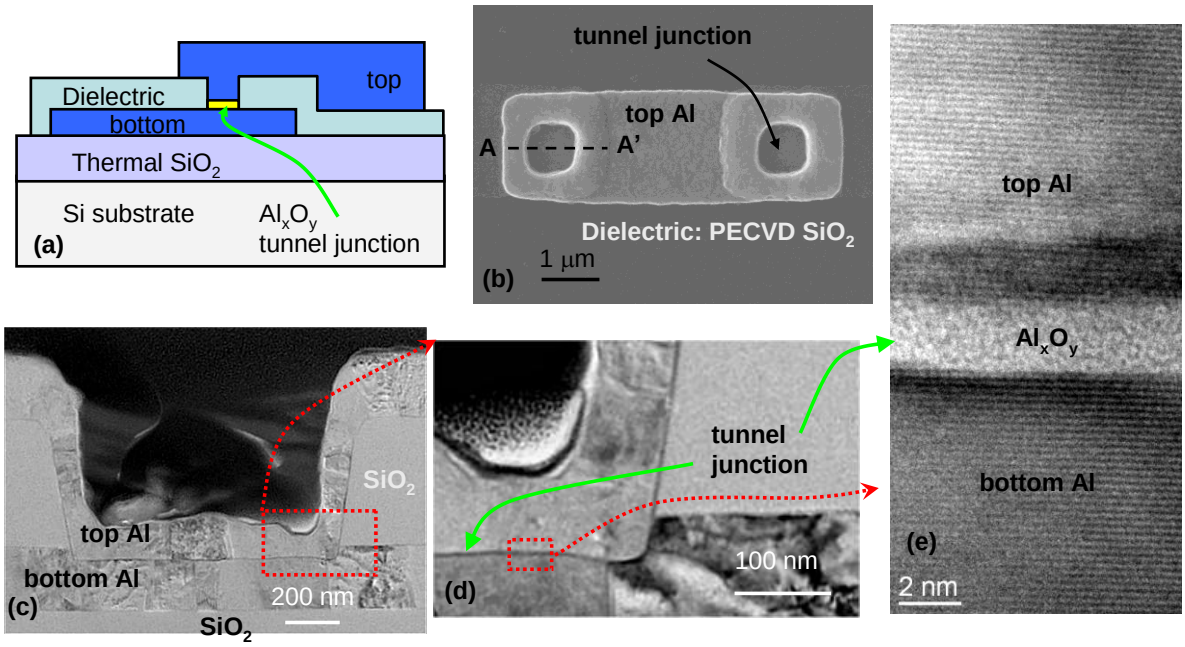

***Fig. 5-1*: (a) Schematic cross-section of CH tunnel junction. (b) Top view SEM image of a rectangular 1 um2 double tunnel junction. (c) TEM cross-section along A-A'. (d) blow up of the junction edge. (e) High resolution TEM of the junction.**

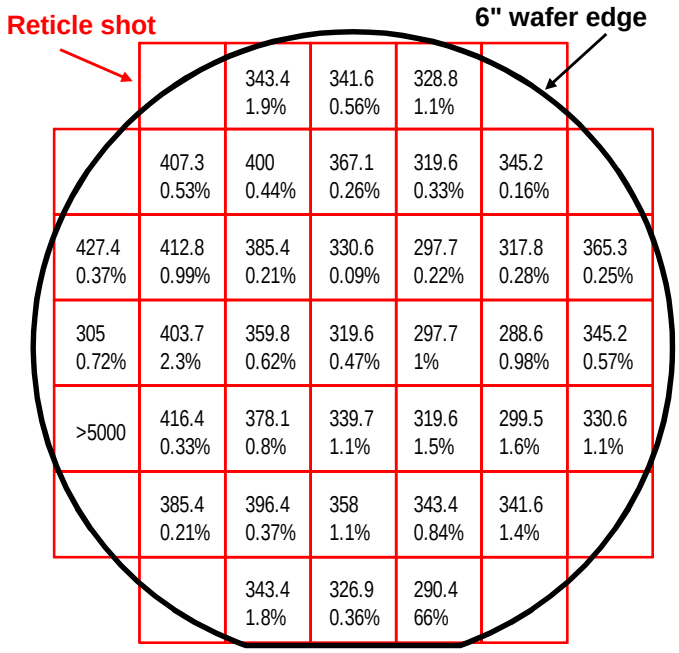

***Fig. 5-2*: Resistance map across 6" wafer. The upper number in each reticle shot gives the characteristic junction resistance in units Ohm-um2. the lower number gives the local deviation. Single number ">5000" means an open circuit, i.e., faulty device. Faulty devices have been observed only close to wafer edges. The local deviation is determined by measuring adjacent junctions (400 um distance on wafer). The data is measured from 700 nm diameter circular junctions with SiN dielectric.**

5.2.4 Task 4.4 – Artificial neuron nodes

Threshold devices with several input parameters are considerate to mimic the action of neurons. Therefore, submicron-sized mesas of resonant tunneling diodes (RTDs) with split drain contacts have been realized. These three-terminal RTDs can be operated at room temperature and exhibit a steep thresholds.

In the upper part of Fig. 5-3 a sketch of the RTD layer sequence is shown. The structure was grown by molecular beam epitaxy. The central part of the RTD is built up by two 3 nm thick $Al_{0.6}Ga_{0.4}As$ barriers embedding a 4 nm thick GaAs layer. Afterward, electron beam lithography and etching were applied for the definition of small mesas with a trench cutting through the upper doped layers. Gold contacts were realized to independently contact the two upper RTD branches further used as input terminals (right part of Fig. 5-3 (a)). The measurement circuit diagram is depicted in Fig. 5-3 (b). The samples were tested at room temperature in the dark. The RTD shows a resonance peak in the I-V curve at 1.25 V. A hysteresis of 30 mV was found between the up and down sweep of V_{dc}. In the right part of Fig. 5-3 (b) the working principle is presented. Via the voltage V_{dc} the RTD was driven close to the bistable transition. When the amplitude V_{ac} is ramped up close to a critical threshold voltage, noise-triggered switching can drive the RTD in the upper state.

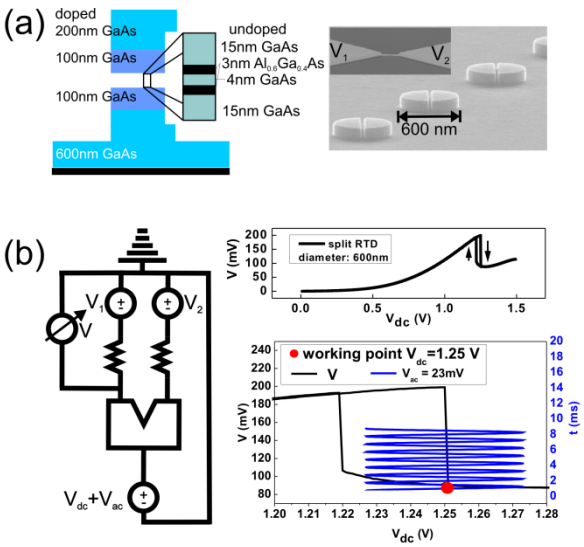

Fig. 5-3: (a) Left part: Sketch of the layer sequence. Molecular beam epitaxy was applied to grow 3 nm thick AlGaAs barriers embedding a 4 nm thick GaAs layer. The outer GaAs layers were doped with Si to form contacts, whereas the inner parts are undoped. Right part: Electron beam lithography and etching were applied to define split RTD mesas with a diameter of 600 nm. The top branches were contacted by gold contacts separately. Different voltages were applied to the top RTD branches (V_1 and V_2). (b) Left part: Measurement circuit diagram. Voltages V_1 and V_2 were applied in series with 2kΩ resistors to the RTD branches. The working point voltage V_{dc} + V_{as} was applied to the back contact. The voltage V was measured as indicated. Right part: The I-V trace of the RTD shows a bistable transition with a hysteresis of about 30 mV. The working point was chosen in such a way that V_{dc} = 1.25V and V_{ac} was modulated between 20 and 30 mV with a frequency of 1 kHz. V_1 and V_2 were set to 0 or 2 mV.

In this dynamical driven regime small voltage changes at the input branches of only a few mV lead to pronounced switching of spike-like signal trains. In Fig. 5-4 time traces of the RTD output voltage V are shown. The bistable character of the dynamics is apparent. By passing from V_{ac} = 23 to 30 mV the system is changed totally by keeping constant all the other parameters. For V_{ac} = 23 mV the RTD stays in the lower state with V < 105 mV . For V_{ac} = 25.9 mV the RTD is close to the threshold so that noise-induced random jumps from one state to the other appear. By increasing V_{ac} now by only 0.1 mV, bursts of spike-like signal trains can be observed. For V_{ac} = 30 mV the upper and the lower state of the RTD are almost equally occupied.

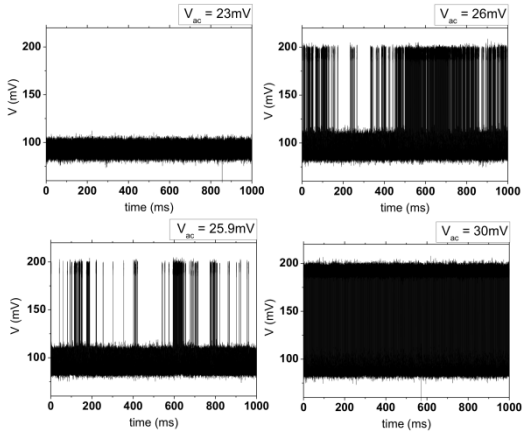

Fig. 5-4: Time series of the RTD output voltage V for different ac voltages V_{ac}. For V_{ac} = 23 mV , the RTD stays in the lower state. By increasing V_{ac} to 25.9 mV it eventually happens that the RTD switches to the upper state. Then a shift of only 0.1 mV

increases efficiently the number of spike-like switching events. For V_{ac} = 30 mV . The RTD stays equally in the upper and the lower state. The mean is used here as a measure for the output signal.

In Fig. 5-5 (a) (right) we show the transconductance-to-current ratio for this device. As it is well apparent such a quantity exceeds significantly the highest value achievable in a standard transistor, the inverse thermal voltage e/kT, pointing towards a non-equilibrium switching process [43]. We stress the fact that a fairly large output change is produced as a function of a relatively small change in the input. Based on these results we can interpret the functioning of the split RTD in terms of a universal NAND logic gate. Most interestingly the logic functioning of such a gate can be easily changed into that of a logic NOR gate. In fact, as we show in Fig. 5-5 (a) by changing the amplitude of the periodic forcing V_{ac} around 26.0 mV, the logic behavior changes from NOR to NAND. Such a change happens in a relatively small amplitude range of the periodic forcing.

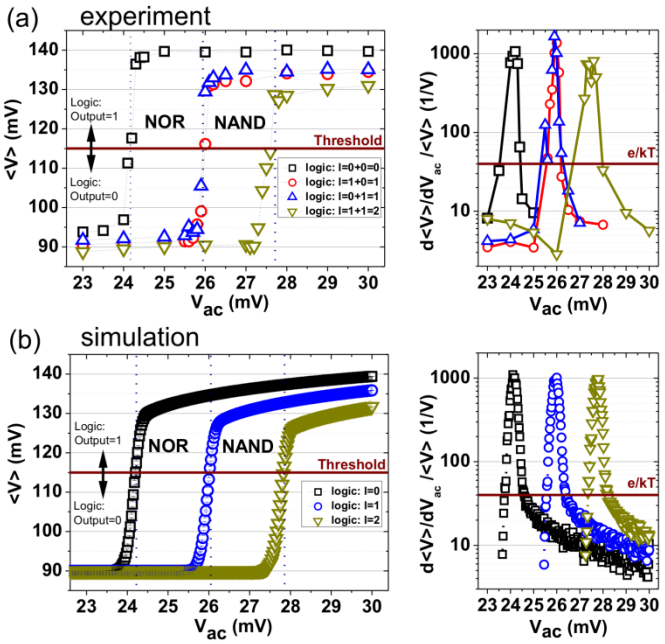

Fig. 5-5: (Left part) <V> is interpreted as a logic output 0 for values smaller than 115 mV or 1 for values exceeding 115 mV as a function of the logic inputs I=0, 1 and 2 for different voltages V_{ac}. No external noise has been added to the RTD. (Right part) Transconductance-to-current ratio versus V_{ac}. It is also plotted e/kT (at room temperature) as a reference. (b) Numerical data from the ideal Schmitt-Trigger model. All parameters are taken from the experiment.

To model our observations we applied a Schmitt-Trigger model. In Fig. 5-5 (b) such a Schmitt-Trigger model simulation is shown. All system parameters were taken from the experiment, e.g. the threshold barriers were set to ±15 mV as the hysteresis was 30 mV. The noise floor was determined by a standard network analyzer with σ = 0.14 mV. The total time dependent force is composed of three different components:

$$F(t) = A(t) + \xi(t) + I(t) \qquad (1)$$

where A(t) = V_{ac} sin(2πft) is the time periodic forcing signal with magnitude V_{ac} and frequency f. ξ(t) is a stochastic force that mimics the presence of noise, that can be assumed exponentially correlated, Gaussian distributed, with zero mean and standard deviation σ. I(t) represents the logic input signal composed by the composition of the two inputs at the two split RTD branches. As shown in Fig. 5-5 (b) the numerical obtained data agree with the

experimental findings. Not only does the logic gate change from NOR to NAND around the amplitude range of V_{ac} = 26 mV, but also the theoretical transconductance-to-current ratio exceed the thermal limit.

Thus the stochastic nonlinear process explains well the logic functioning of the split RTD. This model is also capable of predicting a very useful property, i.e. a wide tolerance to the noise affecting the input signals. The present strategy aimed at reducing the dissipated power in traditional logic gates based on transistors requires a decrease in the transistors operative voltage thus increasing the vulnerability to noise. In the following we show that the new scheme just presented for the description of the RTD functioning, shows a significant tolerance to noise. In Fig. 5-6 (a) we show <V> as a function of the noise standard deviation σ per single input I = 1 for the NAND configuration with V_{ac} = 26.6 mV and in Fig. 5-6 (b) for the NOR configuration with V_{ac} = 24.6 mV. Evidently a logical output coherent with the NOR/NAND scheme (logical 1 corresponding to <V> ≥ 115 mV) is also maintained for noise intensities comparable with the value of the single input. This is quite a remarkable property that could allow the operation of the logic gate in unusually high noise environments. Moreover, with reference to Fig. 5-6 we notice that a larger threshold for the logical 1 might allow the operation of the gate also in the presence of a much larger noise level. We want to stress that the noise-tolerance discussed here is not just a mere consequence of the averaging. In fact the average on the output response of the device is part of the measuring procedure and is taken both in the presence and in the absence of noise.

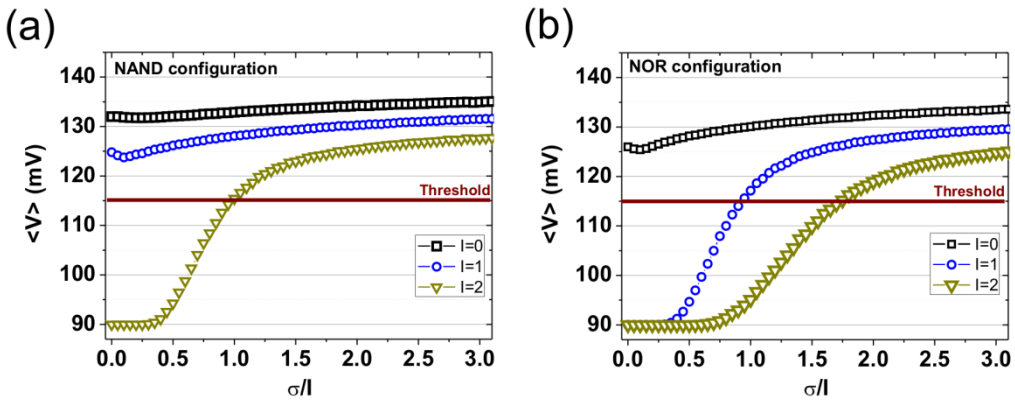

Fig. 5-6: Mean output <V> in the NAND configuration with V_{ac} = 26.6 mV for the logic inputs I(t) = 0, 1 and 2 as a function of the noise standard deviation σ/I where I is the amplitude of the single signal input (here I = 1 (2 mV)). (b) <V> in the NOR configuration with V_{ac} = 24.6 mV for the logic inputs I(t) = 0, 1 and 2 as a function of σ/I.

5.3 Deviations from work programme and corrective actions

No deviations have taken place so far.

5.4 List of deliverables

WP Del. No	Deliverable title	Lead partici-pant	Due date	Delivery date	Estimated person-months	Used person-months
D4.3	Report on advanced designs of multiterminal SR nodes and scheme of adaptive feedback of on-chip noise generator	VTT	M36	M36	20	10,9

The report was delivered in time.

5.5 List of milestones

WP Mile-stone	Milestone title	Lead participant	Due date	Delivery date
M4.3	Experimental demonstration of an adaptive feedback of on-chip noise generator	VTT	M30	M30

Tuneable bistability was demonstrated. The width hysteresis can be tuned so small that the system noise controls the switching (sub kT regime).

[43] F. Marchesoni, F. Apostolico, L. Gammaitoni, S. Santucci, Phys. Rev. E. 58(6 Part A):7079-7084, (1998).

6. WP5 – Sensors & noise enhanced switching

6.1 Objectives and starting point of work at beginning of reporting period

In the last year, deep-in simulation of receiver-operating-characteristics (ROC) were performed. In the ROC, a peak-like structure below the threshold of detector activation was observed. From the ROC very promising features of the SUBTLE detector were deduced. Within the last year, a hand-in-hand analysis of fabricated SUBTLE detectors with the models were performed. One important milestone has been planned for the third period: M5.5: Signal detection test on e.m bistable detector with resolution better than 10%kT (M30)

6.2 Progress towards objectives

The expected milestone (M5.5: Signal detection tests on e.m. bistable detector with resolution better than 10%kT) has been reached with success. We can demonstrate a sensor with a resolution of detection a signal hidden in a noise floor of 0.1%. Main results are summarized below. Noise induced logics is demonstrated, too.

6.2.1 Task 5.1 – Residence time detectors

The main aim of this task was the development of bistable sensors based on Residence time difference used as a quantifier for signal detection. This task was realized successfully within the first and the second year. Moreover, major results of this task have been implemented in real nanoscaled sensing devices.

6.2.2 Task 5.2 – Electro/magneto asymmetry sensors

Magnetic field nanosensor

A new class of promising devices based on Y-branch nanojunctions [44] has been demonstrated to show peculiar bistable behaviors under the action of external control fields [45,46,47]. For such devices the presence of random fluctuations in the measured voltages and currents could be a limiting cause for their employment as sensors or logic gates. [48,49]

We concentrate our attention on devices based on a modulation-doped GaAs/AlGaAs heterostructure with a two-dimensional electron gas (2-DEG) located 80*nm* below the surface with a carrier density $n = 3.7 \times 10^{11} cm^{-2}$ and a mobility $\mu = 1.1 \times 10^{6} cm^{2} / Vs$ determined at 4.2K in the dark. An electron microscopy image of an Y-branched junction is shown in the upper panel of Fig. 6-1.

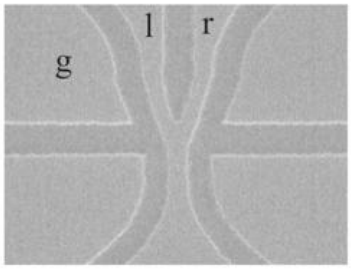

Fig. 6-1: Electron microscopy image of a Y-branched nanojunction. The Y-branch was realized by electron beam lithography and wet chemical etching. The left (l) and right (r) side-gates are separated from the Y-junction by 375nm wide and 90nm deep trenches.

For the measurements, the voltages at either g or l were used as input signals and with the voltage at r serving as output signal. A constant supply voltage was applied in series with a load resistor $R_r = 10\text{M}\Omega$ to the right branch, and the stem of the Y-branch was connected to ground. The voltage V_l was applied to the left branch. We detected the voltage drop at the stem-right branch channel V_r as a function of input voltages at g or l. Thereby we used two different measurement modes: (i) Branch-mode using the left branch l as the input stage. (ii) Gate mode with the side-gate g as the input stage. With these modes inverted as well as non-inverted bistable switching with tunable hysteresis can be observed.
The bistable character of the Y-branch has already been discussed in the deliverables of previous periods as reported in Fig. 6-2 (where the voltage drop at the right branch V_r as a function of V_l is shown).

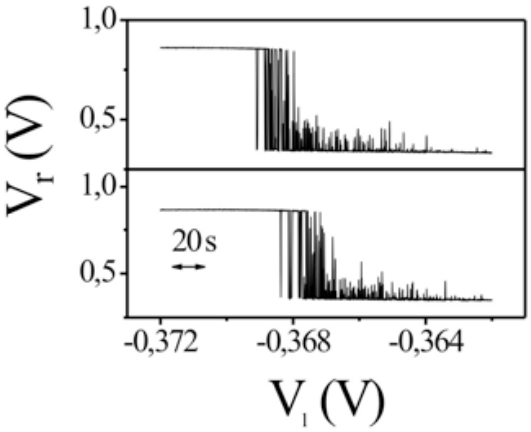

Fig. 6-2: Transfer characteristics as a function of V_l. The bistable character of the Y-branch is apparent here, where the voltage drop at the right branch V_r as a function of V_l with V_g = -0.2990V (upper panel) and V_g = -0.2925V (lower panel) for a system temperature of 20 K is shown. Here the voltage V_l was swept forward and backward between V_l = -0.3620V and V_l = -0.3720V with a sweep rate of about 50µV/s.

In order to exploit noise activated bistable switching (NABS) effects for the measurement purposes we focused our attention to the output time series for different values of V_l and V_g. In Fig. 6-3 V_r is depicted as a function of time for $V_g = $ -0.2990V and $V_l = $ -0.3684V. We stress the fact that the switch dynamics depicted here is completely activated by the device internal noise, without any external signal injection, at difference with other nanoscale devices [50]. Dependent on the values of V_l and V_g the system can reside preferentially in one of the two states defined by margins with the output high (H) for $V_r > 0.75$V and low (L) for $V_r < 0.45$V. The mean residence time as a characteristic quantity for this stochastic process

can be evaluated by measuring $T_{H_i} = t_{Li} - t_{H_i}$ and $T_{L_i} = t_{H_{i+1}} - t_{L_i}$, the residence times for the i^{th} appearance of H and L state, respectively and averaging over $n_{H,L}$ the total number of H and L events during the measurement time interval.

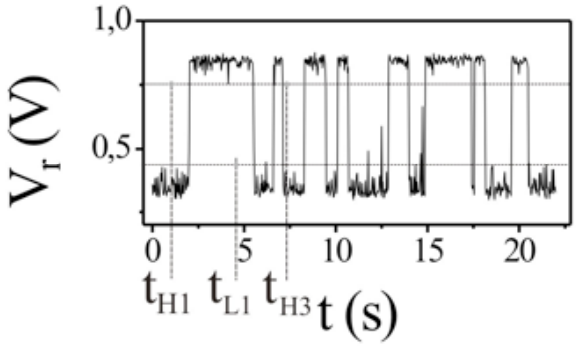

Fig. 6-3: Time evolution of V_r. Thresholds for L and H states are set to V_r = 0.45V and V_r = 0.75V.

Now we present the experimental evidence of the functioning of our Y-branch based device as a magnetic field detector. In order to measure an external magnetic field we relied on a detection method based upon the asymmetry of the residence times of a fluctuating two-state system.[51]
For a symmetric bistable system the residence times in both states are equal on average. In contrast, if an external signal perturbs the symmetry (adding to the DC control signal or skewing the potential) a difference in the mean residence times emerges. Such a difference, quantified as $\Delta T = T_H - T_L$, can be used to detect the perturbing signal.
In Fig. 6-4 the difference in the mean residence times of Fig. 6-3 , $\Delta T = T_H - T_L$ is shown as function of an external magnetic field applied parallel to the growth direction of the sample. The magnetic field intensity B is swept between $B =$ -0.15T and $B =$ 0.25T with a sweeping rate of 0.4T/min. As it is well apparent, NABS occurs around zero magnetic field (approximately symmetric configuration) and is pronounced between $B \approx$ -30mT and $B \approx$ +80mT. A deviation from the zero magnetic field value results in an asymmetry, i.e. a difference in the mean residence times. Using time series measurements, the output voltage is acquired in order to determine the difference in the mean residence times $\Delta T = T_H - T_L$ as function of the magnetic field. The outcome is shown in Fig. 6-4. One observes a linear dependence, now between B and ΔT , for a small deviation ε_B . A linear fit with $B(\Delta T) = B_0 + \beta \Delta T$ between $B =$ -14mT and $B =$ 18mT results in $B_0 = (25.89 \pm 0.25) \cdot 10^{-3}$ T and $c = (-27.00 \pm 0.69) \cdot 10^{-3}$ T/s. The accuracy of the magnetic field determination for a small deviation ε_B is better than $\pm$ 2mT.

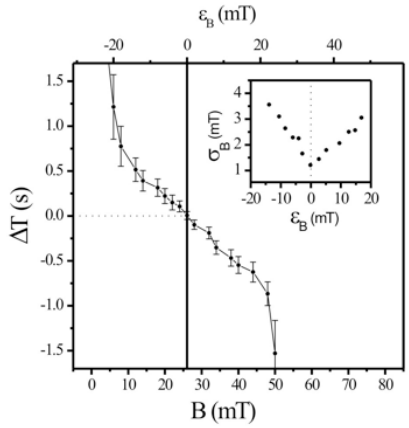

Fig. 6-4: Difference of the mean residence times ΔT ***dependent on*** B ***with*** $\varepsilon_B = B - B_0$ ***defined by*** $\Delta T(B_0) = 0$***. Inset: Standard error*** σ_B ***as a function of the magnetic field deviation*** ε_B***.***

In conclusion we have shown that our noise activated nonlinear nanosensor, thanks to the nonlinear feature of its dynamics can be usefully employed to measure DC (or low frequency) magnetic signal much smaller than the internal noise of the device itself. Moreover, the operating principle is general enough that its application can be extended to the measurement of signals others than the pure magnetic, provided that the coupling with the system dynamics is capable to alter its symmetry.

6.2.3 Task 5.3 – Noise enhanced logics

Main efforts of this task have been already implemented and detailed explained in Task 4.4. In this task, we focused on the explicit artificial neuron functioning of our split RTD device. Moreover, it could be shown, that reconfigurable and universal logic gate can be achieved.
This suggests that noise controls the dynamics in the regime for the observed transition of logic universal gates. Noise driven logic gate morphology is demonstrated experimentally in Fig. 6-5 (a) and verified via digital simulation in Fig. 6-5 (b), which shows the output <V> for the logic inputs I=0,1 and 2 with V_i=0 (0 mV) and V_i=1 (2 mV) as a function of the noise intensity σ. By increasing σ a logic NOR gate can be realized attributed to a logic stochastic resonance. Most interestingly, instead of destroying the logic behavior a further increase of σ leads to a change from NOR into NAND. Worth to mention that both gates are universal, i.e. any logic gate can be realized by combination of such gates. Noise-controlled morphology of universal logic gates as demonstrated here may allow logic gate architectures designed by noise.

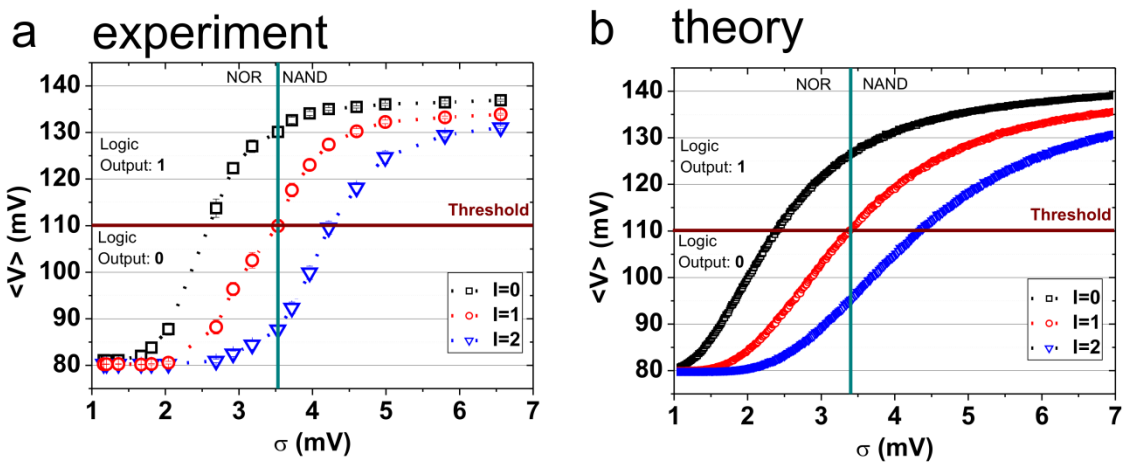

Fig. 6-5: Noise induced logic gate transition from NOR to NAND for different values of the logic input I. a, Experimentally determined <V> as a function of the noise standard deviation for a switching voltage of I=0,1 and 2 with $V_{1,2}$ = 0 (0 mV), $V_{1,2}$ = 1 (2 mV). b, Theoretical simulations with the experimental obtained parameters agree with the experimental data.

6.2.4 Task 5.4 – Evaluation of device limits

Top in Fig. 6-6 A) a sketch of the layer sequence of the split resonant tunneling diode (RTD) is pictured. The structure was grown by molecular beam epitaxy and is based on a GaAs system. Heavily n-doped drain and source layers sandwich the double barrier structure consisting of 15nm width GaAs buffer layers, 3nm thick undoped $Al_{0.6}Ga_{0.4}As$ barrier layers and a 4nm thick undoped GaAs quantum well. With standard mask techniques and dry chemical etching methods split RTD masks were fabricated with diameters ranging from d=600nm up to 1.8µm. Gold was vapor-deposited so that each branch can be contacted independent. The electronic circuit diagram and a FEM picture of the device is shown bottom of Fig. 6-6 A). The total voltage V consisting of a dc component V_{DC} and a time periodic signal V_{AC} sets the working condition of the RTD and the output voltage from each branch is measured over the load resistors R_1 and R_2. Mirror and lenses system focuses the laser with wavelength λ=448nm on the light effective split area of the RTD with A_{RTD}=0.22µm^2. In the residence time difference based sensory action the target signal of magnitude ε introduces an asymmetry in the bistable potential. Without the target signal the difference is zero, $<\Delta T(\varepsilon=0)>= <T_+>-<T_->=0$, while not equal to zero in the presence of the signal, $<\Delta T(\varepsilon\neq 0)>\neq 0$. The input-output characteristic of a split RTD with diameter d=800nm under illumination and without light is pictured TOP in Fig. 6-6 B). Obviously the light induces an asymmetry $\Delta V=V_{UP}(P\neq 0)-V_{UP}(P=0)$, which is the quantity in the residence time difference based sensor dynamics.

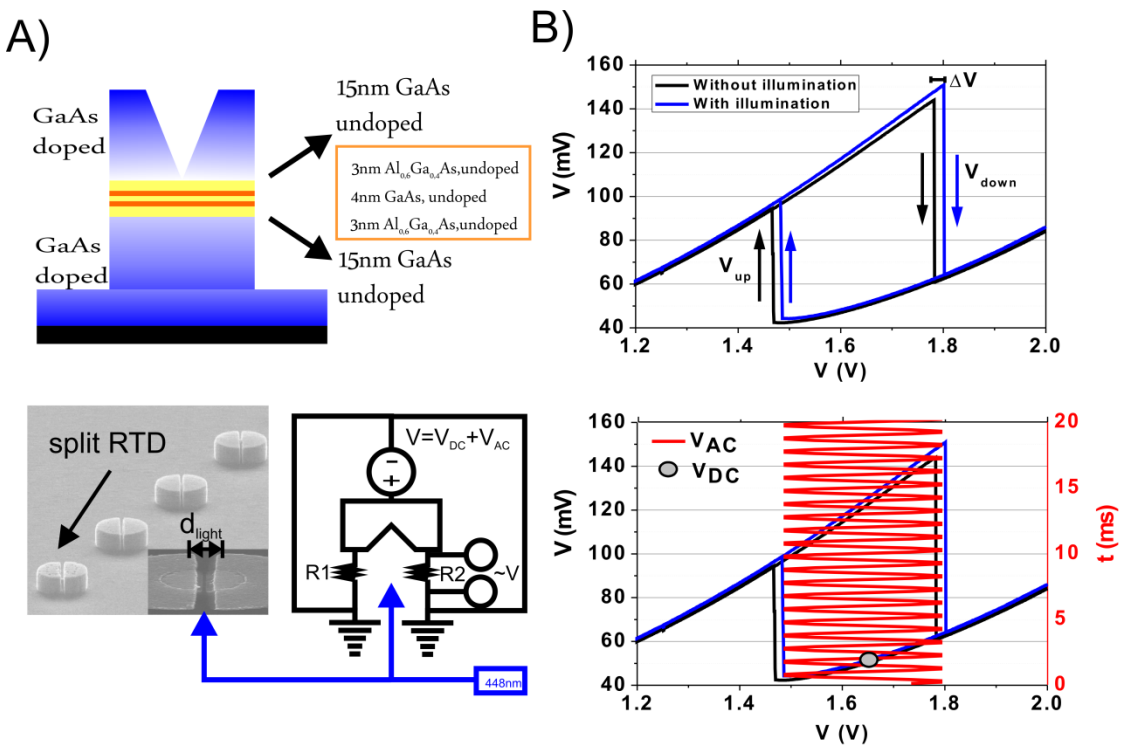

Fig. 6-6: A) (Top) Layer sequence of the split RTD. Heavily n-doped drain and source layers sandwich the double barrier structure. 15nm thick GaAs buffer layers and 3nm thick $Al_{0.6}Ga_{0.4}As$ barriers cover the 4nm thick undoped GaAs quantum well. Within a diameter range from d=600nm up to 1.5µm a split width of 100nm was implemented, so that each branch can be contacted independent. (Bottom) FEM pictures of the RTD and the electronic circuit diagram with the total applied voltage V consisting of a fixed working point voltage V_{DC} and an applied time periodic signal with amplitude V_{AC} and frequency f. The voltage drops over the two load resistors, proportional to the current in each branch, is the quantity for the output. B) Output input characteristic of a split RTD with diameter d=800nm with and without illumination. With light the switching voltages V_{up} and V_{down} change, which introduces an asymmetry ΔV in the bistable potential. (Bottom) In the dynamical Geiger mode analysis a periodic forcing V_{AC} is applied, so that the system response without illumination is the stable outputs V_L≈50mV. However, in the presence of the target signal a shift in the potential leads to a significant change due to noise activated spikes.

From an experimentalist point of view, symmetry in the system is hard to obtain. However from that point of view, the question arises to obtain results with an explicit asymmetry in the system. This is what we will call Geiger mode analysis and the system is biased as follows. The working point V_{DC} is shifted slightly asymmetric, which lead to pronounced noise activated regime. This is pictured bottom of Fig. 6-6 B). In the absent of the target signal the time periodic signal cannot reach the transition value V_{UP} and is therefore stable with output $<V_{OUT}>=V_L$. This is shown in Fig. 6-7 A). However, as the light intensity increases noise induced spikes are generated as a consequence of the potential shift as well as due to the existing noise floor (Fig. 6-7 B) and as the light intensity doubles the number of generated spikes exponentially increases (Fig. 6-7 C)). Further light power of course would creates a spike in almost every cycle of the periodic forcing. In the dynamical Geiger mode, the input-output characteristic of the switch is a nonlinear transfer function limited only by internal noise floor.

For the probability of the detection of ultra small SNRs, we now introduce the Receiver Operating Characteristic (ROC). This well known detection processing tool will guide us through our main ideas, namely that spike counting is most sensitive leading to a maximum

probability of detection as well as a stochastic resonance like sensory action at ultra small SNRs.

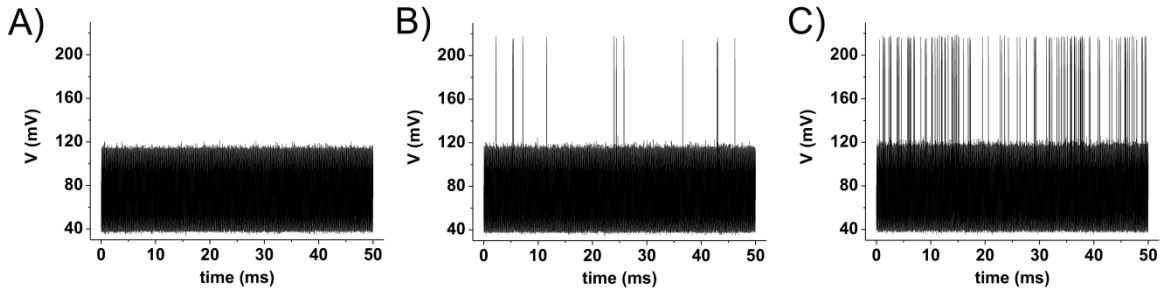

Fig. 6-7: Time trace signals obtained for different values of the light intensity. Without light (A) the Geiger mode is set, so that no noise induced switches occur. As the light intensity increases from B) to C) the number of spikes exponentially enhance the output signal as a consequence of the light induced potential shift. While there are only 10 switches, the number of spikes significantly increase as the light intensity doubles.

In Fig. 6-8 the working principle of the Receiver Operating Characteristic (ROC) is demonstrated. The mean value of the RTD output, under illumination and as a reference signal without illumination is obtained for 500 switches, in total 1000 times. The so obtained signal are first distributed, pictured in Fig. 6-8 A), and for each threshold value $<V_{Min}>\leq\gamma\leq<V_{Max}>$, the probability of detection (PD) (area under the ε shifted curve) and the probability of false alarm (PFA) (area under the ε=0 curve) is obtained, which is pictured in B). Fig. 6-8 C) finally plots the PD versus the PFA. The area under the so called ROC curve indicates the detectors ability for detection. If the ROC area is equal 1 decide that the detector is good otherwise if the ROC area is 0.5 the detector is bad.

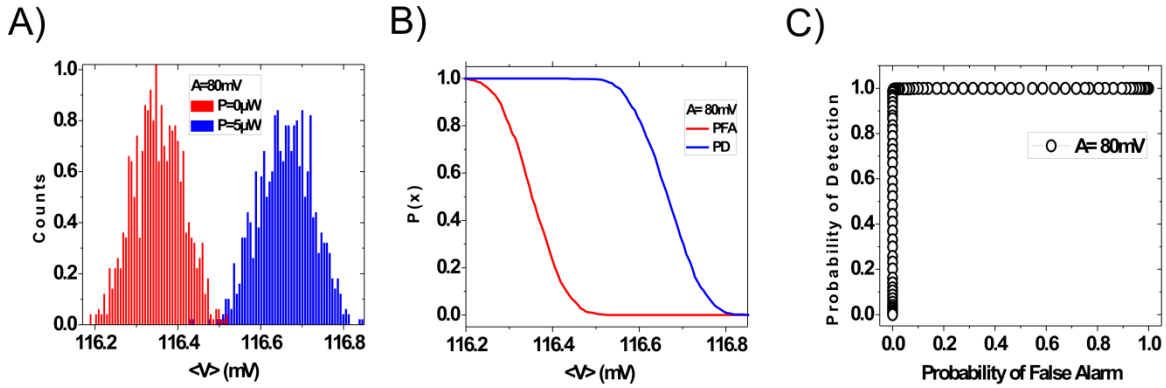

Fig. 6-8: Working principle of the ROC analysis. A time periodic signal with frequency f=10kHz and amplitude V_{AC}=80mV is applied, so that the system switches between its stable outputs. A) Normalized distribution of the averaged outputs <V> obtained for an integration window of 500 switches. B) The area over different threshold values $\gamma_{1,2,3...}$ for the reference signal without the target signal, the probability of false alarm (PFA), and with the target signal, the probability of detection (PD), are calculated. C) As a quantity of the detector the area under PD(PFA), the so called ROC area, gives rise to the detect ability of the system. In our case the ROC area is equal to one. Therefore the detector is assumed to be "good" for the given target signal.

With a barrier value b=71mV the ROC area for two different light intensities P=5 and 2.5µW is measured for a variation of the forcing amplitude V_{AC}, pictured in Fig. 6-9. Obviously the ROC area increases first, reaches a maximum at V_{AC}=71 mV, decreases again to a local minimum at V_{AC}= 71.3 mV with a ROC area of about 0.91. A second increase in the probability of detection is visible and afterwards the system stays more or less equally on the same value. The question arises, what determines the sensory dynamics. In Fig. 6-9. B) a best fit simulation is pictured. The ROC Area as a function of the periodic forcing amplitude

for mean value (red) and by just counting the signal trains. Obviously the change in the number of spikes generated the maximum probability of detection.

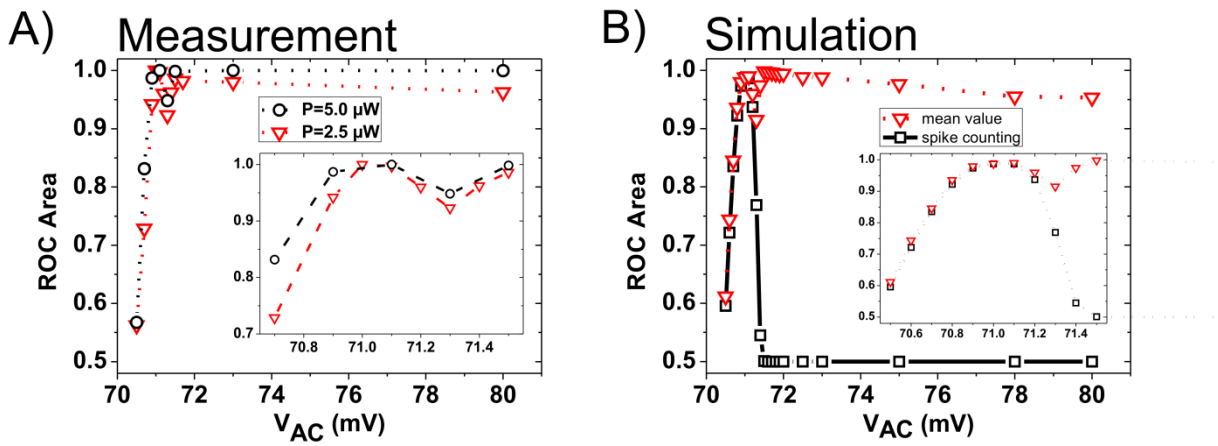

Fig. 6-9: ROC area as a function of the amplitude V_{AC} of the sine-wave periodic forcing for two light intensities P=5 and 2.5µW with frequency f=10kHz, integration time 50ms, in total 1000 counts. B) Simulated ROC area with experimental obtained parameters. Also plotted is the ROC area by just counting the noise generated spikes (squares). Obvious a maximum probability of detection is obtained by lower values of V_{AC}, while the number of counts generate the sensor dynamics.

In Fig. 5 the ROC Area as a function of the Signal-To-Ratio by counting the spike like signal trains is pictured for three different values of the light intensity P = 40, 23 and 2.5pW. However, instead of a monotallicaly decreasing output signal with lower values of the SNR, the ROC Area increases up to a maximum of probability by decreasing the SNR. For the light intensity of P=2.5pW the maximum ROC area value is 0.78 at a input SNR of 0.001. This is a stochastic resonant like effect, which lead to a pronounced detect ability in the system for a ultra small SNR.

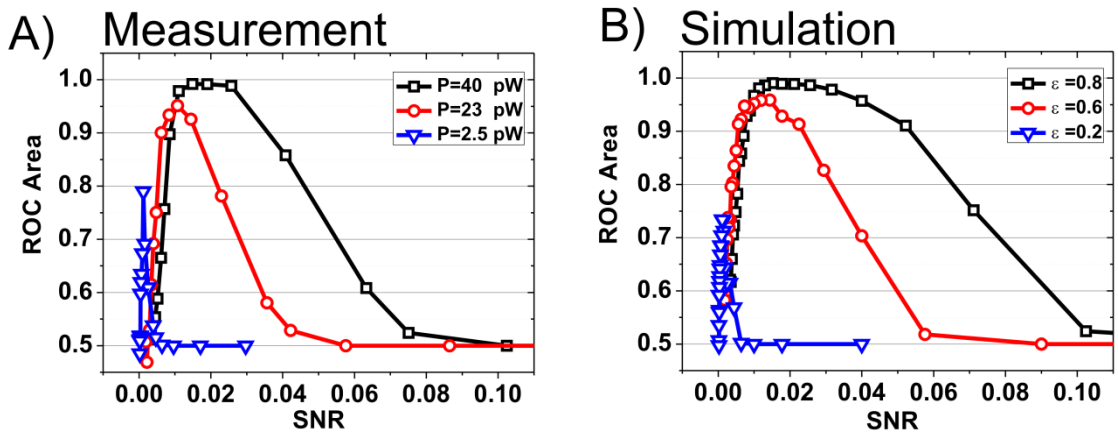

Fig. 6-10: ROC Area as a function of the Signal-to-Noise ratio for experimental (A)) and numerical obtained data (B)) by just counting the spike like signal trains for three different values of the target signal. With V_{AC}=46mV, b=49mV and a frequency of f=10kHz a maximum probability of detection is obtained as the SNR decreases. This nonlinear stochastic resonance like sensory effect approve a minimum light intensity of P=2.5pW for a input SNR=0.001.

To resume our experimental results, we want to point out, that in the dynamical Geiger mode analysis spike counting of neuron like signal trains lead to a maximum probability of detection. Furthermore, an enhanced signal detect ability is obtained by actually decreasing the SNR.

6.3 Deviations from work programme and corrective actions

No relevant deviations have been observed. No deviations are expected for the next period.

6.4 List of deliverables

WP Del. no	Deliverable title	Lead partici-pant	Due date	Delivery date	Estimated person-months	Used person-months
D5.3	Report: Signal detection tests on single and networked prototypes and nanoelectronic SR Sensor	UNIPG	M36	M36	17	11,8

The report was delivered in time

6.5 List of milestones

WP Mile-stone	Milestone title	Lead participant	Due date	Delivery date
M5.5	Signal detection tests on e.m. bistable detector with resolution better than 10% KT	UNIPG	M30	M30

The milestone has been reached within the expected time.

[44] Palm, T., Self-consistent calculations of an electron-wave Y-branch switch. *J. Appl. Phys.* 74, 3551 (1993)

[45] Wesström, Jan-Olof J., Self-Gating Effect in the Electron Y-Branch Switch. *Phys. Rev. Lett.* 82, 2564 - 2567 (1999)

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[48] Birge, R.R., Lawrence, A. F., Tallent, J.R., Quantum effects, thermal statistics and reliability of nanoscale molecular and semiconductor devices. *Nanotechnology* 2, p. 73-87, 1991

[49] Sano, N., Increasing importance of electronic thermal noise in sub-0.1mm Si-MOSFETs. *The IEICE Transactions on Electronics*, E83-C:1203–1211, Aug. 2000.

[50] Badzey, Robert L., Mohanty, Pritiraj, Coherent signal amplification in bistable nanomechanical oscillators by stochastic resonance. Nature 437, 995 - 998 (13 Oct 2005) Letter

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7. WP6 – Project management

7.1 Objectives and starting point of work at beginning of reporting period

The main objectives in this work package are the presentation of results outside the consortium and to manage the exploitation possibilities of results. Furthermore, a supervision of administrative and financial affairs, project progress and check of the deliverable schedule, the exploitation process including the protection of intellectual properties and planning of technology implementation for commercial use are also an object of this WP.

7.2 Progress towards objectives

7.2.1 Task 6.1 – General management

The general management coordinates the administrative and financial issues.

We held 4 meetings during year 3:

- A review meeting in Brussels, Belgium, December 11th-12th 2008
- A general project meeting in Malta, February 5th-6th with tutorial presentations of the host partner and technical presentation of all partners.
- A general project meeting in Perugia, Italy, Mai 11th-12th with tutorial presentations of the host partner and technical presentation of all partners.
- A general project meeting in Wuerzburg, Germany, September 21st-22nd with tutorial presentations of the host partner and technical presentation of all partners.

7.2.2 Task 6.2 – Technical and scientific management

The transfers of technologies, knowledge and man power inside and outside of SUBTLE as well as the management of result exploitation were the main tasks of the technical and scientific management. This management work was performed by the steering committee which organized several points of intersection in the work between the different partners during the third year. To mention a few, examples within this intense interaction between SUBLTE partners are given:

- A bilateral student exchange between UNIPG and UWUERZ for several weeks was performed.
- Dr. Rafael Sanchez, from the University of Geneva, visited Prof. Hongqi Xu in the University of Lund, from 9 August to 15 August, 2009. During this time, he had the opportunity to visit the laboratories and discussed with the members of the group about their experimental and theoretical work on optical and electronic properties of nanowire devices and spin transport properties and charge detection in quantum dots. On 13 August, 2009, he gave a seminar on "Correlated transport in capacitively coupled conductors".
- Enhanced detection schemes elaborated at UNIPG were managed to be tested at UWUERZ.
- Experiments (UWUERZ) on noise triggered switching and logic operation were modeled by UNIPG.

- Further strategies of exploitations were discussed and realized by applications for different funding schemes. New proposal were submitted.
- Parts of the results of our SUBTLE project were discussed with industry.

7.2.3 Task 6.3 – Dissemination of project results

Also in the third year many results were submitted as papers to scientific journals. Especially IEEE journals were chosen. List of the papers are given in deliverable report D6.3. Many talks of the partners were given at conferences and workshops. The objectives of SUBTLE were also reported in broader public media, like newspapers, broader scientific journals, and the WEB (youtube). The SUBTLE website was improved as recommend by the reviewers.

7.2.4 Task 6.4 – Exploitation activities

The invention of the residence-time detector with the Y-geometry and RTDs as basic ingredients was protected ((WO/2009/106595) SENSOR FOR ELECTROMAGNETIC QUANTITIES AND METHOD FOR MEASURING ELECTROMAGNETIC QUANTITIES). The patent is published: e.g.:
http://www.wipo.int/pctdb/en/wo.jsp?WO=2009106595&IA=EP2009052324&DISPLAY=STATUS
Potential industrial partners were contacted and certain routes for different applications (different wavelengths/energies, different sensitivities, etc.) were discussed.

7.3 Deviations from work programme and corrective actions

No significant deviation from work programme.

7.4 List of deliverables

WP Del. No	Deliverable title	Lead partici-pant	Due date	Delivery date	Estimated person-months	Used person-months
D6.3	Submission of a dissemination and use plan	UWUERZ	M36	M36	0.5	0,5
D6.4	Submission of technology implementation plan	UWUERZ	M36	M36	0,5	0,3
D6.5	Submission of annual technical progress reports	LU	M36	M36	2	1
D6.6	Submission of final project report	UWUERZ	M36	M36	0,5	0,3

All reports were delivered in time.

7.5 List of milestones

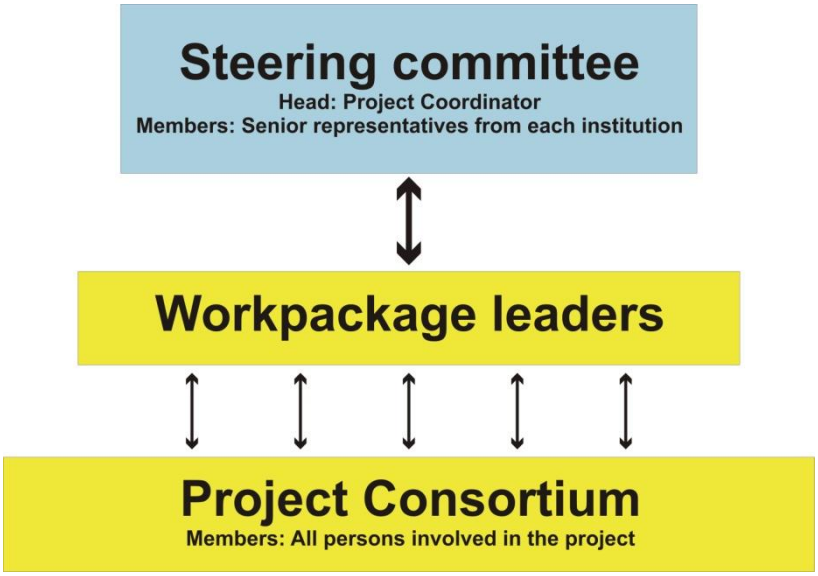
WP Mile-stone	Milestone title	Lead participant	Due date	Delivery date
M6.1	Periodic review of exploitation by exploitation committee	UWUERZ	M36	M36
M6.2	Technology implementation plan	UWUERZ	M36	M36
M6.4	Project completion	UWUERZ	M36	M36

All milestones were achieved.

Section 3- Consortium Management

8. Tasks and Achievements

The project management has to coordinate the different activities and requirements of the project. Six contract partners are spread over five different countries all over Europe and contribute with their expertise to the project. To make the interaction between the partners efficient and to guarantee project success, the project management has the structure shown in the following chart.



The tasks of the different committees are the following:

The **Steering Committee** headed by the project coordinator is responsible for the general management tasks, supervises the correct timing of deliverables and milestones and the sample flow as well as the distribution of results between partners. The status of the sample exchange or any foreseen delay of deliverables/milestones will be periodically reported in the annual progress reports. The steering committee consists of senior representatives who have the authority from their contributing organisation to take any necessary corrective action. The steering committee will produce reports and organize technical presentations to the commission, synthesized by the input from the workpackage leaders. It will analyze the comments of the Commission's reviewers and take any the necessary action to keep the technical aspects of the project on track. It will be responsible to prepare the review meetings at months 12, 24 and 36. The steering committee will serve to identify specific opportunities to exploit major results emerging from the project and identify early valuable intellectual property. Once an intellectual property issue has been identified, the committee will ensure its protection (via patents) in accordance with the consortium contract. The committee will also be responsible for periodic reviews of the state of art and patent situation as well as to produce an exploitation plan for the steering committee. The decision making procedure and issues related to intellectual property and innovations will be defined in detail the Consortium Agreement which follows the guidelines fixed in the model contract. The CA will be a deliverable in WP6. The steering committee will meet regularly at the quarterly meetings and will have overall responsibility for keeping the project goals within the project time table. The committee is also responsible to ensure deliverable and milestone achievements, to

administer the project finances (through the coordinator) and to make strategic re-allocations of resources, re-definitions of tasks and other decisions which impact the project advancement. The coordinator is responsible for the communication with the commission. The steering committee supervises also the technical and scientific work, the results of the project and checks the exploitation possibilities.

The **work package leaders** are responsible for achieving the goals for their specific working area. Its specific tasks will include the review of deliverables and milestones and actions necessary to keep the program on schedule. The work package leaders will produce input for the reports and organize technical presentations. They will analyze the comments of the Commission's reviewers and take the necessary action to keep the technical aspects of the project on track. It will be responsible to prepare the review meetings at months 12, 24 and 36 in close cooperation with the steering committee. They will be involved in all fields of scientific work by a permanent feedback with the project consortium.

8.1 Contractors and consortium

8.1.1 Partner List

No	Participating Institution	Short Name	Country
1	Julius Maximilians Universität Würzburg	UWUERZ	Germany
2	Technical Research Centre Finland	VTT	Finland
3	Lund University	LU	Sweden
4	University of Geneva	UNIGE	Switzerland
5	Dipartimento di Fisica Universita degli Studi Perugia	UNIPG	Italy
6	XENOS Semiconductor Technologies GmbH	XENOS	Germany

8.1.2 Contact information

Contact Information:

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Project Web-site: http://subtle.fisica.unipg.it/SUBTLE

Project Logo: SUBTLE
SUB KT LOW ENERGY TRANSISTORS AND SENSORS

8.2 Project Timetable and Status

Workpackage 1: Theory of electrical switching & sensing	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**
T1.1 Models of optimized SR in NADS and NESN												
T1.2 Modeling of many body effects in eletrochemical capacitance												
T1.3 Role of electrochemical capacitance in non-linear transport												
T1.4 Modeling of magnetic field symmetry of non-linear transport												
T1.5 Shot noise in non-linear regime of multiterminal structures												
Workpackage 2: Technologies for subthermal switching devices												
T2.1 Realization of vertically 2DEGs in GaAs and Si												
T2.2 Patterning technology of laterally coupled conductors												
T2.3 Self-aligned doping of coupled Si nanostructures												
T2.4 E beam pattern controller												
Workpackage 3: EC feedback and single SR devices												
T3.1 Transport and feedback in vertically coupled electron systems												
T3.2 Tailored electrochemical capacitance feedback FETs												
T3.3 SR double-dot channel FETs												
Workpackage 4: SR multiterminal nodes												
T4.1 Integrated bistable feedback FET nodes												
T4.2 Advanced design and layouts												
T4.3 Tunable on-chip noise sources												
T4.4 Artificial neuron nodes												
Workpackage 5: Sensors & noise enhanced switching (UPER)												
T5.1 Residence time detector												
T5.2 Electro/magneto asymmetry senors												
T5.3 Noise enhanced logics												
T5.4 Evaluation of device limits												

In this chart, the timing of each work package is shown, except of work package 6 (project management), which runs through the whole project duration.

8.2.1 Changes of Deliverables

No changes in project goals or deliverables are planned.

8.3 Coordination Activities

8.3.1 Monitoring Deliverables and Milestones

The progress towards maintaining the schedule of deliverables and milestones is monitored carefully by the coordinator. The state of deliverables and milestones is presented, checked and discussed at each quarterly meeting. Deliverables and Milestones which ran the risk of being delayed had been supported by the consortium in collaboration to finish them successfully. Therefore no significant corrective actions, causing a rescheduling of the timetable, were necessary during year two. After consultation with the coordinator, deliverables were combined into a single document after finishing

8.3.2 Quarterly Meetings

Quarterly meetings are held regularly (~every 3 months) with representatives of each partner organization. The meetings are alternating organized and held by the partners. During every meeting, the dates and the location of future meetings were determined. The meetings have the following structure. First the coordinator gives a small welcome and introduction, than the host partner gives a tutorial presentation (only when the respective partner is for the first time the host of such a meeting). Afterwards each partner presents his recent results concerning the deliverables and the milestones. Last point is the checking of status & timing with respect to the time schedule; closing with a discussion on financial issues.

8.3.3 Support Actions for Communication and Reporting

Internal communication was supported by a detailed protocol distributed to the partners after each quarterly meeting tracing the results and describing TO-DO lists of further actions.

The partners did successfully publish and report their results of the SUBTLE project in all major journals and participated in international conferences and workshops. Some of them are also involved in the organization of major conferences. A list with all documented output of the third year is described in deliverable report D6.3, consisting of a large number of publications both in international journals and in conferences. The major achievements of the SUBTLE project do also attend to be of commercial and non-commercial impact. The technology implementation plan is reported in deliverable D6.4.