Project No. 027953

POWERNET

Broadband over powerlines that works and meets the users' expectations

Instrument: Specific Targeted Research (STRP)

Thematic Priority: IST-2004-2.4.4

Final Activity Report

Period covered: from 01/11/2007 to 31/03/2008 **Date of preparation: 12/06/2008**

Start date of project: 01/11/2005 **Duration: 29 months**

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Project coordinator organisation name: TELSCOM AG **Revision: 1.0**

Table of contents

1 Publishable executive summary

POWERNET project started on 1 Nov. 2005, with a small set of partners with the specific expertise suited to realise the Cognitive BPL (CBPL) system, as described in the Description of work. The project consortium has only 5 partners out of which 3 are SMEs, one research institute and one public electric utility company.
The project had an ambitious project objective of design and development CBPL system within in one year for first level of field trials (with off-the-shelf components) so as to confirm the design validation and to develop ASIC for the analog front end, which is one of the complex part of the planned CBPL system. The digital circuits were realized by FPGA, which can be later developed as a digital ASIC to complement analog ASIC for commercial exploitation.
The demonstration units were built according to the specifications laid down and the first set of field trials are carried out between Oct.06- Feb. 07. The results are reported in D4.1 and D5.1 deliverables.
Based on the first set of trials the analog ASIC was developed in the second year, which was available at the end of second year. This chip was tested for its performance and was sent to WP2 to integrate with digital circuit boards and to develop new CBPL demonstrator units with error correction algorithms incorporated.
During the phase 2, WP2 activities designed new interfaces with partitioned HW and SW between Analog board with new ASIC and digital circuits with the improved forward error correction algorithm (Reed-Solomon code) and cognitive algorithm.
In the final phase of the project the focus was the integration of the analog ASIC into the CBPL Demonstrator Units and the second field trials using them. The AFE board was redesigned, the DSP board modified to receive a second ADC and the software adapted accordingly. Following successful integration tests in the laboratory, second set of trials were done during the extended period (Dec.2007 -Mar 2008) and results are documented in the deliverables D4.2 and D5.2.

The CBPL Demonstrator Units were evaluated in the field and compared with PLC modems on the market, following the recommendations from the reviewers to benchmark the results.
The performance investigations included measured data rate, BER, and EM radiation when the CBPL Demonstrator Units were in operation using different transmit PSD and channel bandwidths.
The analysis of measurements leads to expected results: the CBPL Demonstrator Units performed better than the PLC modems on the market while using lower transmit PSD and lower EM radiation.

Dissemination activities continued with number of presentations during the concertation meetings, and conferences, where it received a good response.
The main target of dissemination was however the IEEE P1901 standardization activities.
POWERNET project continued to take an active part in IEEE 1901 standards and have their contribution integrated to Homeplug/Panasonic proposal which has been retained.

The project also received number of enquiries for possible field trials on their electricity distribution networks. Number of contacts were also made for exploitation opportunities. These enquiries will be followed up after the completion of the project.

The project produced number of deliverables, number of them being public can be downloaded from the website www.ist-powernet.org.

The project has contributed to BPL technology innovation, through number of publications and by filing number of patents. The partners have submitted 3 patents (ACN 2 and IMEC: 1). Thus POWERNET is one of the important innovative project, realising valuable IPR increasing their business activity potential and value of the company.

1.1 Objectives of the project and work performed

The main project objective of the POWERNET project is to develop and validate a Cognitive Broadband over Power Lines (CBPL) Demonstration Units that meet the regulatory requirements concerning electro-magnetic (EM) radiation and can deliver high data rates while using with low transmit PSD and working at low signal to noise ratio.
The objectives were set be achieved in 3 phases:
Phase 1/Year 1: System architecture development and building demonstrator units with off the shelf components and to do the feasibility test, for low EMR and low PSD operation, so that analog ASIC can be designed for improved performance. Introduce the CBPL technology into standards.
Phase 2/year 2: Develop the ASIC following specifications drawn-out from the first trials results and to build new CBPL demonstrator units with AFE board (with ASIC), digital cognitive algorithm and error correction incorporated. Contribute to standards and participate actively in dissemination activities.
Phase 3/5 months of year3: Test the integrated system and test in the field for performance and benchmark with the commercial modems. Investigate the exploitation potential with potential investors.

2 Workpackage activities

2.1 Workpackage 1

2.1.1 Objectives

This work package addresses the following objectives of the project management
Administrative: maintain the project management in accordance with the contract and the objectives of the project, including Financial & Legal aspects of funding, payments and reporting. Ensure the IPR of each partner are fairly managed. The activities included contract amendments to extend the project and manage the field trials campaigns.
Conflict Resolution and Risk management are part of project management
Assessment and evaluation: Follow technical activities and assess quality of the work, timing and progress achieved, according to the agreed time plan.
Project reporting: Preparation of periodic management and progress reports
Project linkage and interconnection: Liaison with projects and standards groups

2.1.2 Achievements

The activities of WP1 involved planning of project meetings, agenda preparation and chairing the meeting to discuss all relevant points of contracts, consortium agreement and deliverables. Action points for all partners were defined. During the life time of the project regular audio conferences were orgnised (minimum 1/month) to discuss the progress of the work against each action point defined in the previous meetings. The risk factors were identified and log files of these are maintained.
The meeting reports were prepared for face to face and audio conference meetings, with action points for the period ahead.
In year 1, All contractual procedures were met with new partner SIN who joined the consortium in place of CKW as originally planned. All accession forms were obtained from partners with signatures and sent to the Commission, completing all contractual requirements.
The consortium agreement was prepared, circulated among partners and further improved taking into account all partners comments on all articles and on the IPR issues. The CA was signed by all partners. There were 4 plenary meetings and 2 WP level face to face meetings during the first year.
Completed the project handbook deliverable D1.3 and delivered to the Commission. All administrative procedures regarding the document templates, communication tools (e-mail groups, FTP,et…) are part of D1.3.
Website (D1.2) was installed and is publicly available since Month 1 of the project.
All deliverables due were sent out to the Commission in paper format, in addition to electronic versions submitted before.
Participated in the concertation meeting and presented the project.
Contributed to the FP7 workprogramme on the issues of Powerline communication. Completed the quarterly progress reports (D1.4.X ; X=1-9)) and submitted to the Commission, on time.
Co-ordinated project activities for the technical activities of different workpackages, and supervised the field trials planning and test scenarios for the tests and measurement. Organised the project

meeting towards preparing the field trials. The project results from its first year activities were proposed to the ISPLC conference to be held in Pisa, which is one of the major conference addressing the Powerline communication. All information exchange tools were set up and are operational.

In the year 2, there were 2 plenary meetings and 2 test-campaign meetings. Since there was no second phase field trials during the second year, and only 3 partners were active, project decided to have more audio conferences rather than physical meetings. This also helped on reducing the travel budget and use these for the analog ASIC packaging costs and other components development.
Organised monthly audio conferences for co-ordination across project activity and monitoring the action points defined. During all these meetings the status of activities, any delays and reasons, solutions and replanning were discussed. The risk factors were identified and log files of these are maintained. Additional audio conferences were organised as and when necessary.
All deliverables due were sent out to the Commission in paper format, in addition to electronic versions submitted before.
Towards the first year review held on 14 Dec. 2006, project activity report, project management reports were prepared and submitted along with C-Form with associated Audit certificates from partners.
The project had to undergo 2 review meetings, and one written assessment during the second year, which to some extent downplayed the performance of the consortium plans. The result of the first review resulted in the rejection of 4 WP2 deliverables and deliverables from WP4 and WP5. The project management had to co-ordinate further trials and lab tests to revise these deliverables and to resubmit them during Feb. 07, for the March. review meeting. Even the second review did not provide expected approval of the deliverables, which created major concern among the consortium partners. To remedy this situation, project sought the meeting with the European Commission, which was held on 12 April 2007 in Brussels at EC premises. Meanwhile, project revised the deliverables further answering all clarifications, taking into account the recommendations, and resubmitted them before 30 April 2007. However, the Commission proposed the project to issue a report compiling all the revisions in the new deliverables, and how the questions from the reviewers were answered point by point, in the 2-column report. This was done during May 2007.
This written review resulted in the approval of revised WP2 deliverables, but not D4.1 and D5.1, which received requests for further clarifications. The response to the comments on WP2 deliverables and revised D4.1 and D5.1 were submitted on 13 Sept. 2007 to the Commission. The latter are part of the second year review.
All these co-ordination and communication activity had major workload on the management activities. The resources towards these activities are included in the official quarterly report activities.

During the last phase of the project (Nov-07- Mar.08) was very active period with the second annual review in Dec., followed by preparing the new CBPL Demonstrator Units with ASICs developed by IMEC , conducting trials with commercial and CBPL units, followed by completing all deliverables due until the end of the project, including revisions to some previous deliverables.
Revised the technical annexe requesting the extension of the project until end of Mar.. 2008, to take account of delays in obtaining the ASICs on time and assembled PC boards with new design of CBPL system.

Telscom prepared all annual reports (PAR, PMR; Cost claim documents with audit certificates) for the second annual review held through telephone conference on 3 Dec. 2008. As a precursor, we received number of questions from the reviewers and the answers were compiled from partners activities and provided the clarifications.
This review resulted in the recommendation of 'Continue' with request to modify few deliverables and resubmit. All the revised deliverables were submitted on time to the Commission (D2.6B, D6.2, D4.1 and D5.1).
Organised number of audio meetings to progress the work since the time is very limited between the 2nd review and the end of the project (Mar. 2008).
Sereis of trials were done with commercial modems (to take into account the reviewers recommendations) in the same environment and scenarios as planned in the first and second field trials for benchmaring the results. The second series with few weeks delay with number of CBPL units were conducted and measurements were done. The same has been recorded on video as well, for possible viewing.
Had number of discussions with the project officer regarding the cost claims, since the rejected costs from the first cost claims are not paid.
During this last period number of contacts were established for the possible exploitation opportunities, and presentations were done in the conferences, and to the commercial companies, as well as number of publications in journals were done.
The POWERNET concepts have become part of IEEE1901 standards, in the retained 'Homeplug,/Panasonic' proposal.
Liaison with OPERA was also done in the standards arena to include some part of OPERA proposal into new standards.
Preparation for the next review was undertaken and the date of 23rd May is fixed, to be held in Neuchatel. The agenda proposal was sent to the Project officer. All contractual and review reports were sent to the EC and to the reviewers. The review also had number of demonstrations both in the labs and in the field to demonstrate the operational features of CBPL including cognitive algorithms. The review was successful with acceptance of all project deliverables and demonstrations.

Tablel 1: List of project meetings organised

#	Event name	Date	Location	Purpose/justification/major outcome	Attendee names
1	Kick-off Meeting	O6//10/05	Neuchâtel Switzerland	First Project meeting	All partners, except SIN
2	Meeting at IMEC	25/01/06	Ghent Belgium	Second project meeting	All partners, except CETECOM
3	WP2-WP3 meeting	23-24 Feb. 06	Gent, Belgium	AFE /ASIC discussions	ACN-IMEC
4	Wp2-WP3 Meeting	15-16 March 06	Ghent, Belgium	AFE ASIC Discussion.	ACN-IMEC
5	Plenary meeting	2-3 May 2006	Sarbrücken Germany	Third project Meeting: Work progress monitoting, planning,..	All partners

6	Field Trial Preparation	Sep. 2006	Neuchâtel	Visit to potential locations for the field trials to representatively select the test locations and to arrange the test set-ups optimally.	B. Rebmann, C. Picci, S. Horvath, evtl. others
7	Plenary meeting	24-25 Sept 2006	Neuchatel Switzerland	Fourth project Meeting Visit to field trials location	All partners
8	Test Campaign 1	06. – 10. Nov .2006	Neuchatel	Performing EM Radiation Measurements as required for the POWERNET project	Tesl: S:. Rao ACN : S. Horvath, A. Boss, Cetecom: F. Coulet, M. Burkholz U. Nauertz
9	Review prep. Meeting	7-8/12/06	Neuchatel	Project meeting and review preparatio meeting,	All parners
10	Review meeting	14/12/06	Geneva	Project review	All partners
11	Test Campaign 2	15. – 20. Jan. 2007	Neuchatel	Performing EM Radiation Measurements as required for the PowerNet project	Tesl: S:. Rao ACN : S. Horvath, A. Boss, Cetecom: F. Coulet, M. Burkholz
12	Project meeting	4-5 Feb. 07	Gent	Project progress and planning activities	All partners
13	Project review	7 Mar. 07	Neuchatel	Project assessment- preparation and review	All partners
14	EC-Consortium meeting	12 Apr. 07	Brussels	Project review related issues with Mr. Zimmerman and Mr. Jorge Carvalho	All partners
15	Project review meeting	3 Dec. 2007	Virtual through audio	Second year review	All partners, PO and reviewers
16	Test Campaign 2	20-22 Feb 2008	Neuchatel	Performing EM Radiation Measurements as required for the POWERNET project	ACN : S. Horvath, A. Boss, Cetecom: F. Coulet, M. Burkholz U. Nauertz
17	Test Campaign 2	13-14 Mar. 2008	Neuchatel	Performing EM Radiation Measurements as required for the PowerNet project	Tesl: S:. Rao ACN : S. Horvath, A. Boss, Cetecom: M. Burkholz SIN: C. Picchi
18	29xMonthly Audio conference + adhoc audio meetings	2nd Thurs of the month	Virtual	Project progress monitoring, planning,	All partners

2.1.3 Deliverables list

Del. no.	Deliverable name
D1.1	Project presentation
D1.2	POWERNET Website
D.13	Project Handbook
D1.4.X	Periodical Progress Reports, X= 1-9
I.X	Number of reports: PAR, PMR and C forms
D1.5	Final Report
	Final activity report
	Final management report
	Final financial report

2.1.4 Milestones list

Milestone no.	Milestone name
M1.1	Project presentation
M1.2	First year review
M1.3	Second year review
M1.4	Third year review planning

2.2 Workpackage 2

2.2.1 Objectives

The main objective of this WP was to develop the system architecture and realize the CBPL Demonstrator Units with hardware and software integration to be used in the first field trials. Following successful system test, develop the cognitive algorithms and error correction schemes during the second year. With the ASIC from WP3 available, redesign AFE board and integrate with digital circuits with cognitive algorithms and error correction schemes so as to have working demonstrator units that can be deployed and tested in the field.

2.2.2 Achievements

During the first year, the system architecture and the resulting HW + SW partitioning for the CBPL system to be used in the first field trials was agreed during the first month of the project activities. Investigated different HW, SW and FPGA (Field Programmable Gate Arrays) concepts and defined the following key features of the selected system architecture:

- Selected the HW-SW partitioning together with the definition of the tasks allocated to the two FPGAs on the DSP board.
- Investigated the AFE functions trade-offs with respect to their implementation using analog processing or digital processing. The super-heterodyne receiver architecture chosen takes care of the specified high dynamic range.
- Allocated the functions of the CPU board and the DSP board, respectively.
- Worked out the specifications of the Power Supply board
- Defined SW architecture

Following this analysis, the project focused on the circuitry design of the different HW boards:

CPU Board
The CPU board will provide the data interfaces (Ehternet LAN USB, WiFi) of the CBPL equipment. Two different RISC microprocessors, the Strongarm 1110 and the Intel xScale IXP425, are presently shortlisted. The selected microprocessor will also provide user interface and the element manager based on SNMP.

DSP Board
The CPU board will communicate with the DSP board. The DSP board will have the following components: a TI DSP, two Gate Arrays, two DACs and one ADC. The DSP chosen has floating point operation. It will be mainly used to calculate the coefficients of the equalizer, the frequency offset detection and correction.
The Gate Arrays will perform all real-time processing tasks like the synchronization, the DFB modulation schemes and the equalizer.
The DSP board will also realize the digital to analog conversion (the second DAC is foreseen for the echo canceller) and the analog to digital conversion. The ADC and the DACs will have 14 bit resolution.

AFE Board

The AFE board will do all the analog post-filtering and amplification of the transmit signal and the pre-processing of the received analog signal. It will make all the necessary bandpass filtering, amplification and up-conversion needed to perform bandpass sampling of the received signal.
Significant efforts were spent also by IMEC for investigating the CBPL architecture and the building blocks of the AFE design.
IMEC understood many aspects of the technology on both the system level and AFE board level before we can address the ASIC design. Some critical simulations were done at IMEC for the proper definition of the AFE specifications together with ACN. Moreover, valuable contributions have been given to ACN during discussions via mails and conference calls.

Power Supply Board

The Power Supply board will provide all the necessary voltages together with the coupling unit. Concretely, the analog transmit signal coming from the AFE board for transmission, and the received signal will be de-coupled from the electric line by the Power Supply board and forwarded to the AFE board. The coupling to the power grid is done on the Power Supply board, which is connected to the output and respectively to the input of the DSP board. The analog transmit signal coming from the AFE coupling unit for transmission, and the received signal will be de-coupled from the electric line by the Power Supply board and forwarded to the AFE board.

FPGA Design

The partitioning of the tasks of two FPGAs has been done. The first FPGA will implement all operations carried out on over-sampled data, while the second FPGA will realize all the functionalities remaining after the down-sampling.
The DFB has been coded in VHDL and tested. The programming of the FPGAs in VHDL code has been carried out according the plan. The synchronization, the time-domain equalizer have been implemented and tested.

The final version of the HW includes:

- An AFE board is using SAW filters to isolate the frequency band of interest. The AFE board circuit design has been completed and reviewed. The AFE boards ordered.
- The circuitry design of the CPU board, of the DSP board and of the Power Supply board has been completed, reviewed and the corresponding PCBs for 8 CBPL demonstrator units ordered.

The AFE board is connected to the DSP board, which forwards to the AFE board the data to be sent. On the other hand, the AFE board forwards the received and processed data (by the AFE board) to the FPGAs . Corresponding functional tests have been worked out.
The interfaces to the data network (Ethernet) are on the CPU board. The CPU board sends data to be transmitted to the FPGAs on the DSP board. The CPU board is using a StrongARM 1110 RISC microprocessor. This microprocessor is going to be phased out and shall be replaced by an Xscale IXP 425 microprocessor in the final version of the CBPL equipment.
The PCBs and all the components for 10 CBPL equipment units ordered. Once received, they were assembled and tested in the labs. The board level tests were carried out with the CPU board, the DSP board, the AFE board and the PS board. The final system integration tests have been completed with these tested boards.

SW Design
The SW architecture has been worked out. Basically, all functions related to network interfaces, user interfaces, network management will be realized in software on the microprocessor of the CPU board. The CPU will employ thereby a Linux kernel.
The SW running on the DSP will take care of the DMA needed to load or download the FPGAs, receive and send the data to the AFE board, and to allocate the thereby needed SDRAM locations. The DSP will use a strongly simplified, proprietary O/S.
Telscom compiled information related to CBPL system requirement from SW perspective to address configuration, set up and operation. The SW architecture and functional blocks are studied. The IP stack has been installed with LINUX operational system and some of the communication protocols are being tested. The SNMP MIBs are being studied and relevant information are being compiled.
The software architecture has been finalized. While the CPU board is using Linux, the DSP board has a self-developed small O/S. The DMAs on the DSP ensure fast delivery of data to be transmitted and received data.
Major parts of the software have been coded and tested under real-time conditions. The state-machines coded and verified.
SW development activities between ACN and Telscom was agreed. While ACN is implementing SW for the PHY and MAC layers, Telscom will concentrate to develop and/or validate application SW running at level 3 and above. Telscom is working on the SW development to improve the QoS and network management based on SNMP. SW development has started on these functionalities and first implementations hav been completed and were demonstrated to ACN team. Number of applications have been chosen such as VoIP with interworking with ISDN/PSTN gateway, Video streaming, so that functionalities of QoS, security and management SW can be demonstrated effectively.

In the second year, due to requests to improve the WP2 deliverables from the first year to include the BER measurements, additional tests had to be done with the CBPL Demonstration Units developed in the first year. With all the improvements and tests done according to the recommendations of the reviewers, the deliverables were revised and submitted multiple times: for the first review in Mar. 07, second one in Apr. 07, and the last one after the written review in Sept. 07. Towards developing new CBPL Demonstrator Units with the analog ASICs inclusion on the AFE board, FEC and additional SW functionalities have been developed and implemented.
To further reduce the BER, ACN implemented a Forward Error Correction (FEC) scheme using Reed Solomon code, where the encoding and decoding operations require the use of Galois Field Arithmetic in GF(2^8). The implementation supports standard and shortened Reed-Solomon codes.
The Reed Solomon code has been first simulated in MATLAB and implemented in VHDL code. The Reed-Solomon code has 32 parity symbols and therefore the capability of correcting up to 16 symbol errors within a codeword up to 255 symbols.
The VHDL implemented Reed-Solomon code has been integrated in the FPGA and has been tested using test-benches. Additional MATLAB simulations have been carried out showing that a concatenated Reed-Solomon code (as a FEC) leads to an important reduction of the BER measured compared with only using Trellis Code Modulation (TCM): a measured BER of 10^{-3} using only TCM will result in a BER of 10^{-9} if Reed-Solomon is employed as a FEC. The VHDL code has been tested using the MATLAB generated testbenches.

Results of the additional system tests with the implemented FEC carried out in the Lab, over the LV distribution network and over the MV power grid indicate that the performance of the CBPL technology compares favourably with the performance of alternative BPL technologies.
The aggregate payload and aggregate PHY data rates derived from the measured payloads during the System Test correspond to previous MATLAB simulations. The Deliverable D2.6 "Report on System Test" has been completed.
Additionally, a MATLAB simulation of a block Turbo code (BTC) has been realized to investigate the performance of these codes regarding BER and the delay issues associated with them.
It has been shown that Turbo codes provide the same BER at lower a SNR level (nearer to the Shannon limit). The major drawback of Turbo codes, which is latency is still being investigated. It is hoped that this drawback can be mitigated by using advanced parallel processing techniques.
Another FEC code, the Low Density Parity Check (LDPC) Code has been simulated in MATLAB and its performance at low SNR compared with the performance of BTC. Although BTC is quite popular, LDPC codes are presently gaining interest. The iterative decoding required in both codes leads to complex circuitry with the result of latency issues. The challenge is to design a parallel decoding procedure allowing for a lower latency.
The AFE board is presently being redesigned to be able to use the analog ASICs developed by IMEC. The new AFE board will be ready when the ASICs are available. The CBPL Demonstrator Units with the analog ASIC will be used in the second field trials.
Simulations of the ASIC are done to evaluate certain PCB design decisions e.g. the input impedance of the line driver could impact the bandwidth or the dynamic range of the transmitter
The SW functionalities of the CBPL system design and is presently implemented to provide further improvements to SNMP management using the standard MIB. The GUI to manage the parameters are also incorporated.

In the last phase of the project, new CBPL Demonstrator Units were developed with the analog ASICs inclusion on the AFE board, FEC and additional SW functionalities implemented.
To further reduce the BER, ACN implemented a Forward Error Correction (FEC) scheme using Reed Solomon code, where the encoding and decoding operations require the use of Galois Field Arithmetic in GF(2^8). The implementation supports standard and shortened Reed-Solomon codes.
The activities in the last phase included.

- The AFE board was redesigned to integrate the analog ASIC developed in WP3. The DSP board was modified to be able to use a second ADC, and additional VHDL code and DSP software were developed to match the functions of the FPGA to the new AFE board. The redesigned AFE board was laid out, manufactured and assembled.
- The AFE board assembly had to be carried out by an external company, since all the components employed required SMD techniques. Unfortunately, the SMD assembly line reserved for this task was broken and this resulted in an unplanned delay. The schedule for the field trials had to be modified accordingly.
- The Demonstrator Units were modified to be able to work with a channel bandwidth of 60 MHz.

The system integration was quite complicated as the analog ASIC required new interfaces and also because the ASICs were delivered untested.

- Due to the large number of defective analog ASICs, only 18 new AFE boards could be assembled and successfully tested. As a consequence, 18 CBPL Demonstrator Units using the analog ASIC were built.

- The performance of these CBPL Demonstrator Units employing the analog ASIC was investigated in the laboratory and in the final field trials.

2.2.3 Deliverables list

Del. no.	Deliverable name
D2.1	Report on HW Design
D2.2	Report on SW Design
D2.3	Report on FPGA Design
D2.4	Report on AFE Design
D2.5	Report on System Integration
D2.6A	Report on System Test (CO)
D2.6B	Report on System Test (PU)

2.2.4 Milestones list

Milestone no.	Milestone name
M2.1	FPGA tested in the field trials
M2.2	Software available
M2.3	Successful first set of trials
M2.4	Successful second trials (lab and field tests)

2.3 Workpackage 3

2.3.1 Objectives

The main objective of this WP is to design the analog ASIC needed for high sensitivity and for cost-efficiency. The specifications and the design methodology was agreed and the ASIC to be designed and produced. The ASIC requirements have been defined jointly with WP2. Design and get the Analog ASIC fabricated in 2.5 micro bicmos technology, test and supply to WP2 for the redesign and building of revised CBPL demonstrator units.

2.3.2 Achievements

In year 1, though WP3 was palnned to start few months later, it was realised that it is important to understand the System architecture to implement the analog ASIC; WP3 started earlier than planned. WP2 sent a block diagram of the AFE architecture to IMEC after finalisation of system architecture and system partition and there was an intensive exchange of questions and answers concerning the AFE functions and their requirements to ensure that the equipment in the first field trails and the equipment using the analog ASIC designed by IMEC will have the same performance.
An intensive study was performed on all specific problems before Innovative concepts can be created for the ASIC design to meet the challenging requirements of high bit rate, high sensitivity, wide dynamic range and high linearity.
The early activities included:

- Technology selection (CMOS versus SiGe BiCMOS, STMicroelectronics versus Aanalog Devices)
- Acquire new (not yet accessible by many companies/universities) STM 0.25um SiGe BiCMOS 7 RF design kit.
- Installation and learning of this very advanced design kit.
- Investigation of building blocks such as LNA, VGA, on-chip filters to find out what is the technology limitation (no libraries are available)
- Studied commercial available power-line front-ends (big differences with the ACN approach)

WP2 and WP3 worked out jointly the ASIC Requirements for the ASIC to be designed. Several phone conferences have been carried out to discuss the different issues and options. It was important to agree what functions of the AFE board will be integrated in the ASIC and which will be realized by discrete components.
The Deliverable 3.1 “ASIC Requirements” summarizes the functions of the ASIC together with the specifications to be fulfilled.
Different AFE concepts have been analysed by WP2 and discussed with WP3 in order to define the specifications of the analog ASIC. The face-to-face meeting in Ghent on March 15-16, 2006 was organised to better understand the differences between an analog AFE board design and an analog ASIC design for AFE.
Task 3.1 (ASIC specifications) is already started in advance of the planning as this task is related to many aspects of the system.

- WP2 proposed ASIC requirements were evaluated. This involved the translation of top level specs into voltages, currents, dynamic range etc. of the different building blocks and this also involved top level simulations to show the impact of certain requirements and potential risks (e.g. peak to peak voltage resulting from the TX power), which did not become clear in the matlab simulations.
- The ASIC integration of the AFE was evaluated on a block diagram level, which resulted in a detailed architecture study. Based on the current set of requirements and the proposed architectures were analyzed and a preliminary ranking was made based on performance, degree of integration, etc. From these studies it came out that ASIC architecture will be different from the architecture selected in WP2. A very important part of these activities was

to decide which functional parts should be done analog, digital or a combination of both and to trade-off on-chip versus off-chip implementation.

- The technology for the ASIC integration was selected: a 0.25 µm SiGe BiCMOS process from ST Microelectronics. This technology was chosen for its excellent analog performance, and as future safe technology.

For every building block such as the mixer, IF filter, LNA,… target specifications have been defined. The analog ASIC specifications are completed and documented in Deliverable D3.2. Through these specifications, it is clear for the second phase of the project what components will be on-chip or off-chip and what signal processing is required in the analog or the digital domain. The derivation of the ASIC specification took into account these trade-offs and as such, a number of components (e.g. ADC, DAC, etc.) was selected and algorithms were suggested for digital signal processing, especially for the improvement of the image rejection in a Weaver mixer, which is a different type of mixer compared to the first design phase of this project. Other suggestions were made to reduce the peak-to-average power ratio of the multi-carrier signal, to calibrate the line driver in the transmit path, to improve the clock design and distribution on the second AFE board etc. As such our most important contributions to tasks of Final HW design, Final FPGA design, Final Analog Frontend Design and Final System Integration are included in D3.2 because all these aspects are related with each other and in particular the ASIC specifications.
A matlab model (incl. noise and non-linearity) was developed based on the specifications proposed in D3.2 to verify the analog ASIC performance in a multi-carrier scheme. We are now preparing a paper on the ASIC requirements, which we will submit to the ISPLC conference.
The design of the analog ASIC (including task A3.3 “Test Designs” and task A3.4 “ASIC Design”) is on schedule. The building blocks of the RX part are almost finished and compliant to the specifications. The RX part is now being assembled and we are verifying whether all blocks still work well when they are interconnected. The layout of some of the blocks has started and soon, the design of the transmit path will start. If everything goes well, we expect that the design and layout are finished by the end of January as planned in the project proposal.
As a result of first field trials, WP3 and WP2 worked out jointly the ASIC Requirement improvements for the analog ASIC to be designed. Several phone conferences have been carried out to discuss the different issues and options. It was important to agree what functions of the AFE board will be integrated in the analog ASIC and which will be realized by discrete components.
The technology for the analog ASIC integration was selected: a 0.25 µm SiGe BiCMOS process from ST Microelectronics. This technology was chosen for its excellent analog performance, and as future safe technology.
Final Analog Frontend Design and Final System Integration are included in D3.2 because all these aspects are related with each other and in particular the ASIC specifications.
A MATLAB model (incl. noise and non-linearity) was developed based on the specifications proposed in D3.2 to verify the analog ASIC performance in a multi-carrier scheme.
The design and layout of the analog ASIC is finalized. This included the finalization of the different building blocks, testability features, the IO ring, the top level (architecture) followed by the manual layout and post layout simulations and finally the mask generation. As only one MPW run was planned due to time and budget limitations, two different version chips were designed in order to reduce the risk. The first version is the fully functional version as specified in Deliverable D3.2, whereas the second version is a test chip to test the different building blocks separately. In the second chip the inputs and outputs of the building blocks are directly connected to the IO’s of the

chip, which makes it possible to better characterize or debug the different building blocks. The die size of the first chip is 3.5 mm x 3.5 mm, whereas the die size of the test chip is 2.9 mm x 2.9 mm. The package (QFN48) and pinout have been chosen.
The few remaining open points in the specifications (deliverable D3.2) were resolved together with WP2 e.g. the output interface of the TX path has been chosen to be a voltage mode interface.
A paper was written for the ISPLC conference (IEEE International Symposium on Power-Line Communications and Its Applications) which was hold in Pisa, Italy from March 26-28, 2007. This paper focuses on the ASIC requirements to show the feasibility and performance of the ASIC in a multi-carrier system using frequency division multiplexing to achieve co-existence.
The ISPLC conference well attended and a very positive feedback was received. In fact, POWERNET contribution was the only presentation on a BPL system that could operate above 30MHz. Several contributions on channel measurements and modelling showed that this is useful in a number of cases. Moreover, several keynote speakers expressed a high interest to see a practical realization for this part of the spectrum.
The sign-off of the analog ASIC was done and the tape-out took place on the 27th of April.
The bonding diagrams were made and the packaging options were chosen. The order for the packaging was placed and paid in advance to speed up the process. An empty package was ordered to check the footprint.
Deliverable 3.3 “Report on analogue ASIC Design” has been submitted and a patent application has been filed on the innovations of the analog ASIC design.
Test boards to evaluate the analog ASIC performance have been designed and built. As mentioned above, two different chips were designed. A fully functional chip, as specified in D.3.2, and a test chip to evaluate the building blocks individually. However, testing these on-chip blocks is not straightforward because these are optimized to drive on-chip loads (the interconnections and the input impedance of the following stage). On-chip loads usually consist of a low capacitance (below 1pF) and usually a very high resistance, which are easy to drive yielding much lower distortion. As a consequence, these blocks are not able to drive large capacitors (e.g. 20pF) or low-resistance loads(e.g. 50 or 500 ohm). Solutions to test these blocks using 50 Ohm equipment will be discussed in deliverable D.3.4.
As both chips have a different functionality and different pin outs, different test boards have been required. A detailed list of the tests will be part of deliverable D.3.4 (e.g. noise, distortion, offset, bandwidth, etc. for different settings, signal levels, frequencies, etc.). It is clear that a good choice of measurements and a good test strategy is required. Regularly, conference calls were organized with WP2, concerning the AFE board redesign.
The test results are very good. Both chips are “first time right” and a very high dynamic range is achieved. As a consequence, the ASIC is suited for integration in the redesigned AFE board. Unfortunately, the samples for the field trials faced several delays caused by the new distributor of STMicroelectronics (delivered on 5/10/2007) and due to the shipment/packaging in San Diego (evacuation due to the fires). As a consequence, these samples have been only recently available.
In the last phase of the project, few remaining open points in the specifications (deliverable D3.2) were resolved together with WP2 e.g. the output interface of the TX path has been chosen to be a voltage mode interface.
Number of journal papers were written with the results obtained from ASIC design and tests, which have been accepted and few are already published.
A fully functional chip, as specified in D3.2, and a test chip to evaluate the building blocks were tested. As both chips have a different functionality and different pin outs, different test boards have

been required. A detailed list of the tests are given in the deliverable D3.4 (e.g. noise, distortion, offset, bandwidth, etc. for different settings, signal levels, frequencies, etc.). Regularly, conference calls were organized with WP2, concerning the AFE board redesign.
A number of additional tests have been done, to show that the wide dynamic range of the ASIC results in a very low error-vector-magnitude (or bit-error-rate) for complex modulation schemes (e.g. 1024 QAM) and that a high number of carriers can be supported. These constellation measurements also showed that a very high attenuation between TX and RX can be supported, and that the ASIC can also be used above 60MHz.
A guide to program the chip was provided to ACN, and a step-by-step list of low level hardware checks for the fast debugging of the AFE boards, including the expected outputs and allowed variations.
Completed the deliverable D3.4 and submitted to the Commission.

2.3.3 Deliverables list

Del. no.	Deliverable name
D3.1	Report on ASIC Requirements
D3.2	Detailed design specifications of Analog ASIC
D3.3	Report on Analogue ASIC design
D3.4	Report on analog ASIC test

2.3.4 Milestones list

Milestone no.	Milestone name
M3.1	Analog ASIC requirements agreed.
M3.2	Delivery of packaged ASICs
M3,3	Delivery of tested ASICs
M3.5	Delivery of tested ASICs

2.4 Workpackage 4

2.4.1 Objectives

The goal of this workpackage is to validate the performance of the CBPL Demonstrator Units in the field, including the activities of WP2 (since there is no deliverable defined in WP2 with the concerned activities).
Two test phases have been planed in the project: one with the CBPL Demonstrator Units using of-the-shelf-components to validate the CBPL technology and the AFE function in the field during the first year before starting the analog ASIC design work; a second test campaign to be carried out with

the final CBPL Demonstrator Units with analog ASIC integrated during the extended period. The first field trials were continued in the second year to do more tests and EM measurements according the review recommendations.

2.4.2 Achievements

Early in the project, exchange of information with WP2 about CBPL system and couplers, towards planning the field trials was undertaken. The pre-activities of the field trials started early in the project related with planning, network configurations, scenarios to be followed, test cases, etc..
A visit of a representative LV transformer station showed that there are different possible installations having advantages and drawbacks. The number of five different testing will be carried out at each location according to plans. It was decided that one of the main issues in the field trials is to prove that CBPL technology can ensure coexistence. The testing will be finalized and available according to plans, if the system would be made available.
Meetings were organised for discussing the organisation of the Field Trials including the discussion about relevant characteristics for the selection of locations.
Planning the preparation of the electrical utilities network of the Neuchâtel town was taken up jointly with SIN to address both medium voltage (8kV) and low voltage (400/230V) Network.
This preparation allowed the provision of information specific to the test.
Discussions with WP2 and definition of the scenarios for the 5 tests campaign resulted in :

- 1 x Medium voltage, 3 different lengths.
- 2 x Distribution network utilities low voltage to the user premises (CBPL modem)
- 2 x interior network of installation, school or administrative office.

Analysis of distribution network and preparation for the field trials with detailed information on topology, location and user types was prepared and distributed to the partners. Produced the reports titled: “introduction to the power distribution network and description of the planed field trials” in double version, (French and English).
The analysis on approximate location of deployment and measurement sites was realised by using the topographical and topological tools, and visited the places in person to assess the suitability. Had multiple meetings with WP2 for finalisation. The locations for the field trials have been selected. The selection has been based on the goals of the field trials. Had discussion on possible test methods and their relevance in the field trials. Information required to optimally select the test locations were identified. "Draft Measurement Guide Cable Attenuation V1.0" is distributed to the consortium. This document also highlights the methods to synchronise transmitter and receiver during the measurements.
CETECOM evaluated the documents as provided by WP2/WP4 on the proposed measurements points in the Neuchâtel network. CETECOM analysed the locations on basis of the documents (photos, network plans, maps, drawings) to prepare for the meeting in Neuchâtel. It was investigated what would be the recommended measuring points (number and kind of tests per location). This was done for all locations.
During the October project meeting all locations were visited and further clarifications were made on the test sessions as to be performed during the field trial campaign.
The selection of the places to be used in the field trials has been completed. Adequate means to carry the CBPL Demonstrator Units have been built.

« Description of the planed field trials Localizszion of the places » document with the photos, topology and network information was distributed to the partners, to facilitate the testing from WP4 was provided to WP5.
The Medium Voltage links to be used have been selected together with WP5.
In view of the planned field trials during Oct-Nov. 2006, the project consortium meeting was organized at the SIN premises on 24-25 Sept. 2006. The project members were taken around the user premises where 10 CBPL units have been installed and being tested,
All necessary precautions were taken for installation of CBPL modems, without intrusion to the normal usage of electrical networks, and priory information on the testing campaign among the user community was done.
Testing in both school and industrial environment has been foreseen and the special procedures were necessary with permission from the authorities for such trials, and they were undertaken. In the case of industrial environment the electrical energy meters were installed at each level so that influence of BPL campaign on normal network can be evaluated.
Aspects of security involved at the field trials location, for the staff involved, and involvement of users and the protection of involved people were of high importance in the organisation of the system installation and the trials planning.
The work done for the preparation of the field trials are summarized in Deliverable D4.1: Report on First Field Trials

In year 2, the field trials were set up in the real powergrid without disturbing normal operation of the electricity distribution. The users were communicated about the planned trials during Nov. 06, and corresponding permissions were obtained from the operational department of SIN .
Authorized personnel was assigned for different users premises to guarantee the security and undisturbed operation. All connections (for modem, low voltage centres and medium voltage premises and distribution units in multi-home environment) were established by the authorized personnel, with a specially built infrastructure. Special tents were installed to be able to work in the rainy environment.
The video recording of the 2.2 km link field trails operation was done so that it could be projected during the review meeting in Geneva. Discussions were held to present the electro-magnetic (EM) radiation measurement following the standard test report. Two CBPL Demonstrator Units were set up for the review meeting, so that reviewers could see the hardware and software in operation.
Deliverable D4.1 was delivered just before the first year review, though the project plan was foreseeing its delivery beginning of year 2. On the recommendations of the reviewers, the second set of field trials was carried out in Jan. 2007 as reported in the revised Deliverable D4.1.
The results obtained of the throughput and BER measurements and the EM radiation measurement results have been analysed as requested. The main findings are:

- The CBPL technology is providing a bandwidth-efficient notching capability.
- The CBPL technology generates low EM radiation in the field.
- The data rates obtained using a 1MHz channel and 2MHz channel are as anticipated by the computer simulations.
- A comparison with equipment on the market is difficult, since the payload and not the PHY data rate has been measured.
- Since no FEC has been used in the field trials, the BER measured are not representative.

Following the recommendations of the reviewers, Deliverable D4.1 was completely revised and a new section 8 entitled “Analysis of Results of the First Field Trials” added. This section reports on the findings of the additional field measurements in connection with the system tests carried out. The results obtained were better than that measured in previous field trials.
In view of foreseen second field trials, new capacitive couplers and inductive couplers have been installed on the medium voltage power grid.
At the same time, tests on the LV distribution network with the commercial BPL euipment on the market has been carried out.

During the last phase of the project, the final selection of the field trials sites was done jointly with the consortium. Two Medium Voltage links have been selected, one of about 450 meters and one of 2,2 km.

Two trials campaign were done during the reporting period, since the first series could not be completed because of non-availability of number of CBPL demonstration units. The first trials were done with the Commercial units in the field and measurements were so that results can be compared to assess the CBPL performance in real life.
SIN undertook installation of equipments and preparing the security procedures for two trials campaigns for both low and medium voltage.
Modification of different coupling was done at medium voltage field trials premises. They conducted various tests with both capacitive and inductive couplings in cooperation with ACN.
Communication with the house owners regarding planned field trials so as to access the infrastructure at their premises, and expected disturbances so that the rapport between SIN and households are protected.
All premises for the field trials were prepared ahead of time and prepared the planning document for the field trials so that tests can start as soon as CETECOM arrives in Neuchatel.
During the trials campaign the SIN electric personnel were stationed at the premises for guaranteeing the safety of personnel, network and equipment.
Results were documented and D4.2 was edited following the reviewers recommendations.

WP4 was the key activity during this final phase of the project. Activities involved are:

- definition of the conditions, under which the field trial tests shall be performed to ensure a better correlation between the performance testing and the testing which is performed under WP5.
- definition of the test plan as well as the definition of parameters to be observed
- Investigations of the performance of the CBPL Demonstrator Units using the analog ASIC carried out in the laboratory.
- Performance measurements of Reed Solomon coding used as a FEC conducted in the laboratory and in the field.
- Selection of the PLC modems on the market to be used in the benchmarking. Performance tests with these modems in the laboratory.
- Work out the performance tests to be conducted during the final field trials (together with SIN and CETECOM).
- Set-up and installation of the CBPL Demonstrator Units using the analog ASIC and the PLC modems for the final field trials.

Deliverable D4.2, entitled “Final Field Trials” describes how the integration of the analog ASIC has been carried out and summarized the different set-ups considered during the field trials to validate the CBPL technology.
D4.2 includes WP2 activities as well, since there was no deliverable planed within WP2.

2.4.3 Deliverables list

Del. no.	Deliverable name
D4.1	Report on First Field Trials
D4.2	Final Report on First Field Trials

2.4.4 Milestones list

Milestone no.	Milestone name
M4.1	Successful completion of first field trials
M4.2	Successful completion of second field trials

2.5 Workpackage 5

2.5.1 Objectives

The objective of this work package is to conduct EM measurements in real user environments available during field trials. All the EM measurements have been carried out as specified in regulatory requirement documents.
Experienced experts have done these EM measurements and to avoid unnecessary discussions about the results of the field trials and all results have been precisely documented.

2.5.2 Achievements/progress

Although the main work was planned to start later in the project, first evaluations of standard test methods were initiated early in the project (incl. first assessment of their applicability for CBPL and field trials).
Pre-activities on the measurement issues, scenarios and evaluation methods were discussed, towards planned field trials. Meeting between the concerned parties was organised.
Test cases to be performed in the Field Trials were prepared. The preparation included the analysis of the standardization status for the different test cases. As there was no decision within the allocated working groups of standards, CETECOM provided their view on relevant test cases to the PowerNet project.

Prepared radiated emission measurements and demonstrated a typical test set-up (real-life demonstration outside of a building) as basis for technical discussions for the testing, during the plenary meeting. Prepared a draft measurement guide to measure the attenuation on the power line cabling in the relevant frequency area (Evaluation of the cable characteristics between two termination points in the power line network).
Provision of a Technical Guide "PLC Measurement Campaign" was prepared - In-situ measurement set-up and process for power line communication networks in the frequency range from 1 MHz to 30 MHz.
First evaluations of automation capabilities for the relevant test cases (number of sites and different tested values requires an automated test performance) were conducted.
Several Ethernet protocol testing procedures have been worked out and evaluated in the laboratory.
Specifically, the formerly distributed “Measurement Guide V1.0” was revised. Beside some editorial changes, the most severe technical change was the addition of a test campaign for conducted measurements (using a current clamp) as complementation for the radiated test
Related Document: Draft Measurement Guide V2.0 is made available to the consortium.
The measurement approach proposed by CETECOM has been analysed and compared with other proposals. The channel measurements done for the IEEE standardisation has been also studied and used in the comparison.
It was decided with CETECOM and SIN to use the proposed measurement methods in the field trails. It was agreed however that the measurement methods was finalized (and if necessary improved) during the September meeting.
The standards are being followed for the tests to be followed in different test and measurement scenarios.
On basis of the latest discussions on the tests, which are to be performed in the field trials (WP4/WP5) CETECOM had to re-design its measurement software. Some hardware components needed to be exchanged to meet the expected accuracy. This lead to further alignments in the test software. CETECOM made sample set-ups to verify the appropriateness of the tests as they are proposed for the field trial measurement campaigns.
CETECOM built a new set of coupling network for performing the tests at the expected quality. Two new designs were set-up and compared. After validation tests were performed a second sample of the coupling network based on one of the solutions was built. The two achieved coupling networks were validated in detail. Measurements of the single components are available at CETECOM (documentation of validation). The newly validated coupling networks have been put into a test set-up to verify the optimal function.
During the October project meeting all locations were visited and further clarifications could be made on the test sessions as to be performed during the field trial campaign.
Cross-check of the PowerNet test plan with activities from other projects such as OPERA. D5.1 provides the results of the first year measurement campaign.

The first test campaign was held from November 6th through November 10th 2006. During that campaign EM radiation measurements were performed at the MV and the LV distribution network of the city of Neuchatel. The EM radiation measurements were performed at the transformer stations as well as residential homes, always following the measurement recommendations as defined in MV05. The first results were provided in a preliminary test report, which was available at the first review meeting.

The second test campaign was performed from January 15th through January 20th 2007. The focus of that test campaign lay in the EM radiation tests for In-house CBPL application as well as combined Inhouse/Access CBPL applications. These tests were performed in a school building, which was selected during the preparation of the entire test program. Further, tests were carried out to define the quasi-peak-to-peak correlation, which is required to assess the results with respect to national and/or regional specifications (such as NB30 or FCC). The results of the EM measurements are reported in the Deliverable D5.1. The document strategy for achieving complete and consistent results was selected in a way, that the results of WP4 (field trials, performance) were reported in D4.1 and the results of WP5 (EM radiation measurements) were reported in D5.1, both documents referring to each other to display the full view (radiation vs. performance, etc.). During the review process of the project the reviewers requested to bring more visibility in the correlation of the documents D4.1 and D5.1. Therefore, several revisions of these documents had to be made. After clarifying some further issues during the April 12 meeting in Brussels, the revised deliverable with correlation results obtained with the measurements was resubmitted during Sept. 07 as input for the 2nd year review.
Field trials at 3 different locations were set up for the Mar. 2007 review meeting, so that reviewers could see in person, the performance of the CBPL Demonstrator units in real user environment.
Results of the Deliverable D5.1 have been also taken as an input to the assessment of the results obtained reported in the Deliverable WP4. All results from D5.1 (and D4.1) were submitted to the project partners to assess the results with respect to impacts this might have for the next version of product implementation (ASIC, etc.). Furthermore, an assessment on basis of relevant regulatory documents (FCC Part 15) has been made. This assessment is stated a project-internal document as basis for further activities within the project.
A small benchmarking test over the LV distribution used in the first field trials has been conducted with two BPL modems on the market (that have been recommended by the reviewers). The goal was to compare their performance over the same LV distribution network. with the measured performance of CBPL Demonstrator Units Both BPL modems were not able to establish a reliable connection. The maximum data rate measured was 200 kb/s, with one of them.

In the last phase of the project, the test campaign for the second field trials were planned for Jan/Feb. 2008, with an assumption that CBPL modems will be available by that time. The team worked out a proposal following the settled and well-accepted test standards for EMC testing. According to that the in-situ measurement will be following the test standards BNetzA 413 MV 05: December 2007 (former RegTP 322 MV 05). Furthermore, there were still activities required for cleaning up documents from the review of the first contractual year (D4.1 and D5.1).
The actual test campaign was moved to Feb. 2008, with a renewed plan. However, even during this period the CBPL modems were not available due to various difficulties.
In February and March 2008 CETECOM ICT Services performed the EM radiation measurements as defined in WP5 during the final field trials in Neuchâtel. With the support of ACN and SIN all locations which were selected for performing the EM radiation measurements were accessible. CETECOM performed the EM radiation measurements in two test sessions.
The first test session took part from 20.02.2008 through 22.02.2008. In that session mainly the investigation of performance and EM radiation of "Off-the-Shelf" products from the market was in the focus, completed by in-development tests for the CBPL devices which were in the stage of optimization before release at that time. The results of these measurements are collected and reported in the deliverable D5.2.

The second test session was performed from 13.03.2008 through 14.03.2008. In that session the thorough evaluation of EM radiation at a well-monitored performance was in the focus. For each of the measurements, the performance relevant data as often discussed in the course of the project review meetings was monitored and recorded during the EM radiation measurements. The results of those EM radiation measurements are presented in the deliverable D5.2. Completed the D5.2 by the evaluation of the results with respect to the expected behaviour of the CBPL products in a higher volume deployment in typical power mains networks. To enable the leader of WP2 and the representatives of the network operator (SIN) to perform such evaluation, the test results were provided. A correlative analysis of the data rates, BER, and EM radiation were measured when the CBPL Demonstrator Units were in operation using different PSD and channel bandwidths (together with SIN). By thoroughly weighting the achieved performance at specific transmission configurations with the resulting EM radiation this assessment could be made. This statement which is contained in D5.2 refers to both results those reported in D4.2 (Performance in the Field Trials) and those reported in D5.2 (EM radiation in the Field Trials).

2.5.3 Deliverables list

Del. no.	Deliverable name
D5.1	Report on First Measurements
D5.2	Report on Final Measurements

2.5.4 Milestones list

Milestone no.	Milestone name
M5.1	Successful measurements in the real world environment
M5.2	Successful measurements in the real world environment

2.6 Workpackage 6

2.6.1 Objectives

The objectives of this WP include:

- **Dissemination:** Awareness creation through on-line web site, publications and participation in conferences, workshops and concertation process in the IST framework.
- **Clustering and Standardisation:** BPL/PLC technologies related issues will be discussed in the cluster group, standards to be followed and contributions to be made
- **Liaison:** collaboration and integration with scientific standard bodies.

- **Exploitation:** Define the exploitation strategies.

2.6.2 Achievements

As soon as the project started the project logo was designed, which was accepted by the consortium.
The domain name of www.ist-powenet.org was registered for the project website. The website itself was designed and after approval by project partners the project web site was officially launched with the contents, during M2 ahead of plan.
The first deliverable D1.1 was edited and submitted to the Commission and is also made available for public download.
The Press release was prepared and has been circulated through different channels.
Participated in the Broadband Europe conference and in the convergence workshop, where the CBPL issues were contributed to the panel discussions.
Contacts with OPERA and IEEE PLC working groups have been established. Now this has been extended to OPERA II to be started soon, to our understanding.
The public project information as requested by the Commission was delivered on time.
Participated in the concertation meeting and 'bridging the ICT divide in Europe' workshop in Brussels held on 22 Mar. 2006 and presented how Poewrline infrastructure can be effectively used. Telscom also participated in the Sept. Cluster meeting and organised the traffic monitoring and measurement workshop in the broadband cluster.
Made conference paper proposals to Access'2006 conference to be held in Athens in Sept, and to Net@Home conference. The paper was accepted to be presented at Access'2006 international conference, but that was not the case with Net@Home event.
Contributed to FP7 workplan discussions on the access networks area and reseach challenges ahead.

CETECOM as a member of ETSI contributed to DKE/UK 767.17, AK3 PLC; on the comment resolution processes for EN 50 471, EMC – Product Family; Emission Standard for Wire-Line Telecommunications Networks (including PLC). They also hosted will hosted the Bitkom PLC meeting in Saarbrücken.They als Participated in the PLC workshop and panel discussion during CeBit 2006. Participated in the ETSI NGN@Home Plugtests Event for Triple Play over Broadband Technologies. In this event, CETECOM supported the ETSI Plugtests Services by organising the event with respect to the technical aspects of broadband transmission in the access network and in the preparation of the PLC testing part of that event. As the event was held by ETSI too early in the current project, no solution could be provided. The provision of the test plans and the test schedules (provided by ETSI delegates of Sagem) was observed by CETECOM and aligned with further activities in the event.
Information on the current POWERNET project was included in the June 2006 edition of CETECOM´s Newsletter which is distributed to customers and partners of CETECOM as well as to further recipients. This was done as a further step in the networking around the POWERNET project and the CBPL technology.
The current developments in the standardization are being followed as a member of ETSI, very closely

The ETSI and IEEE activities in this area are being followed. The contact with OPERA is being renewed for joint activities in the standards area, but there was no response. Also a proposal for PLC session in Broadband Europe conference was proposed and it has been accepted.

Stephan Horvath attended to the IEEE standardization meeting in Tokyo, with ACN being a member of IEEE. The meeting focused on the Technical Requirements. Coexistence is a main requirement for the new BPL standard. The CBPL technology employed in POWERNET is therefore well placed to play an important role. Next to coexistence, there are requirements for the Access and In-House applications. Once there is an agreement about the Technical Requirements, the proper standardization will start.

There was joint meeting in Sofia-Antipolis (France) together with ETSI in September. During this meeting the Technical Requirements for the Access and In-House was discussed. Thee down-selection process for the BPL standard shall begin in November in San Francisco. The goal is to have a draft standard by March 2007. ACN plans to attend from now-on to all next meetings. The reports of these meeting were sent to the Commission for information.

ICT summit is being organized in Lausanne on 4 Dec. 2006, to disseminate information to Swiss researchers. Broadband Europe conference is being organised in Geneva during 11-14 Dec. 2006, with Telscom taking a leading role.

Telscom organised a networking session during IST2006, in Helsinki to discuss future Networking issues, and contributed different aspects of networking issues, including the Powerline communication, and the challenges involved.
Telscom participated actively in organising the Broadband Europe conference held in Geneva (11-14 Dec. 2006). Presented the latest results from the first set of electro-magnetic (EM) radiation, to the conference, which received very positive response from the audience.
Telscom also organised the Interworking 2006 conference in Santiago, Chile in co-operation with BB cluster projects. The results of POWERNET were presented to the audience, and considerable interest was shown by NTT for possible industrial exploitation, once the project is completed.
Similar interest was expressed by delegates from Brazil and Chile to extend the Internet connectivity to the rural and semi-urban areas in particular.
Contributed to the AFRICA 2007 conference with a paper, which was accepted against the tough competition. However, we could not go personally due to prevailing status of the project.
Liaison with Opera 2 has been established and maintained.
The paper presented in the ISPLC conference in PISA drew high interest among the participants.
Another paper showing the latest results has been submitted to the Broadband Europe 2007 conference. The paper has been accepted for presentation at the conference.
The results and factsheets of POWERNET were sent to IST results service for possible exploitation interest development.
Number of contacts to industrial companies have been established. Enquiries from ABB, a Malaysian electricity distribution company have been received. These companies are showing interest in POWERNET technology. IBM and Siemens have also shown interest the CBPL technology and are in contact with ACN .
The deliverable D6.2 was completed and submitted.
The CBPL technology used in POWERNET was proposed to IEEE P1901 standards working group. ACN actively participated in the WG meetings and contributed to HomePlug/Panasonic Merged Proposals.

The submitted proposals for IEEE standardization have to consider at least one of the three clusters (Coexistence, Access, and In-Home) defined by the committee. Coexistence issues and related procedures have been addressed and discussed by ACN with CEPCA.
As mentioned above, the CBPL technology has been partly integrated into the HomePlug/Panasonic Merged Proposals for In-Home and Access. ACN did a short presentation during the Boston meeting highlighting the features of the band-pass wavelet OFDM technology that has been added when merging the proposals. ACN's presentation has been well received.
The HomePlug/Panasonic Merged Proposals have been selected for the draft IEEE P1901 standard, need however to be confirmed. The rules states that they have to receive 75% of the votes.

Three patents have been filed by the projects during the last year:
ACN has filed 2 applications:

- Method For Robust Synchronization Of A Multi-Carrier Transceiver Using A Digital Filter Bank And Corresponding Receiver
- Method and Apparatus to Quarantee

IMEC has filed its patent application for

- "Communication System Over A Power Line Distribution Network"

Swiss ICT summit was organized in Witnerthur, Switzerland on 16 Dec. 2007, to disseminate information to Swiss researchers. Broadband Europe conference was organised in Antwerpen during 3-6 Dec. 2007, with Telscom taking a leading role.

In the last phase of the project, Telscom co-organised the Swiss ICT summit on 17 Nov. 2008. in Winterthur and presented the POWERNET poster.
Telscom participated actively in organising the Broadband Europe conference held in Antwerpen (3-6 Dec. 2007). Presented the latest results from the trials held in the project, to the conference, which received very positive response from the audience.
Presented a paper to Africa-Middle East NGN summit with number of African operators and industries participation. The event itself was a commercial event and hence the results presented were towards finding opportunities for the possible exploitation in Africa, bridging the prevailing ICT divide in that continent. The Govt. agencies showed high interest in possible field trials, which will be followed up after the successful completion of the second trials.
Number of contacts to industrial companies have been established. Enquiries from ABB, a Malaysian electricity distribution company have been received. These companies are showing interest in POWERNET technology. IBM and Siemens have also shown interest the CBPL technology and are in contact with ACN. Number of agencies in India have shown interest to conduct field trials and are in touch with Telscom and ACN in this context.
The CBPL technology used in POWERNET has been proposed by ACN to IEEE P1901 standards working group. ACN has actively participated in the WG meetings and contributed to HomePlug/Panasonic Merged Proposals.
ACN has actively participated in the IEEE Standardization meetings in San Francisco, USA and in Fukuoka, Japan:

- There was a two-day discussion concerning the Access industry needs and requirements in San Francisco. This cooperative effort should lead to the 75% votes needed for the Draft Standard.

- In Fukuoka, down-selection votes have been carried out concerning the Merged Proposals for the Coexistence Cluster. The Merger Proposal of HomePlug-CEPCA (to which ACN is a contributor) has received 78% of the votes. The Merged Proposal of UPA-Mitsubishi has been down-selected.

With these last votes, the CBPL technology used in POWERNET is part of all three survival proposals concerning In-Home, Access and Coexistence.
The next steps are as follows:

- A revised version of the survival Merged Proposals are due for April 18, 2008.
- The confirmation votes will be carried out during the week of July 7-11, 2008, in Miami, USA.

ACN has become a member of the ITU-T SG15/Q4 standardization committee and has already made three contributions, the first one in Bordeaux and the two others in Charleston, USA:
- Bandwidth-Efficient Coexistence Techniques
- Proposal for Wavelet-OFDM modulation
- Coherence bandwidth, RMS delay spread and tone spacing

The contributions are all related to the CBPL technology used in POWERNET. All three contributions were well received
The submitted proposals for IEEE standardization have to consider at least one of the three clusters (Coexistence, Access, and In-Home) defined by the committee. Coexistence issues and related procedures have been addressed and discussed by ACN with CEPCA.
The HomePlug/Panasonic Merged Proposals have been selected for the draft IEEE P1901 standard, need however to be confirmed. The rules states that they have to receive 75% of the votes.

IMEC has published two journal papers:

J. Bauwelinck, E. De Backer, C. Mélange, E. Matei, P. Ossieur, X.Z. Qiu, J. Vandewege, S. Horvath, “High dynamic range 60 MHz powerline front-end IC”, *IET Electronics Letters*, vol. 44, no. 5, Feb. 2008, pp. 348-349.

E. De Backer, J. Bauwelinck, C. Mélange, E. Matei, P. Ossieur, X.Z. Qiu, J. Vandewege, S. Horvath, “2.5 V, 35 dBm IIP3, 75 MHz 6th order active RC filter”, *IET Electronics Letters*, vol. 44, no. 7, Mar. 2008, pp. 466-467.

Four other journal papers, focusing on the 1024 QAM constellation measurements and some interesting building blocks of the ASIC, are under preparation.

IPR isuses

Three patents have been filed by the projects during the last year:

ACN has filed 2 applications:

- Method For Robust Synchronization Of A Multi-Carrier Transceiver Using A Digital Filter Bank And Corresponding Receiver
- Method and Apparatus to Quarantee

IMEC has filed its patent application for

- "Communication System Over A Power Line Distribution Network"

The deliverable D6.3 and D6.4 were completed and submitted.

Dissmination activities Summary

Date	Paper title	Conference/Workshop	Place	Authors
Jan. 2006	Website	Open to public	World	*Telscom*
Jan. 2006	POWERNET: European Commission funds development of new Broadband over Powerlines access technology	Press Release	World	*Consortium*
Oct. 2006	Powernet: New drive into powerline technology	CETECOM newsletter	Europe and USA	*Cetecom*
15 Dec. 2006	Powerline communication - a solution for broadband access	Broadband Europe and Convergence Workshop	Bordeaux, France	S. Rao
21-22 Mar. 2006	Use of ubiquitous powerline infrastructure for providing broadband access to bridge the ICT divide	Concertation Meeting: Bridging the ICT divide	Brussels	S. Rao
29 March 2006	BPL technology: Comparison of known techniques	IEEE P1901 and P1675 Standardization Meetings	Orlando USA	S. Horvath
March 2006	Standards on PLC and measurement methods	BITKOM PLC Meeting	Saar-brücken	A. Ehre
April 2006	Broadband over Power lines to bridge the digital divide	FP7 Consultation Workshop	Brussels	S. Rao

13-16 June 2006	BPL Standardization	IEEE P1901 and P1675 Standardization WG Meeting	Tokyo Japan	S. Horvath
14-16 June 2006	QoS issues in the access networks	ITU workshop	Geneva	S. Rao
11-15 Sept 2006	BPL Standardization Status	IEEE P1901 Standardization WG Meeting	Sofia-Antipolis (Nice)	S. Horvath
3-4 Sept. 2006	Importance of monitoring in performance assessment	Concertation Meeting, Measurement and Monitoring Workshop of BB4ALL Cluster	Brussels	S. Rao
4-5 Sept. 2006	"Broadband for All' using the Power Grid	Access'06 International Conference	Athens	S. Rao S. Horvath
Oct. 2006	POWERNET: New drive into the powerline technology	CETECOM Newsletter	-	A. Ehre
21-23 Nov. 2006	Networking issues of the future	IST 2006 Conference and Networking Sessions	Helsinki	S. Rao
28-30 Nov. 2006	BPL requirements: Technology standards	IEEE P1901 Standardization WG Meeting	San Francisco	S. Horvath
1 Dec. 07	Swiss ICT summit	ICT Presentation	Lausanne	S. Rao
11-14 Dec. 2006	"Broadband for all" over the powerline to bridge the ICT divide in Europe	Broadband Europe	Geneva	S. Rao S. Horvath
15-19 Jan. 2007	Bridging the rural area with ICT over BPL	Interworking 2006	Santiago, Chile	S. Rao
25-27 Jan. 2007	ETSI Standards Group: DKU UK 767.17	ETSI group Meeting	Wurzburg	A. Ehre
22-25 Jan. 2007	BPL requirements: Technology standards	IEEE1901 Standardization WG Meeting	San Francsisco	S. Horvath
26-28 Mar. 2007	Analog Front-End ASIC Requirements for a FDM Broadband Powerline System Enabling Co-Existence	ISPLC conference	PISA	Johann Bauwelinck
9.13 Oct.	CBPL technology	IEEE1901	Edinburgh	S. Horvath

2007	presentation for IEEE	Standardization WG Meeting,		
9-11 May 2007	Powerline Communication: Future of the intelligent home	AFRICA 2007	Maputo, Mozambique	S. Rao
25-26 Sept. 2007	Broadband cluster and future Internet	Concertation Meeting	Brussels	S. Rao
16 Nov. 2007	Technology brokerage event	Swiss ICT Summit	Winterthur	S. Rao
1-6 Dec. 2007	Powerline communication system with alternative technology based on new modulation schemes	Broadband Europe 2007	Antwerpen	S. Rao, S. Horvath, Jan Vandewege
January 2008	A 1024 –QAM analog front-end for broadband powerline communication upto 60 MHz	Journal of solidstate circuits, Vol. 43, January 2008	Journal	J. Bauwelinck, E. De Backer, C. Mélange, E. Matei, P. Ossieur, X.Z. Qiu, J. Vandewege, S. Horvath
3-7 Feb. 2008	A 60MHz 2.5V 0.25µm SiGe BiCMOS Powerline Front-End IC with 99.5dB DR	ISSCC conference (submitted)	San Francisco	Jan Vandewege Johann Bauwelinck
Feb. 2008	High dynamic range 60 MHz powerline front-end IC	IET Electronics Letters, vol. 44, no. 5, Feb. 2008, pp. 348-349	Journal:	J. Bauwelinck, E. De Backer, C. Mélange, E. Matei, P. Ossieur, X.Z. Qiu, J. Vandewege, S. Horvath
Mar. 2008	2.5 V, 35 dBm IIP3, 75 MHz 6th order active RC filter	IET Electronics Letters, vol. 44, no. 7, Mar. 2008, pp. 466-467.	Journal	E. De Backer, J. Bauwelinck, C. Mélange, E. Matei, P. Ossieur, X.Z. Qiu, J. Vandewege, S. Horvath
April 2008	1024 QAM constellation measurements and some	To be decided	Journal	Open

	interesting building blocks of the ASIC			

2.6.3 Deliverables list

Del. no.	Deliverable name
D6.1	Dissemination and Standardization Report
D6.2	Final plans for disseminating the knowledge
D6.3	Report on raising public participation and awareness
D6.4	Exploitation plans

2.6.4 Milestones list

Milestone no.	Milestone name
M6.1	Dissemination and standardization plans
M6.2	Dissemination report and exploitation plans
D6.3	Awareness creation report
M6.4	Dissemination report and exploitation plans

2.6.5 Exploitation potential of partners

Exploitable Knowledge (description)	**Exploitable product(s) or measure(s)**	**Sector(s)** of application	Timetable for commercial use	Patents or other IPR protection	**Owner** & Other Partner(s) involved
CBPL system concepts	The new technology has been patented and can be licensed	Home and access networks using the electric utility networks	2008	4 patents in place	ACN
CBPL system solutions	Both HW and SW has been designed and would be available soon.	System and product level exploitation for the mass market in the Access and Home networks	2008 -	More patents are pending	ACN Telscom

Exploitable Knowledge (description)	**Exploitable product(s) or measure(s)**	**Sector(s)** of application	Timetable for commercial use	Patents or other IPR protection	**Owner** & Other Partner(s) involved
New measurement concepts	Automatic measuring system SW conforming to standards	Measurement methods for conformation testing and certification	2007-	Proprietary know-how	CETECOM
2.5 μm BiCMoS design	Expertise in designing analog ASICs	ASIC design	2007 -	Proprietary know-how	IMEC
CBPL demonstrator units with ASIC	Final demonstratable CBPL modems with analog ASIC	Explioatable product for field trials usage with clients	2008	Proprietary know-how	ACN, IMEC

3 Conclusions

POWERNET project addressed the design of new type of communication system over Powerlines based on cognitive concepts and using new technology of digitalfilter banks and asynchronous communication principles with only 5 partners including 3 SMEs and has achieved its set objective in designing, developing, intergrating, testing and conducting field trials in real users environment. The project results have shown significant improved results compared to the commercial products in the market.

The new technology so developed was also part of standardisation discussions in IEEE1901 group, and has become part of accepted standard proposal from Homeplug/Panasonic.

The project also was successful in its dissemination activities across IST programme (concertation process), international conferences, commercial events and publications in the journals.

The project has 3 international patents into its credit, showing innovation aspects of the project.

The partners are very committed to the exploitation of project results in the commercial terms and are discussing with different parties for the possible trials in the short term followed by business prospects.

3.1 Publishable results

POWERNET project has number of public deliverables, which provides the readers the results of the project which are state of the art and of exploitation nature. The website (www.ist-powernet.org) has all public deliverables and publications to access and download.