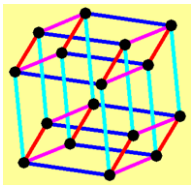
SIXTH FRAMEWORK PROGRAMME, PRIORITY IST-2002-2.3.2.2.2

OPTICAL, OPTO- ELECTRONIC, & PHOTONIC FUNCTIONAL COMPONENTS



synQPSK
Univ. Paderborn, Germany
CeLight Israel
Photline, France
IPAG, Germany
Univ. Duisburg-Essen, Germany

Key components for synchronous optical quadrature phase shift keying transmission

Publishable Final Activity Report

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Period covered: from 01.07.2004 to 30.06.2008
Date of preparation: 15.12.2008
Start date of project: 01.07.2004
Project duration: 48 months
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Participants: UPb, Photline, CIL, UDE
Version: 1.0
Total number of pages: 55

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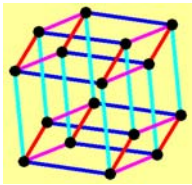

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Photline, France
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Contract No.: FP6-004631
Project Duration: 36 months
Project Website: http://ont.upb.de/synQPSK

For the implementation of synchronous RZ-QPSK transmission with polarization division multiplex this project aims at the realization of all key components which are not commercially available. The symbol rate is 10.7 Gsymbols/s, the bit rate 43 Gbit/s. At least the optoelectronic components shall also perform at 12.5 Gsymbols/s, for operation in combination with super FEC.

Synchronous quadrature phase shift keying (QPSK) transmission combined with return-to-zero (RZ) coding and polarization division multiplex is an extremely attractive modulation format for metropolitan area and long haul fiber communication. Compared to standard intensity modulation the line rate is 4 times lower, the needed number of photons per bit less than half as high, the tolerance to chromatic dispersion and polarization mode dispersion several times better, and the tolerance against fiber nonlinearities, in particular cross phase modulation, is excellent. Moreover, the detected electrical signals are proportional to optical fields. This transfers the advantages of photonic processing 1:1 into the electrical domain. It is (almost) correct to say that "optical signal processing is performed electronically". In particular, all linear optical distortions (polarization transformations, polarization mode dispersion, chromatic dispersion) can be equalized electronically without losses. Synchronous QPSK possesses also distinct advantages over all other modulation formats, in particular duobinary, RZ, DPSK and DQPSK and all variants thereof. These modulation formats receive a lot of interest from researchers who consider synchronous QPSK as too challenging. In fact, the components required for synchronous QPSK are simply not available so far. In the traditional, phase-locked loop based receiver concept this holds especially for lasers with linewidths in the lower kHz region. However, in our concept these are not needed. Rather, the laser linewidth specifications are greatly relaxed due to a novel carrier recovery scheme. It shifts the burden from the lasers to electronic integrated circuits, which can be manufactured at a very low cost in CMOS.

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Introduction

1.1 Workpackage summary

- **WP 1: QPSK modulator development**

  Photline designed and validate the concept of the QPSK modulator integrated on X-cut technology with two first versions. From these preliminary design, the fabrication of the Z-poled QPSK modulator was launched and successfully achieved. It was tested both at the component level and in a DQPSK transmission system architecture. The devices were tested over the full C & L band. Samples were supplied to UpB for the demonstration workpackage. The final devices fulfils all the specifications required in the original proposition. It is in particular characterized by low driving voltage (<5V) and very low insertion loss (<5.5dB)

- **WP 2: 90° hybrid and front-end development**

  CeLight Israel designed and fabricated two different configurations of a low loss 90° optical hybrid having a form factor and transverse dimension suitable for integration of a 4 diode array. They were realized on Z-cut and X-cut crystals respectively. As a result of experimental optimization of the waveguide width at specific locations and electrode parameters two 90° optical hybrids, a Z-cut one and a X-cut one were finalized, both meeting the requested specifications. Two packaged 90° optical hybrids were embedded in the test-bed.

  CeLight designed, fabricated and characterized the prototype coherent receiver version A (non integrated TIA). This coherent receiver has the requested functionality for the testbed.

  Celight continues with the fabrication and the characterization of coherent receiver version A and in parallel developed the coherent receiver version B (integrated TIA.) The coherent receiver has low optical losses, a high conversion gain, and a RF bandwidth around 8 GHz that rolls off sharply near 10 GHz. An error-free detection of 8 GSym/s optical DBPSK signal were achieved with a receiver sensitivity less than -36 dBm at 10^{-9} BER using an optical pre-amp. The integrated coherent receiver compares favourably to discrete components. The integrated coherent receiver shows much higher detection sensitivity (-25 dBm) than discrete components (-7 dBm).

- **WP 3: Balanced photoreceiver development**

  In the first project year IPAG and UDE have developed and fabricated differentially connected photodiode pairs based on InP. In the second project year UDE developed an opto-electronic integrated circuit including pin-diode pairs and a HFET based transimpedance amplifier. Simulations of two different designs (serial pin-diode connection and fully differential design) have been carried out to evaluate the optimum amplifier design. After the decision to develop a pin-TIA circuit with a serial pin-diode connection, the Layout of this design was done. First the technology of both kinds of devices was optimised separately. On the other hand the necessary technological steps for integration of both devices with strongly different topology were developed. Finally a first run of fully balanced OEICs has been produced and characterized in the time domain.

  Further the development of the transimpedance amplifier with optical input is described. UDE put great efforts in developing a optimized layer stack and improving the measurement techniques. The layer stack was improved to fit the differences between transistor

simulations and measurement results. These changes result in TIAs of higher performance and yield. A new on-wafer optical/electrical measurement setup was designed and implemented for a complete and time efficient characterization of the pin-TIAs.

- **WP 4: Signal processing component development**

  Two versions of a SiGe 5 bit analog-to-digital converter was taped out, fabricated and evaluated. Signal processing algorithms for fast hardwareefficient phase estimation and robust polarization control were simulated, programmed in VHDL and tested on an FPGA before they were implemented as CMOS ASICs. CMOS chip version A which contains a 1:16 demultiplexer and the carrier and data recovery logic was measured and evaluated. CMOS chip version B which contains full custom demultiplexers and signal processing for polarization multiplex was taped out, measured and evaluated in the testbed.

- **WP 5: Synchronous QPSK component testbed**

  Within the synQPSK project, UPb has achieved the worldwide first synchronous QPSK transmission system with real-time data recovery and standard DFB lasers in 2006. This first setup included components from the synQPSK partners as well as intermediate solutions (commercial ADCs, FPGA instead of CMOS chip for digital signal processing).The major challenge remaining after project year 2 was to combine the phase and data recovery with a digital polarization control in order to allow polarization multiplex transmission. With its FPGA-based intermediate testbed, UPb achieved the first realtime polarization-multiplexed QPSK transmission with electronic polarization control in the year 2007. All new components developed within synQPSK were integrated into the testbed on availability. Succesful combination of all these components in the same testbed was demonstrated in 2008, just at the completion of the project.

1.2 Strategic impact

The strategic impact of the synQPSK project is that the results allow for synchronous QPSK transmission with standard DFB lasers for the first time. This breakthrough will enable the widespread use of synchronous RZ-QPSK transmission with polarization division multiplex. The value of this scheme lies in avoiding the large chromatic and polarization mode dispersion penalties of 40 Gbit/s systems due to the reduced symbol rate of only 10 Gsymbols/s. Also, the RZ signal format together with PSK guarantees a superb resilience against nonlinear degradations due to cross phase modulation. The combination of QPSK and polarization division multiplex means that the cost per bit is lower than for binary PSK or for the transmission of only one polarization because the receiver complexity stays essentially unchanged.
For the new 100 Gbit/s Ethernet standard, the demonstrated feasiblity of QPSK with polarization multiplex is an important milestone and is expected to continue to play an important role in the ongoing discussion.

2 General Project objectives and state of the art

Synchronous quadrature phase shift keying (QPSK) transmission combined with return-to-zero (RZ) coding and polarization division multiplex is an extremely attractive modulation format for metropolitan area and long haul fiber communication. Compared to standard intensity modulation the line rate is 4 times lower, the needed number of photons per bit less than half as high, the tolerance to chromatic dispersion and polarization mode dispersion several times better, and the tolerance against fiber nonlinearities, in particular cross phase modulation, is excellent. Moreover, the detected electrical signals are proportional to optical fields. This transfers the advantages of photonic processing 1:1 into the electrical domain. It is (almost) correct to say that "optical signal processing is performed electronically". In particular, all linear optical distortions (polarization transformations, polarization mode dispersion, chromatic dispersion) can be equalized electronically without losses. Synchronous QPSK possesses also distinct advantages over all other modulation formats, in particular duobinary, RZ, DPSK and DQPSK and all variants thereof. These modulation formats receive a lot of interest from researchers who consider synchronous QPSK as too challenging. That is highlighted for example by Lucent's invited paper P.J. Winzer and R.J. Essiambre, "Advanced optical modulation formats", Proc. ECOC-IOOC 2003, Th2.6.1, where synchronous QPSK was not even mentioned, obviously because it seemed to be out of reach! In fact, the components required for synchronous QPSK are simply not available so far. In the traditional, phase-locked loop based receiver concept this holds especially for lasers with linewidths in the lower kHz region. However, in our concept these are not needed. Rather, the laser linewidth specifications are greatly relaxed due to a novel carrier recovery scheme. It shifts the burden from the lasers to electronic integrated circuits, which can be manufactured at a very low cost in CMOS.

3 WP 1: QPSK modulator development (Photline)

During the synQPSK project, Photline has been working on the development of a QPSK modulator, showing simultaneously low voltages , broadband and low insertion loss. The choice of technology was pushed on a new configuration of Z-cut modulator reaching all the best performances of a comparable X-cut modulator, but with lower driving voltage and a very low chirp thanks to the ferroelectric poling techniques used in the fabrication. Photline started the development of the X-cut QPSK modulator to establish the state of the art and to allow the other WP's to start system evaluation and a demonstration of DQPSK systems at 2 x 10Gbps and 1550nm wavelength. After the first version of X-cut dual Mach-Zehnder were demonstrated, the Z-cut design, fabrication and characterization was fully completed. The low chirp of the device is obtained thanks to a ferroelectric domain inversion carried out locally on the original wafer. Prototypes could be delivered to Upb. It could be demonstrated that the modulator fully comply with preliminary specifications required in the original proposition and could be used on the C&L band. It is in particular characterized by low driving voltage (<5V) and very low insertion loss (<5.5dB)

3.1 Objectives

This workpackage aims to study new types of QPSK modulators. Dual parallel Mach-Zehnder (QPSK) modulators are based on the integration in one single substrate of two parallel Mach-Zehnder modulators on which two different data streams can be applied. These two Mach-Zehnders are linked together in parallel via input and output optical Y-junctions. Thus, the global device exhibits four arms. Each sub Mach-Zehnder is equipped with both RF and DC electrodes. The data stream at 12.5Gb/s up to 28Gb/s today is applied on the RF electrodes while the DC

electrodes allow to control the phase between the two arms. Another set of DC electrodes is positioned in order to control the total phase difference between the two sub Mach-Zehnder modulators. 5 electrodes are required to drive the QPSK modulator.

Such device is generally integrated in a substrate of lithium niobate, a crystal featuring superior performances for the electro-optic characteristics. Two kinds of crystal orientations do exist. The X-cut orientation is generally used because it offers a pure amplitude modulation at the output without any associated residual phase modulation. This non-intentional phase modulation which can be introduced by a modulator is known as the “chirp“. The chirp can be a severe drawback in long haul transmission through optical fibre. Moreover, the chirp can introduce a strong crosstalk between channels when used in the QPSK format. The X-cut modulator provides a modulation without chirp.

On the other hand, X-cut modulators exhibit higher driving voltage than the other crystal orientation, i.e. the Z-cut configuration. The drawback of Z-cut modulators is that they exhibit a strong chirp parameter that makes them unsuitable for integration as QPSK modulators. The adavantege is that for an identical design of CPW electrodes, i.e. same length, same conductor width, same gap, same electrode thickness, same buffer layer thickness, in principle, Z-cut modulators have smaller driving voltage than X-cut modulator: typically, if an X-cut modulator has a half-wave voltage of 5V, the equivalent Z-cut modulator can be as low as 4 volts.

The characteristic impedance of Z-cut modulator can also be higher than X-cut modulators, which mean that the impedance matching can result in improved electro-optic bandwidth. This is due to the anisotropy of the permittivity parameters of lithium niobate in this configuration.

We proposed in this workpackage to design a QPSK modulator in Z-cut lithium niobate substrate to benefit from the low driving voltage which is mandatory for QPSK modulation. The problem of the chirp associated to Z-cut configuration will be cancelled out by a design we recently validated, based on the use of local ferroelectric domain inversion, and corresponding phase reversal RF electrodes. With such a scheme, the asymmetric design used with standard Z-cut modulators, resulting in residual chirp, is counter-balanced in order to retrieve a symmetric configuration and hence a zero-chirp behaviour.

3.2 Description and principle of operation of a QPSK modulator

A conventional QPSK modulator can be built on X-cut Lithium niobate with propagation of light along the Y-axis. The Z-axis is transverse. An input Y junction separates the light in two branches that illuminates two parallel Mach-Zehnder modulators. Each of these modulators is driven by an RF electrode on which each signals DATA1 and DATA2 are applied. Each modulator also gets DC electrodes that allow to adjust the working point on a $+\pi$ or $-\pi$ radians phase shift for QPSK modulation format.

Finally, after recombination, the two output fields propagate in straight branches where a third set of electrode can adjust the final phase shift between the response of the two Mach-Zehnder. This phase shift is $\pi/2$. Then the last output Y-junction recombines totally the 4 output fields in the output waveguide.

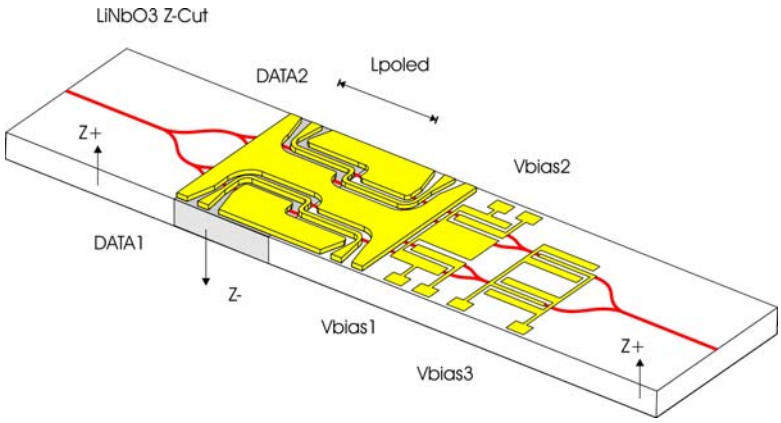


Fig. 1: Scheme of the Z-cut poled modulator for QPSK application

The modulator, which is studied in the frame of the project synQPSK, is shown in Fig. 1. It differs from the classical QPSK modulators by the crystal orientation. This modulator is integrated in a Z-cut lithium niobate substrate. The goal is to take advantage of smaller driving voltage and larger bandwidth. The configuration proposed here will also allow a low chirp or near zero-chirp behaviour, which is of critical importance for QPSK applications.

The basic design of the optical circuit does not differ strongly from the X-cut modulator. The main difference is in the arrangement of the electrode lines. Indeed, in Z-cut modulator, the origin of the chirp comes from the asymmetry between the optical/electrical overlap coefficients of the waveguide placed under the central conductor of the CPW electrode and the one placed under the lateral ground plane. The first one is submitted to a strong electric field that produces a large phase modulation via the electro-optic effect while the other waveguide arm is submitted to a weaker phase modulation. At the recombination of the two arms, due to this imbalance, only a portion of phase modulation difference contributes to the amplitude modulation, while a residual phase modulation produces the resulting chirp at the output of the modulator.

The basic idea of the new Z-cut modulator we proposed to apply to this QPSK modulator is to establish a symmetry in the arrangement of the electrodes with the optical circuit in such a way that the residual phase modulation is cancelled out at the output. This will be done without sacrifice on the whole modulator performances.

Since a QPSK modulator has to be driven with a peak-to-peak voltage equal to 2 times the half wave voltage, the latter has to be as small as possible to reduce the power consumption of the two RF drivers, which are necessary to apply both the I and the Q data sequences. Two types of crystal orientation does exist in lithium niobate technology which is the best developed in industrial applications of modulators mostly in fibre communications of long distance and high data rates.

3.3 Technological description of the device

The synQPSK modulator consists in two Mach-Zehnder Interferometers (internal MZIs) integrated inside another MZ- interferometer that drive a λ/4-path difference between them, see figure 6 in "the Poled Z-cut QPSK modulator description" section. Both the internal MZIs and the combiner are based on the electro-optic effect in lithium niobate. To benefit from the highest electro-optic coefficients all the optical/electrical interactions are based on Z-aligned fields. On Z-cut substrates this occurs for TM-polarized optical modes and vertical electric fields (underneath the electrodes). As described in the "principles of operating" sections, some areas are electrically poled so as to reverse the spontaneous polarization of the crystal in that sections.

To fulfil those requirements, the lithium niobate substrates will be Z-cut ones. Reversed sections will be made by electric-field poling. The whole guiding architecture will be realized with a proton exchange process fully compatible with the previous poling process. One of the main interests over the very good level of losses in such waveguides is that they act as polarizers: only TM- modes are supported in the waveguides. As no TE-modes are excited, no polarization scrambling can occur.

An electrical architecture is placed on top of the waveguides over a buffer layer. RF-electrodes, that can be seen as microwave coplanar waveguides (CPW) are made of thick electroplated gold on top of a silica buffer layer. LF-electrodes are made with a stack of thin dielectric and metallic layers on top of the optical waveguides. One of the challenges here is to place two MZI's inside another one without increasing the size i.e. the microwave and optical losses. At the same time, one needs to avoid any crosstalk between both internal MZIs, while keeping the performances at the same level than for stand-alone devices.

3.4 Optical Architecture

The global optical architecture is entirely made by a proton exchange process on Z-cut substrate. All the waveguides are made on the same technological step. The resulting refractive index is the same for all the waveguides (width-changes only). The optical architecture is made of single mode waveguides that compose two internal Mach-Zehnder interferometers inside a combining one. Both internal interferometers are standard like devices, while the combining has to be carefully design so as to split the incoming light into two 50% parts without instabilities.

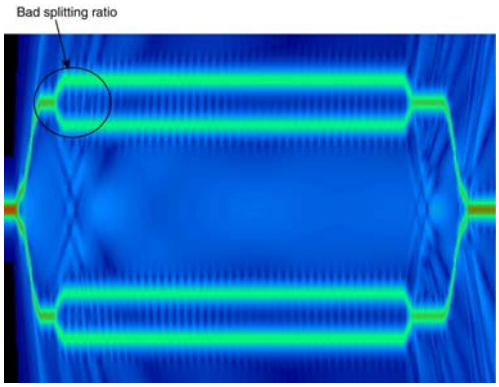


Fig. 2: BPM simulation of the mach-zehnder

The splitting ratio of the Sub-MZ seems to be a critical point that can cause degradations of the modulator performances (low contrast…). In that case, the overall optical losses are estimated to be in the range [–4.5;–5] dB. These losses result from a combination of fiber-to-waveguide mismatch, propagation and radiative losses.

3.5 Technological flow chart

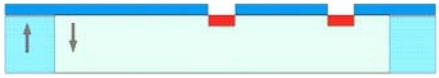
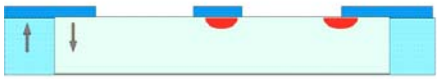
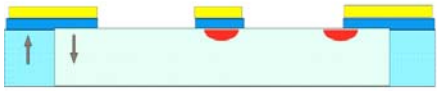
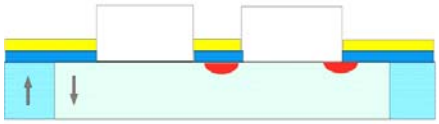
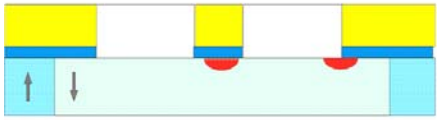
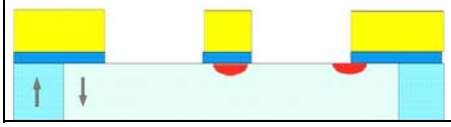
	Substrate Lithium niobate Z-cut
	Poling of the crystal to get a localised ferro-electric domain inversion
	Elimination of the poling mask
	Photolithography and Deposition of the protecting layer before proton exchange process
	Proton exchange and waveguide fabrication
	Elimination of the Protecting layer
	Post annealing of the PE waveguide
	Silica buffer layer deposition
	Silica buffer lithography and etching
	Electrode lithography and deposition process
	Thick photoresist coating and photolithography
	Electro-plating of thick layer of gold on electrodes
	Elimination of the photoresist mould

Fig. 3: Representation of the flow chart for fabrication of the Z-poled QPSK modulator

3.6 Package design

We saw before the operating of such a DPSK-modulator and the impact on the design of the chip. According to the previous considerations a high performance package is required to bring out the performances of the chip. The general design (materials, connectors, dilatation considerations…) of the package is based on the ones of the standard commercial products at Photline. This approach allows making a custom designed package with the insurance of a good behaviour in respect of the user and environmental (such as temperature variations) requirements. The QPSK- Modulator package will exhibit:

- Double RF- inputs with K-connectors
- Triple DC- inputs (pins)
- Two monitoring photodiodes outputs (pins)
- Single mode optical fibers at both the optical input and output. Maintain polarization fibers can be use if required and optical connectors will be chosen in respect with the overall project standards.

The following image is a view of the package footprint, showing the dimensions, the position of the input-outputs, and the screw holes for implementation on an emitter board.

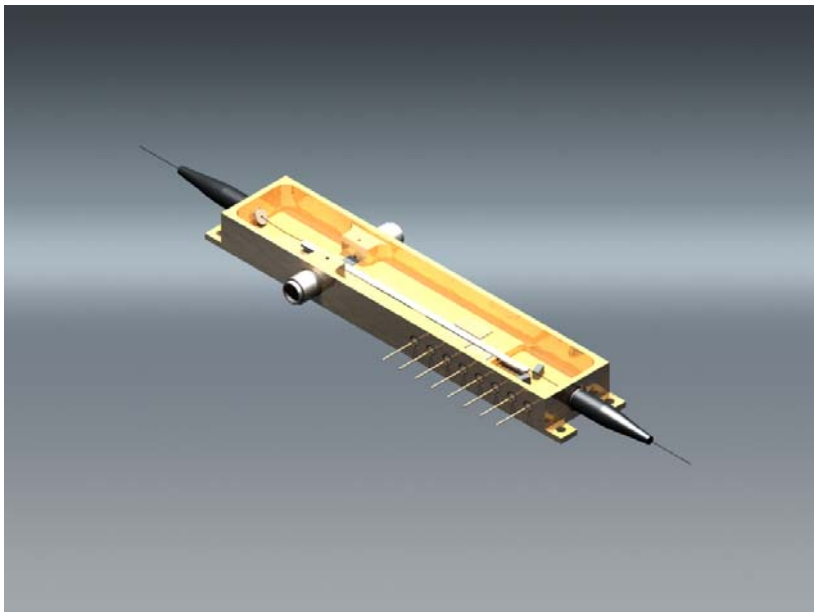


Fig. 4: Packaging virtual representation

3.7 Z-cut quasi zero-chirp QPSK modulator fabrication

From all the previous information accumulated thanks to X-cut version, a complete fabrication was launched on a Z-cut lithium niobate crystal. The waveguide fabrication involves two layout level: one to implement alignment crosses, and the other one to define the protecting mask at the surface of the crystal and which is removed after the waveguide process. Thus, the first technological step was to apply a local ferroelectric domain inversion. This was done by defining the area of the crystal having to be inverted, thanks to a thin layer of photo resist and a lithographic step. A dedicated set-up was used to apply a high voltage of specific shape during a brief time throughout the thickness of the crystal (typ 500µm). As the correct parameters are adjusted then a small current is delivered indicating that the ferroelectric inversion operated conveniently. This is achieved at room temperature. The rest of the operation consists in the

proton exchange waveguide fabrication by use of the proton exchange process as mentioned earlier. All the other operations are described and summarized in the previous paragraph.

3.8 Wavelength behaviour on the C & L band and 10 Gbit/s transmission

The transmission loss of the modulator was checked from 1500nm to 1600 nm. The insertion loss remains within 2dB. The half wave voltage was checked on the same spectral range. The variations on the half wave voltage did not exceed the excursion due to the proportionality of $V\pi$ with wavelength. Finally the modulator was inserted in a complete set-up of DQPSK modulation at 2x10Gb/s. The QPSK eye diagram was recorded at 1525nm, 1535 nm, 1542, 1550nm, 1560nm, 1565nm and 1606 nm without noticeable modification in the quality of the signal. No corrections was necessary to be introduced in the voltage control between each wavelength modifications.

The quality of transmission was characterised at 10Gb/s on each channel I & Q separately by OOK modulation format. This allowed to control the quality of the eye diagram and the distortion of the eye diagram after propagation in a single mode transmission fibre. This is an other way to assess the influence of any residual chirp. Each nested Mach-Zehnder was individually tested at 10GB:s NRZ PRBS signal to check the quality of the transmission in a tunable dispersion module, again to verify that any contribution of the chirp has an influence on the modulation. For that, one of the Mach-Zehnder is set at extinction while the other one is set at quadrature and submitted to the data stream signal.. We checked the results for both slopes of the modulation transfer function.These experiments were carried out with Z-cut component confirming that the chirp properties issued from both technologies were very comparable and close to zero.

Version B of the Z-cut modulator fullfills all the target specifications originally defined:

- 14..16 GHz Bandwith
- 8..10 V Driving voltage
- 5..7 dB Insertion loss
- >25 dB Extinction ratio
- >30 dB Polarization extinction ratio
- <0.1 Chirp magnitude

4 WP 2: 90° hybrid and front-end development (Celight Israel)

4.1 Objectives

The strategic objective of Work Package 2 is to realize and test the receiver of a synchronous optical RZ-QPSK communication system. There are two phases in the route to accomplish the objective: a) The 90° optical hybrid development, b) the integration of the balanced receiver to be developed in WP3 and the above 90° optical hybrid into the synchronous QPSK receiver.

The detailed objectives are:

- To design two different configurations, to be realized on Z-cut and X-cut crystals respectively, for a low loss 90° optical hybrid having a form factor and transverse dimension suitable for integration of a 4 diode array. The design should allow for experimental optimization of the waveguide width at specific locations, and electrode parameters. The optimization dealt with the reduction of the distance between the output ports, minimizing the expensive diode footprint, while enhancing its matching properties, which are essential for differential operation;. The goal was the reduction of optical insertion losses, and the reach for a smaller package footprint.
- To fabricate hybrid prototypes of the above configurations (Milestone M2-1 and M2-2)
- To optimized the unpackaged X- and Z-cut 90° hybrids prototypes for initial characterization and reach the pre-defined basic functionality (Deliverable D5)
- To design synchronous 10 Gbit/s QPSK receiver front end with PIN diode array (Milestone M2-3) and to assemble the unpackaged synchronous 10 Gbit/s QPSK receiver front end with PIN diode array (Milestone M2-4.)
- To finalize the packaging of the Receiver front end on submount (Milestone M2-5.)
- To characterize the Integrated Receiver front end and have an acceptance test for the version A (Deliverable D15.)
- To fabricate coherent receivers for the test bed
- To design and fabricate the integrated receiver front end version B

All the above objectives (except the fabrication of the integrated receiver front end version B) were achieved.

4.2 Design of the 90° optical hybrid

In general, the design goals for the 90° optical hybrid work in concert with each other.

The contributors to the insertion losses (excluding coupling losses) are the straight waveguide intrinsic losses that are scaled with the length, and the waveguide bending losses. The main factor defining the longitudinal dimension is the distance between the output ports, which also affects the curvature of the -s-bends. By decreasing the distance between the output ports and using our design rules, the length of the 90° optical hybrid can be significantly decreased, resulting in lower total insertion loss and a smaller footprint.

The 90° optical hybrid contains four 3dB-couplers, a number of S-bends, and a crossing waveguide structure (Fig. 4).

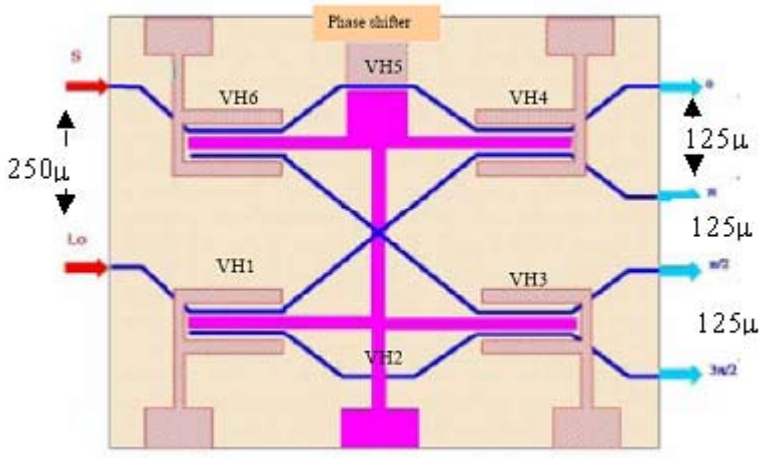


Fig. 4: 90° optical hybrid schematic

The S-bends are designed to connect the two input ports with 250µm spacing with the four output ports with 125µm spacing. The input spacing is dictated by the fiber array (commercial) used for pigtailing the receiver. Another limitation is a requirement to provide enough space for 3-dB couplers such that they can be operated within a reasonable bias voltage range. The crossing voltage is almost linear with the effective coupling length; therefore higher crossing voltages are excepted when compared to hybrids with larger footprints.

The 3-dB coupler design is based on our experience with the X-cut 250µm output spacing hybrids. A typical 3-dB coupler is presented in Fig. 5. The upper figure shows the waveguides and the electrodes layout. The lower figure shows the electrostatic field distribution in the X-cut plane geometry.

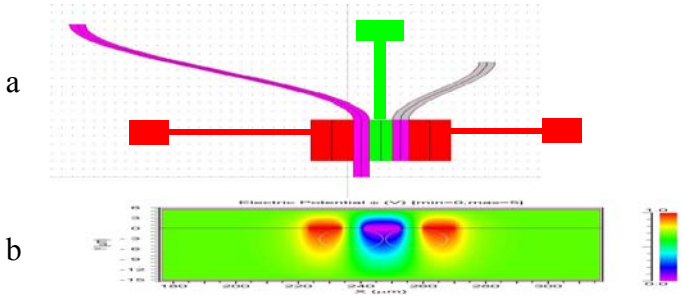


Fig. 5: a) the waveguides and the electrodes layout. The pink waveguide is the input (left). The red electrodes are for DC bias. The green electrode (middle) is the ground. b) The electrostatic field distribution in the coupler cross section.

For both geometries different fabrication parameters were tested. In order to calibrate the model parameters and the fabrication parameters for the Z-cut plane, we fabricated the basic structure (straight, S and X waveguides) using an existing mask.

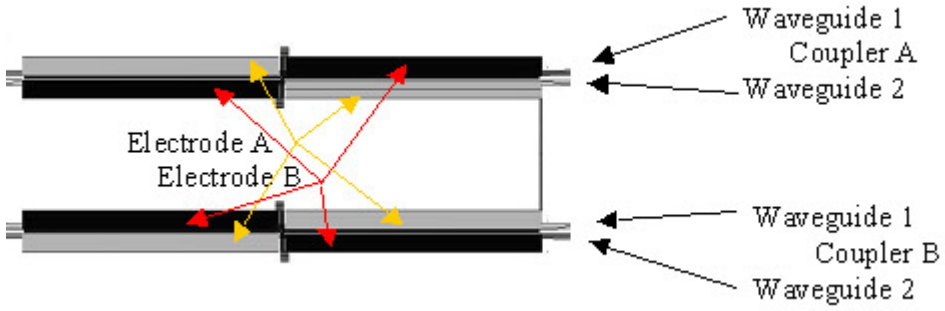


Fig. 6: Z-cut hybrid electrode's geometry

4.2.1 Wafer characterization

The processed wafers were characterized using our alignment machine. The schematics of the devices are given in Fig. 7. Fiber pigtails have to be connected on both sides of the device, and variable DC voltage sources have to be connected to the VH pads of the device.

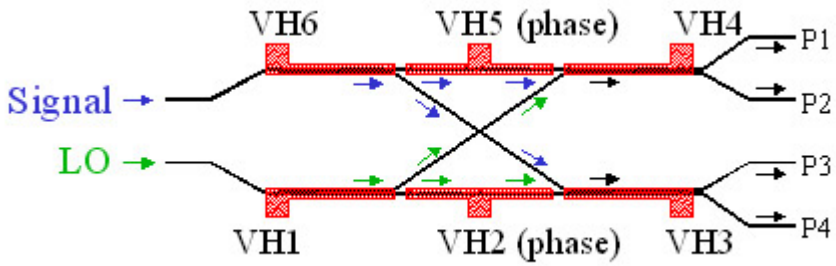


Fig. 7: Connection scheme of the 90° optical hybrid

The pigtailing is performed with a robotic alignment machine (Fig. 8). The 90° optical hybrid is placed on the middle static stage and two fiber arrays are placed on the two sides 6 axes stages. While a commercial 250µm V groove can be used at the input side, a special transition stage is pigtailed at the output side.

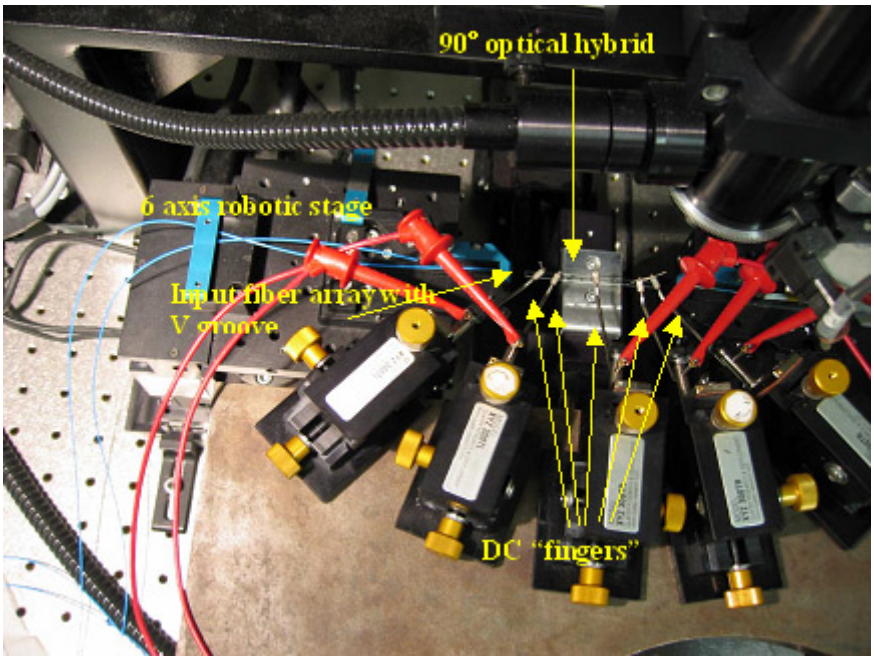


Fig. 8: 90° optical hybrid on the alignment machine

4.2.2 Unpackaged synchronous 10 Gbit/s QPSK receiver front end with PIN diode

During October 2005, months ahead the due date, the first 90º optical hybrid was mounted on a submount that included a PIN diode array, processed by IPAG, and commercial TIAs.

This device enables us to validate the method used for positioning the LiNbO3 die and the detectors. The assembling procedure enables alignment of the Lithium-Niobate device, already connected to the Fiber Array by V-groove, to the Photodiode Array mounted on the Components Block. The Components Block is fixed on Optical Bench.

The diode submount is used to place the photo-diode array in front of the 90º optical hybrid's waveguide output and to place the TIAs close to both the photo-diodes and the external output RF connectors. To fulfill these placement requirements, the photo-diode array is positioned on the face of the diode submount that faces the 90º optical hybrid; while the TIAs are positioned closed to the photo-diode array, but on the top of the diode submount, which faces the cover of the packaging, Fig. 9.

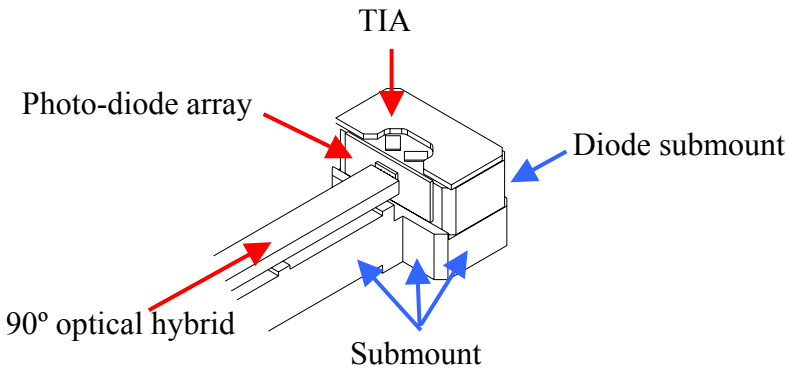


Fig. 9: The Component Block with the mounted photodiode array and the TIA is bonded to the Submount that carries the 90º optical hybrid.

Two interface PCBs are used (Fig. 10): the TIA interface board that is used to interface with the 'external world', and the Diode Transition piece. On the package itself, there is an additional PCB that interfaces with the package pins.

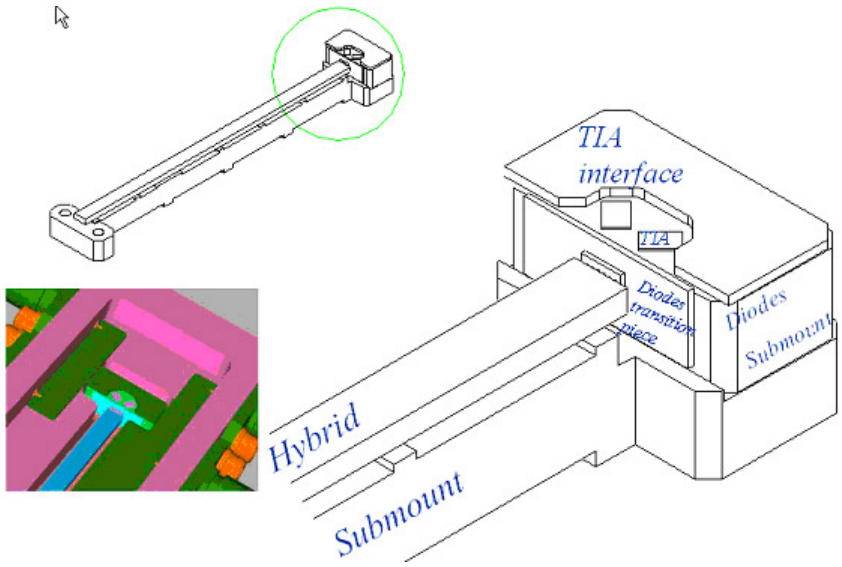


Fig. 10: The TIA interface, the Diode transition, and their placement in the package (bottom-left)

The diode transition piece accommodates the diode array, capacitors, connecting pads for ground and bias voltages, pads for the wire-bonding to the TIAs, and sets of resistors. The electrical pads on the side of the PCB panel enable access to the resistors for fine tuning of the packaged device.

The TIA Interface (Fig. 11) interfaces between the TIA outputs and the input bias/output transition piece.

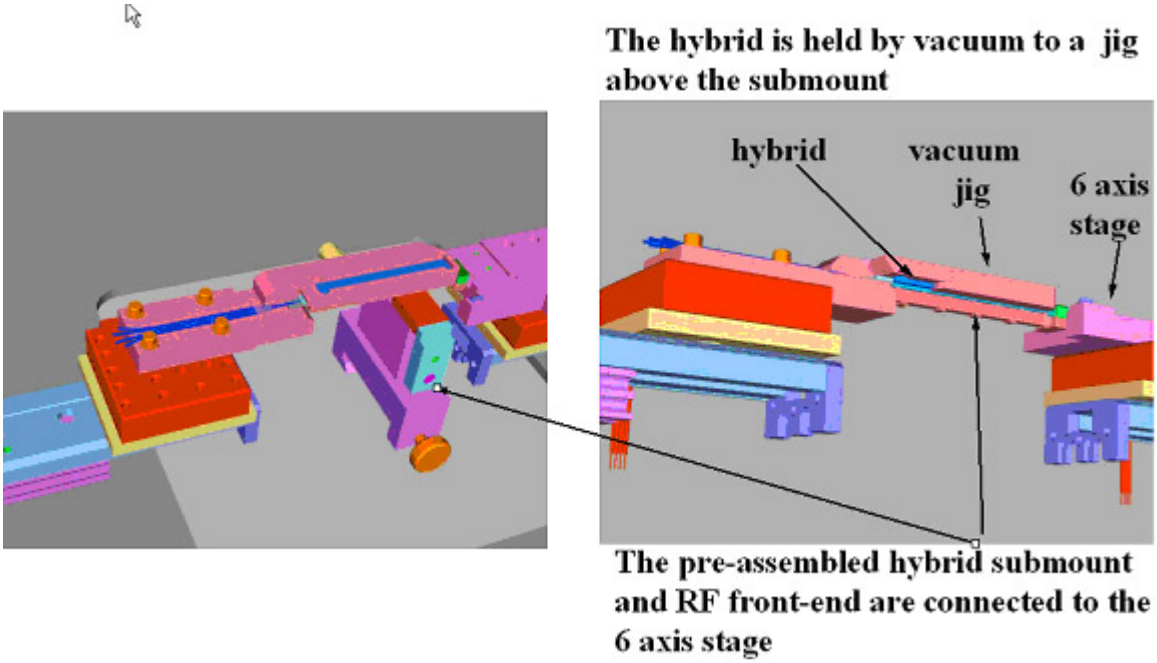


Fig. 11: Two angle computer simulation views of the final assembly process

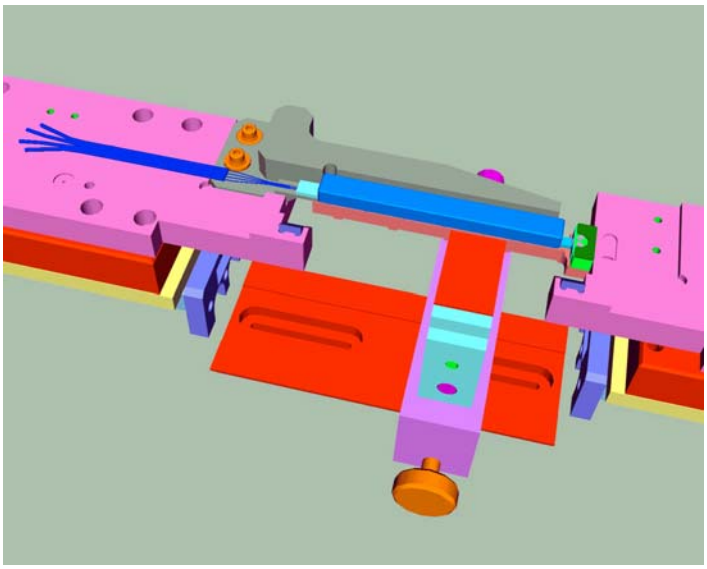


Fig. 12: A pigtailed 90º optical hybrid aligned with the photodiode array on the alignment machine

4.2.3 Integrated receiver front end version A

The package of the device should secure the device while interfacing with the external electronic circuit. The package with 12 DC input pins, and 4 RF SMA output ports is shown in Fig. 13.

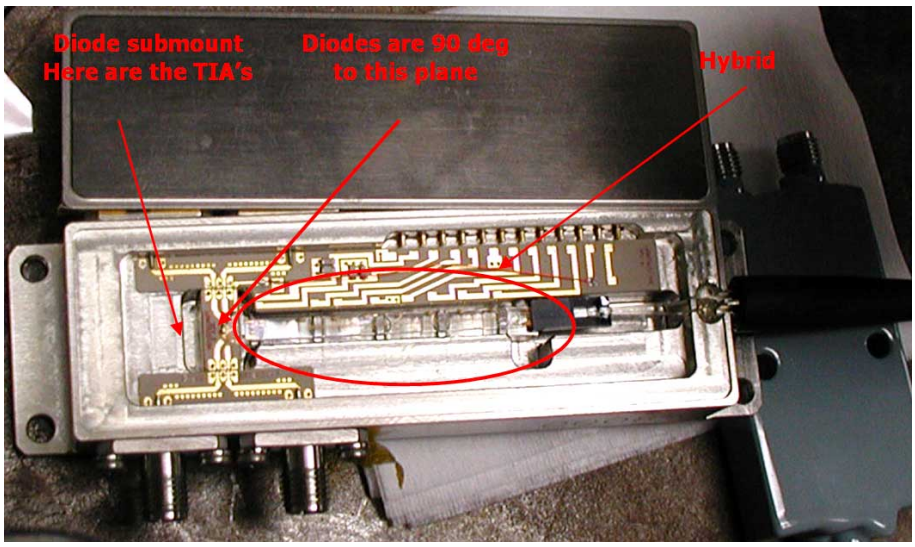


Fig. 13: The assembled device in the package.

A bias and RF interface PCB is used to connect the assembled device with the package inputs and outputs. The interface PCBs are seen in Fig. 13. The package device with and without it lid is shown in Fig. 14. Its main elements are marked.

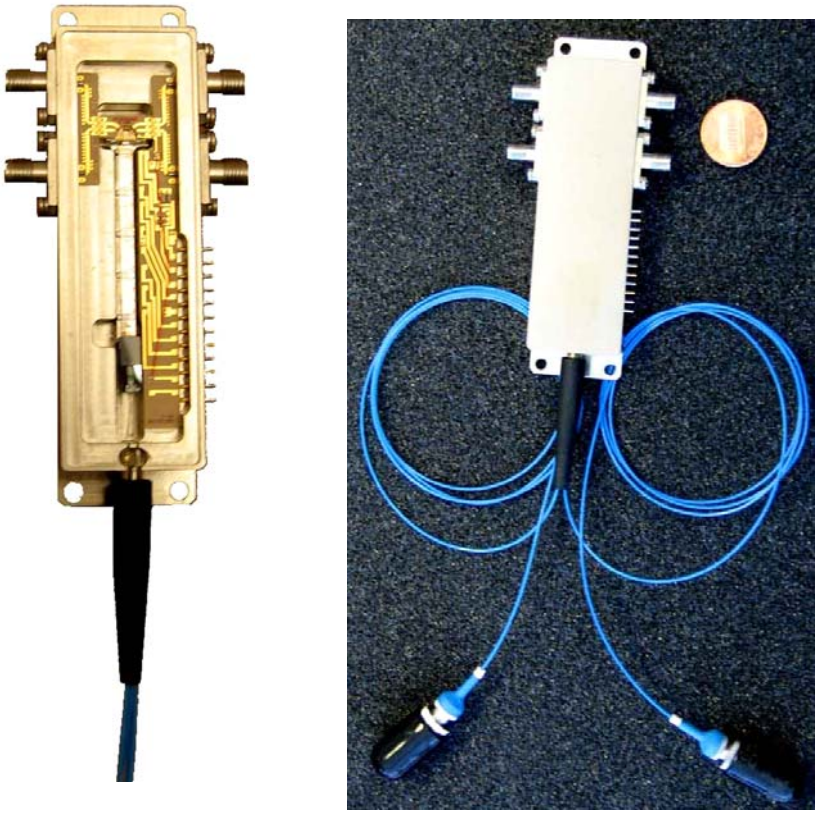


Fig. 14: The packaged receiver, open (left) and closed (right).

4.3 Detection of optical PSK signal

The coherent receiver was used to detect optical PSK signals of different formats and symbol rates for system performance evaluation. Error-free (BER < 10^{-9}) detection of a 8-GSym/s differential binary PSK (DBPSK) signal using the integrated coherent receiver with optical pre-amp and filtering at the receiver employing differential detection was achieved as can be seen in Fig. 15. The 8-GSym/s DBPSK signal was produced by a Mach-Zehnder modulator (MZM) biased at null and driven by a 8 Gb/s non-return-to-zero (NRZ) pseudo-random binary sequence (PRBS) with a word length of 215-1.

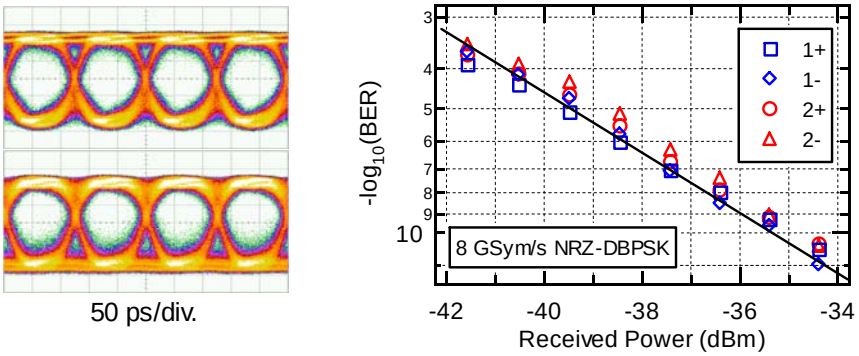


Fig. 15: Left: eye waveforms of detected 8 GSym/s NRZ-DBPSK signal from 1+ port of integrated coherent receiver. Vertical scale: 100 mV/div. Right: Measured BER of the four RF ports of the integrated coherent receiver versus received power.

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4.3.1.1 Test set up for the 10 GS/s QPSK photoreceiver front end with integrated TIA

The Balanced Photoreceiver is comprised of six PIN photodiodes and two transimpedance amplifiers (TIAs), in Fig. 16. As with the PIN photodiode arrays, the photodiodes are arranged as two balanced diode pairs and two single diodes used to facilitate alignment during packaging. Functionally the photoreceiver chip can be divided into two sections comprised of a balanced photodiode pair and a TIA. Each section has its own DC connections, note the top and bottom of the images in Figure 30, and high frequency signal output from the TIAs. The output from the TIAs is a differential signal and the pads are in a ground-signal-signal-ground (GSSG) configuration. To characterize the device, a plurality of DC and RF probes, as well as four dense packed PM optical fibers should reach the appropriate location on the device.

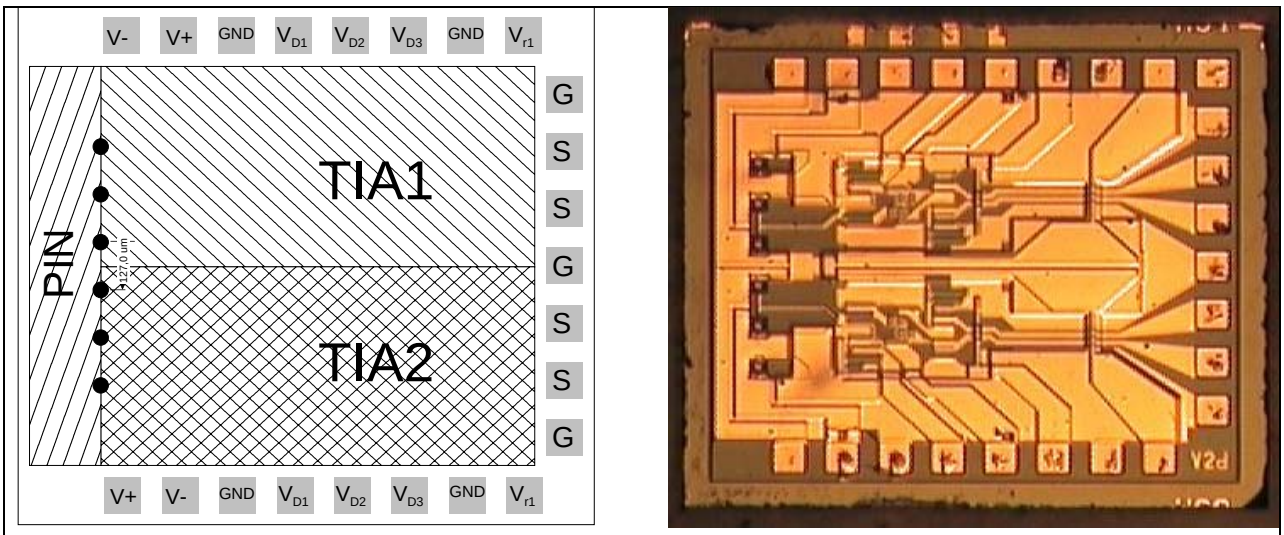


Fig. 16: Balanced Photoreceiver. Layout and picture of chip.

The four diodes that comprise the photodiode pairs were tested for DC responsivity and optical-to-electrical (O/E) response up to 20 GHz. The two alignment photodiodes were only tested for DC responsivity.

Fig. 17 shows the test configuration for the O/E characterization of the Balanced Photoreceiver. Only one functional section of the photoreceiver was probed and tested at a time. During the tests both of the photodiodes in the balanced pair of the section that underwent testing were illuminated; an Agilent 8703A Lightwave Component Analyzer (LCA) provided a modulated optical input signal, frequency swept from 0.13 to 20 GHz, for exciting the diode under test and a CW diode laser was used to illuminate the photodiode not under tested in order to keep the DC currents on the chip balanced. The LCA also measured the RF output of the photoreceiver.

Source/meters were used to provide the bias voltages and to monitor the currents for the photodiodes, and DC power supplies were used to provide the TIA supply voltages. A bias tee in the RF line was used to connect the RF and DC grounds.

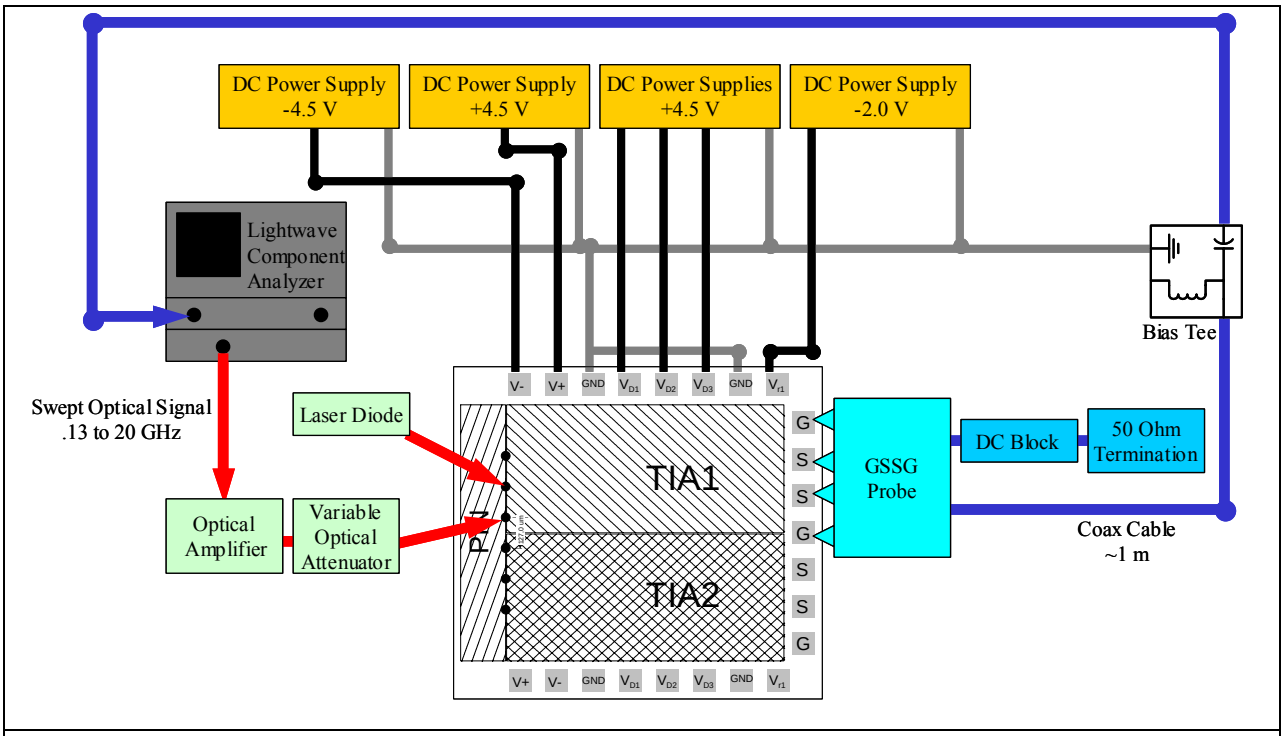


Fig. 17: Test Setup for Optical to Electrical Characterization of the Balanced Photoreceiver.

The DC connections to the chip were made using the custom multi-contact DC probe shown in Fig. 18. The capacitors detailed in the figure provide an RF bypass to ground, keeping the RF path to ground short.

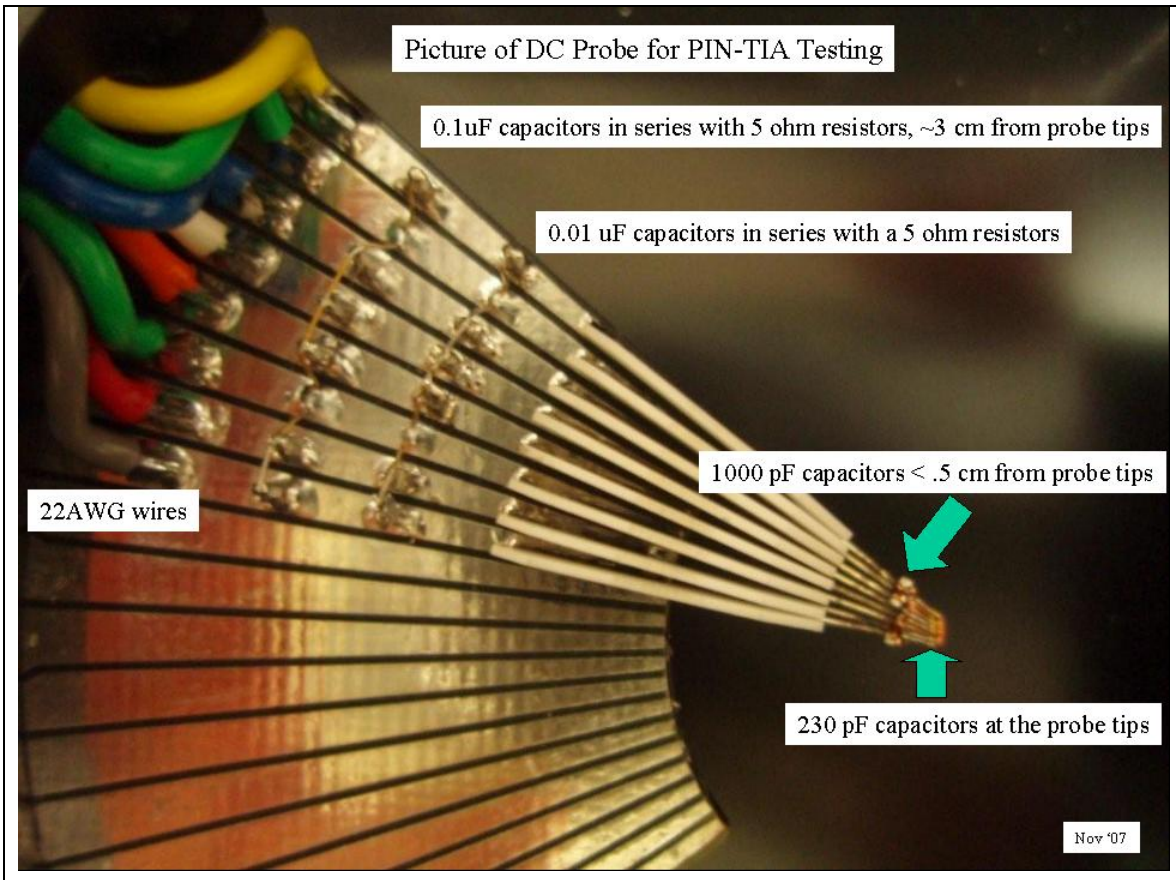


Fig. 18: Probe for Making DC Connections to the Balanced Photoreceiver.

A microwave GSSG probe was used to connect to the output of the TIA of the photoreceiver under test. The signal from only one of the differential outputs could be measured at a time; the other output signal was terminated using a DC block and a 50 Ohm load.

The first batch of the non-integrated 127µm photodiode arrays arrived before the end of the project. The arrays of this batch exhibited a new phenomenon: a capacitor on one side of the diode pair blew out when the RF probe was used to supply the ground. UDE argued that this was the first batch with a new photoresist and that some fabrication issues may still have existed. In a new batch that arrived too late to be packaged, better uniformity was observed and almost no issues with the capacitors were seen. The majority of the bandwidths were within the specifications, similar to the good 125µm diode arrays (Table 7 of D-19 report).

4.4 Coherent Receiver for the testbed

Nine coherent receivers were built. Seven where built when the first batch of non-integrated photodiode arrays arrived. Out of those seven, only two survived the packaging process; 3 suffered from mechanical damage and with the other 2 some of the photodiodes malfunctioned; it is not clear if this was a result of the packaging process or the diode fabrication process.

The two working devices were tested. CIL kept one of the coherent receivers, S/N 0009, and the second was sent to the test bed, S/N 0003. The characterization by UP revealed that one balanced detector contained a short. We decided to wait for photodiode arrays with higher bandwidths prior to building more coherent receivers.

In the meantime CIL was asked by UP to reduce the optical back reflection from the devices by pig tailing an optical hybrid with angle polished faces. CIL developed the polishing process.

Packaging of more coherent receivers was differed in anticipation of the integrated balanced receiver chips. When we realized that none of the integrated devices met the specifications, we decided to package three working non-integrated devices using the fully functioning photodiodes from the batch that had the capacitor problems.

4.5 Work Packet Objectives and Success

The strategic objectives as defined for WP2 and WP3 are to realize and test the following dedicated key components necessary for synchronous optical RZ-QPSK transmission with polarization division multiplex using standard DFB lasers:

- Optical 90° hybrids in $LiNbO_3$ and receiver front end
  - ≤ 4 dB insertion loss
  - < 1 %, < 0.01 rad power and phase mismatch after biasing
  - Co-packaging of 90° hybrids and balanced photoreceivers
  - $LiNbO_3$ substrate
- Balanced photoreceivers
  - 9.5...12.5 GHz bandwidth
  - ≥0.85 A/W responsivity
  - 9 pA/√Hz input noise current density
  - InP substrate

The achievements meet the strategic objectives. However, the yield and the repeatability are very low. Even the best receiver we have, which has 8.5±1 GHz bandwidth, does not have a smooth response curve.

5 WP 3 : Balanced photoreceiver development (UDE)

5.1 Objectives

The task of IPAG and University of Duisburg-Essen (UDE) within WP3 was to design and fabricate various balanced pin-diode arrays and integrated pin-TIAs using InP technology. Based on the given specifications, IPAG and UDE developed and fabricated as a preliminary step differentially connected photodiode pairs shown in Fig. 19, the photodiodes being connected in series. All arrays will aim at 2 balanced front ends (4 photodiodes) but can be readily extended to 4 balanced front ends for polarization diversity.

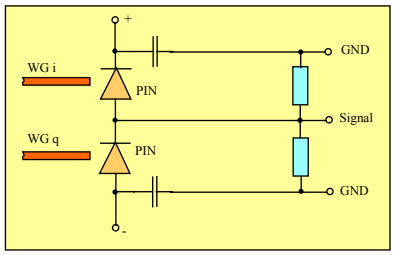


Fig. 19: Schematic of the building block for the differentially connected pin-diode pair

5.2 Progress towards objectives

The balanced photoreceiver consists of 6 pin photodiodes: two balanced photodiode pairs and two monitoring diodes for the adjustment during assembly. Each pair of balanced photodiodes has an own power supply, the monitoring diodes are connected to one of the power supplies of balanced pair of photodiodes and ground. The monitoring diodes are only used for assembly.

First two main types of arrays had to be fabricated in order to fulfil all system requirements: one with 125 µm distance between the pin-diodes and the other with 250 µm distance with different lengths of the rf-taper. Finally pin-diodes with 127 µm distance were designed to be compatible with the 90° hybrid.

A photograph of a fabricated pin-diode pair is shown in Fig. 2:

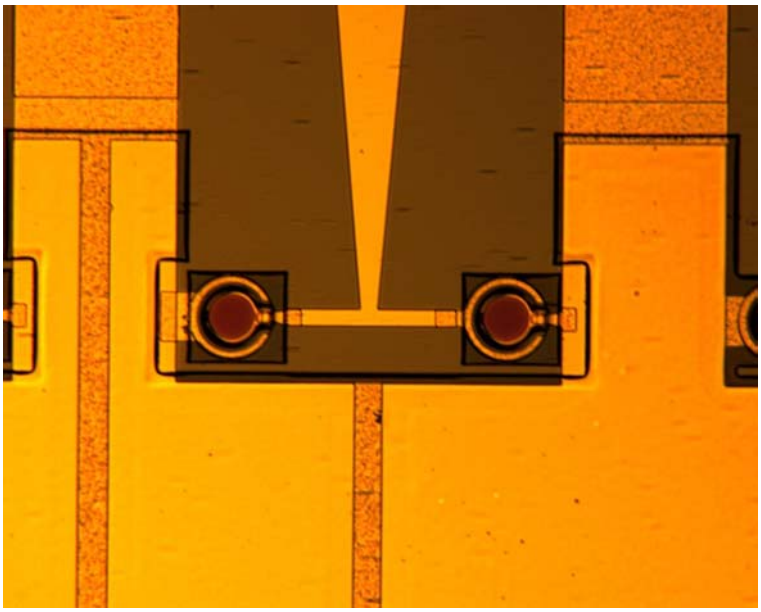


Fig. 20: Fabricated photodiode pair. The active diameter of the diode is 21µm.

Based on the technology used for the fabrication of the pin-diode pairs, IPAG had proposed and developed a technological approach for the realization of the balanced photoreceivers. The design studies included a study of a pin-HBT approach, instead of pin-HEMT, employing part of the layer structure for both, the pin-diodes and HBT. It turned out, that in this case the compromise necessary with respect to the layer thickness and doping results in insufficient pin-diode and HBT performance for responsivity and corner frequence. Therefore a combination of HEMT and pin-diode-technology is a better choice with respect to producibility and also the noise properties as well as the linearity of the device would be appropriate for the system application.

The cross section of such a device is given in Fig. 21:

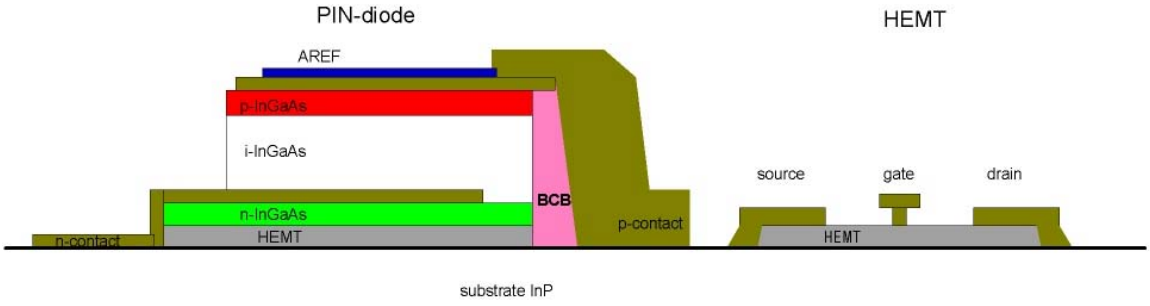


Fig. 21: Cross section of the proposed integration of pin-diode and HEMT for the balanced potoreceiver.

After the withdrawal of IPAG in June 2005 UDE took over their part and continued to fabricate and characterize the pin-diode arrays.

A main task of UDE is to develop a transimpedance amplifier which is able to convert the pin-diode current to a differential voltage output. Two different designs had to be designed and compared by simulation.

The circuit shown in Fig. 22 (left) is a balanced photoreceiver with serial photodiode connection. The other circuit is a balanced photoreceiver with fully differential design. Both have differential outputs.

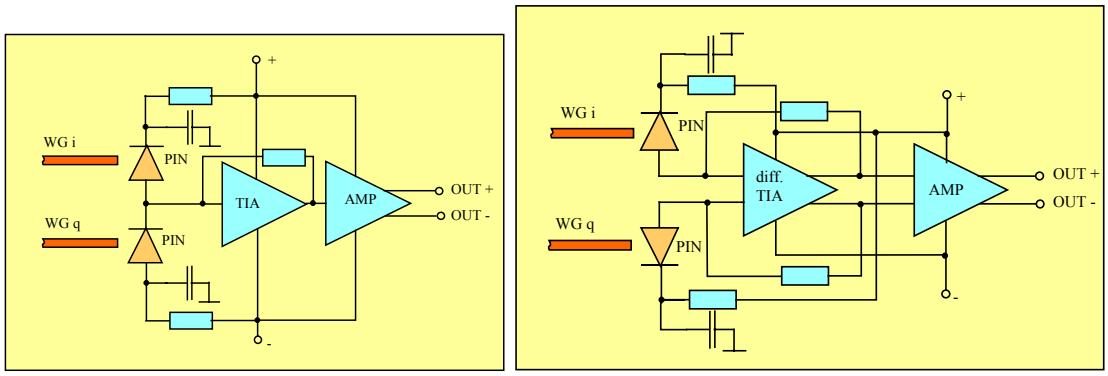


Fig. 22: pin-TIA designs for single ended pin-array (left) and for differential connected pin-TIA (right)

5.3 Modelling, Simulation and Layout

For preparation of an appropriate design and layout the two TIA circuits were simulated. The simulations are based on measurement results on fabricated transistors.. The maximum of the transconductance is 37 mS at a gate source voltage of 0 V. This is important for the bias point of the transistors inside the TIA circuit.

With the modelled transistors the two TIA circuits were designed and compared In the first circuit the two pin-diodes are connected directly to the TIA. At high absolute optical input levels this results in a high dc-current into the TIA. This affects the bias points of the transistors inside the TIA. Both circuits show nearly the same transimpedance and cut-off-frequency. The advantages of the circuit with a balanced pin-diode-array are as follows: Only the rf-signal is fed to the circuit, there is no susceptibility to dc-photo current variation, and the complexity is lower. Therefore, the circuit with a balanced pin-diode-array is preferred.

The selected TIA circuit with a balanced pin-diode array has a low complexity and contains three different stages. The first stage is a cascode employing a dual gate HFET which provides the gain. The second transistor gate of the cascode is short circuited to ground for the rf-signals. The second stage is to convert the impedance and to feed back the output to the input via R_f, forming the typical TIA-configuration. The last stage is a differential amplifier which provides the match to 50 Ω.

All stages use active transistor loads yielding current source function and compact high rf-resistances. Based on the simulations described further specific designs are investigated. Three different HFET layouts are employed, i.e. HFET with a 1-finger, a 2-finger and a dual gate configuration, with the advantage of reduced impedance between the two gates in case of the dual gate version.

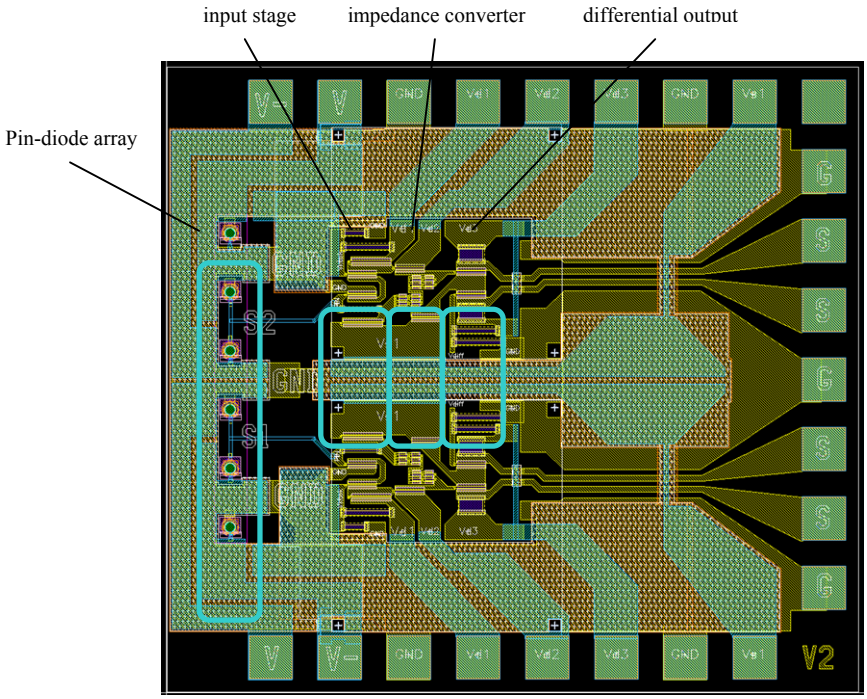


Fig. 23: Example for a fabricated layout, circuit with pin-diodes und 1-finger gates

Each circuit includes the same kind of output. A configuration of ground, signal, signal, ground is normally used for a differential output. The characteristic impedance of the signal output is 50 Ω.

5.4 Technology and Measurement

The layer structure for the pin-TIA has been grown using MOVPE on s.i. InP. The thickness of the absorbing InGaAs layer has been chosen to 1900 nm. In Fig. 24 the integration concept is shown.

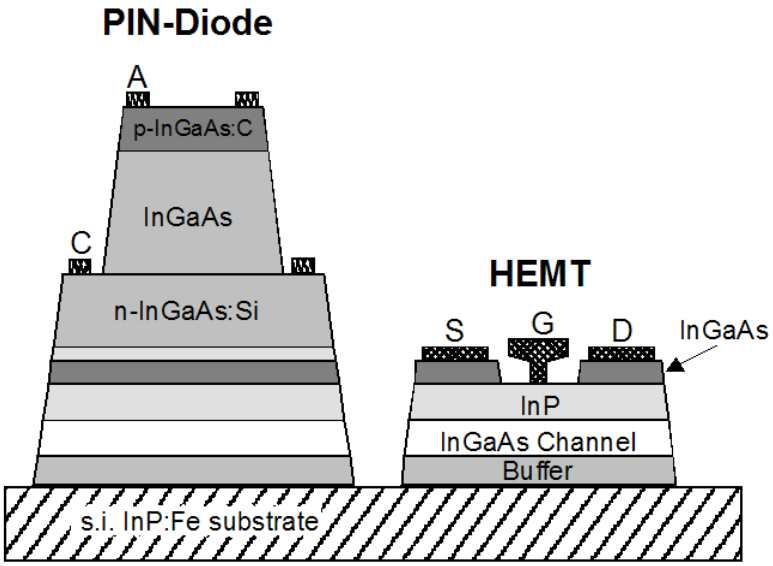


Fig. 24: integration concept for pin-diode and HFET

One of the main technological challenges is the high topology of the pin-diodes. A height of nearly 3 µm results in difficulties to protect the pin-diodes during the gate-process, which, on the other hand, needs a thin resist for defining the sub-µm-gate.

Our approach is to protect the pin-diodes with a thick resist followed by a thin e-beam resist for the gate process. Fig. 25 shows an SEM-image of a 2 µm high test mesa.

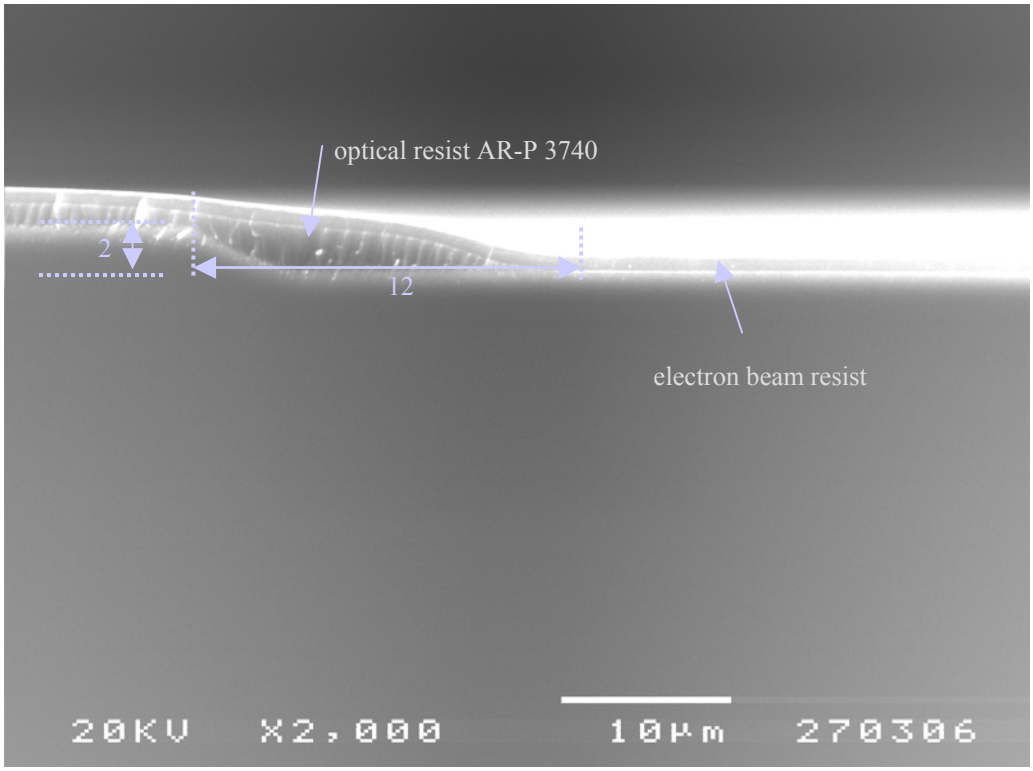


Fig. 25: SEM image of photo resist on 2 µm mesa structure

At a distance of only 12 µm from the pin mesa edge, the e-beam resist regains its typical properties like on flat surfaces. The distance between pin-diodes and TIA in the developed circuit is larger than 40 µm, so this process is applicable also for 3 µm topologies.

Another problem is an annealing step at 300 °C for curing the BCB, which is used for the capacitor dielectric and for passivation. During the mask design for the synQPSK-Project the effects of the annealing procedure on the specifications of the transistor were unknown.

Tests revealed a shift in threshold voltage of about 0.2 V (see fig. 16 and fig. 17).

Fig. 26 shows a picture of the fabricated pin-TIA circuit including the pin-diodes and 1-finger transistors.

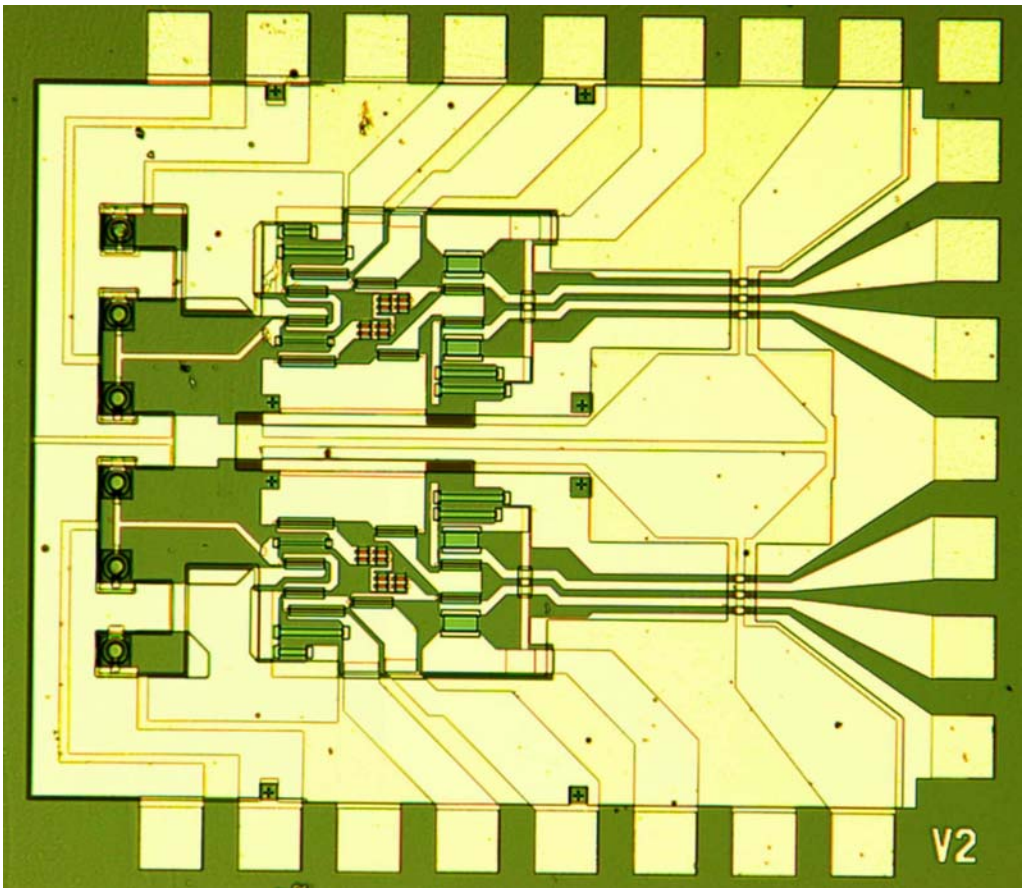


Fig. 26: Picture of the pin-TIA

For a first and simple test already including rf properties, the pure electronic circuits were measured in the time domain (see Fig. 27).

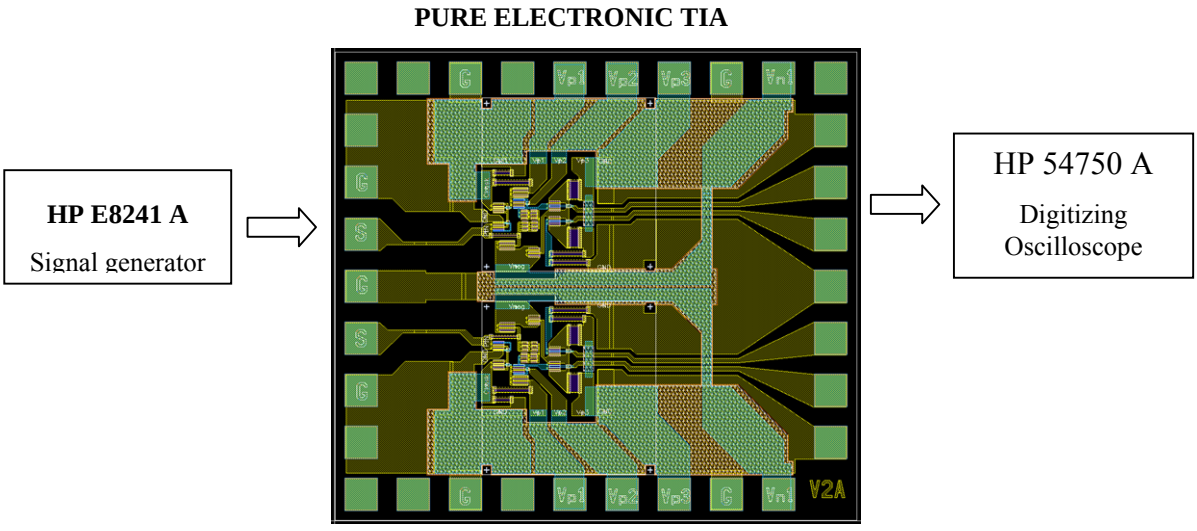


Fig. 27: Setup for time domain measurement

Signal pulses with 1 dBm input power are applied to the input and the differential output signal is displayed for 1 GHz. First, a reduction of the output voltage at 10 GHz is observed, compared to 1 GHz operation. This is mainly due to the higher R_f, which reduces the bandwidth. Secondly, an asymmetry is obvious especially at 10 GHz, which is contributed to the shift of the threshold voltage and the transconductance maximum.

5.5 Balanced receiver OEIC B and Layer Stack Redesign

As described, two main challenges appeared during the first characterizations of the pin-TIA. The sheet resistance of the layer used for the resistors was unexpectedly high. Additionally, due to an annealing step which is introduced for circuit fabrication we got a threshold voltage shift of the heterostructure field effect transistors. Because of these two challenges the first pin-TIAs have shown functionality but ended in a lower bandwidth and lower gain than expected from simulations. Because of this a redesign of the layer structure was done instead of new tape out.

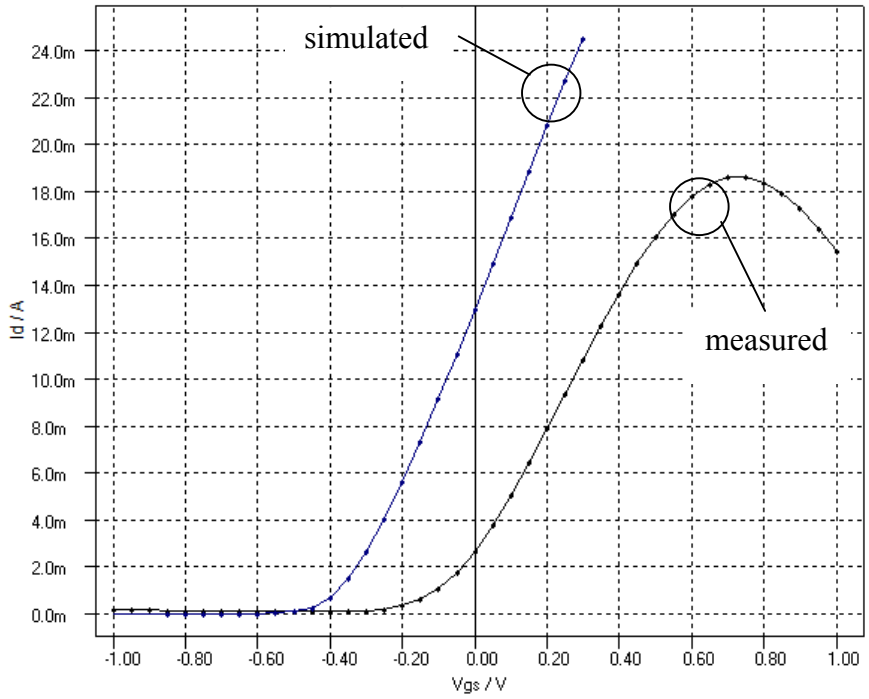


Fig. 28: transfer characteristic (U_{DS}=1V) of the transistor used for simulation and the measured transistors on the pin-TIA sample

These two problems were solved by changes in the layer stack. The thickness of the InGaAs contact layer was increased by 10 nm from 20 nm to 30 nm to decrease the sheet resistance and the InP-barrier layer was increased by 5 nm up to 12 nm to cancel the threshold voltage shift curing the BCB.

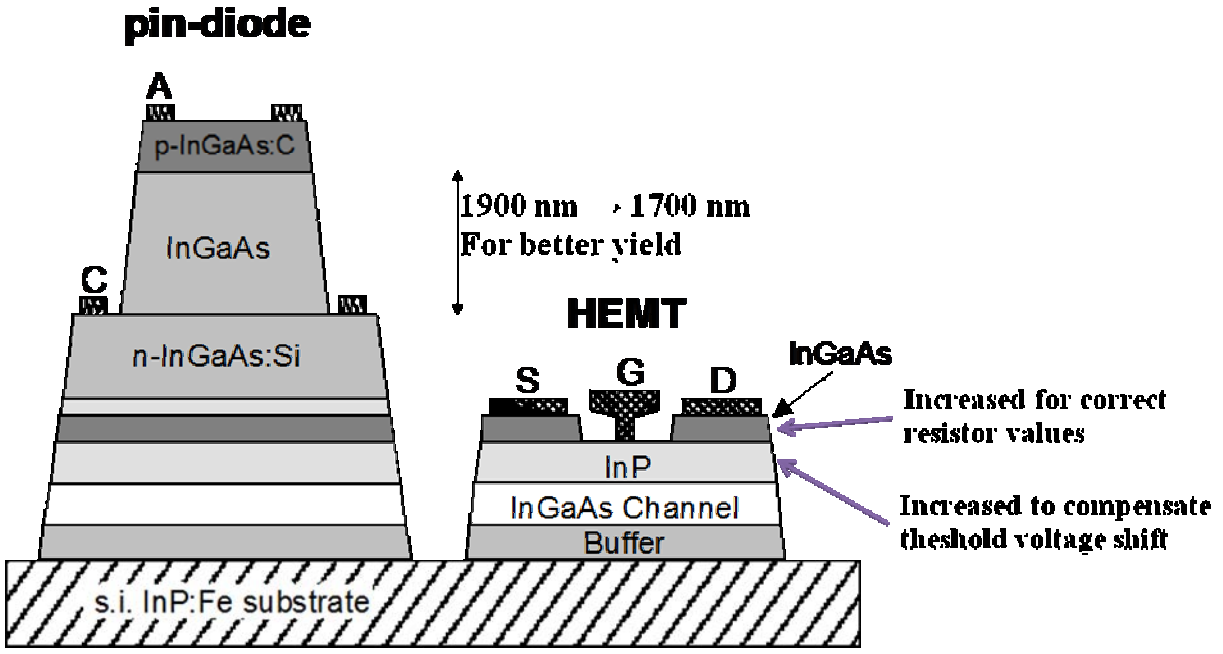


Fig. 29: changed layer stack of pin-TIA

The non doped pin-diode absorption layer was decreased to 1700 nm. This nearly does not affect the dc-responsivity of the pin-diode which is at least 0.85 A/W. But this will increase the yield of the pin-diodes because of the shallower wafer topology. This leads to higher cut-off frequencies, because this is transit time rather than RC-time limited around 10 GHz.

Technology runs with an additional transistor mask set were done to check the new parameters. TLM-measurements (fig. 22) of the new layer stack have shown, that the sheet resistance decreases as expected and is now around R_{SH}≈100 Ω/square with a contact resistance R_C≈150 Ω*µm which is perfect for the designed resistor dimensions within the circuit.

5.6 Characterizing of TIAs

For testing the TIA separately from the pin-TIA circuits, circuits with electrical input were considered in the layout. Using a ground-signal-ground (GSG) probe an input signal is provided to the circuit. The layout of the TIA including the electrical output is the same as the design of the pin-TIA circuits. At the output a ground-signal-signal-ground (GSSG) probe is used to measure the differential output signal of the circuit.

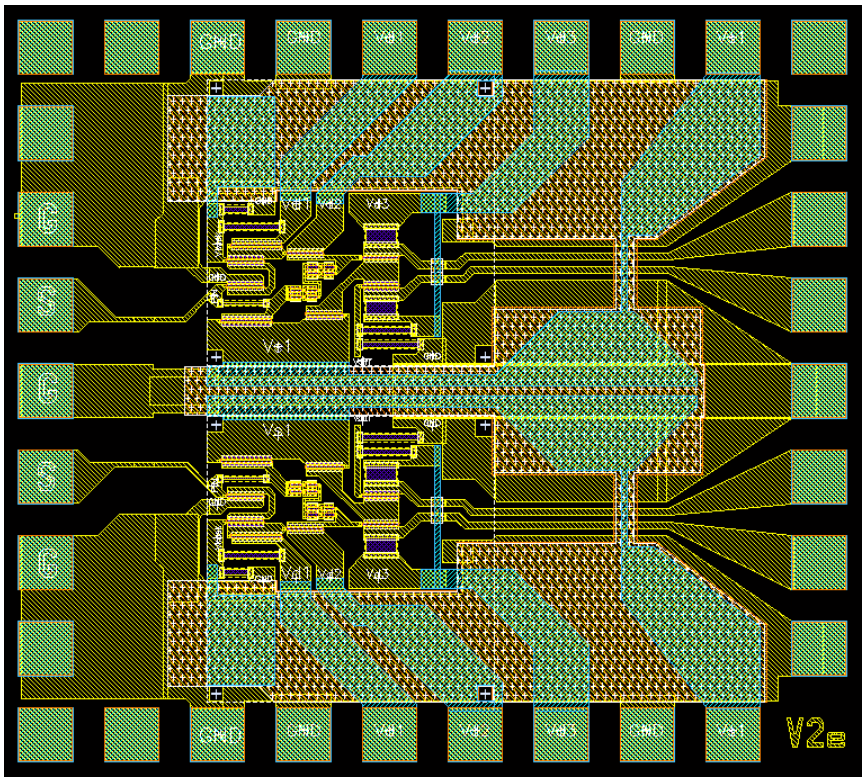


Fig. 30: EE-TIA for testing the TIA without pin-diodes

Tests in the rf-domain were performed by measuring the scattering parameters with a HP8510C Vector Network Analyzer. A dc-voltage of 0 V superposed with rf-signal of the analyzer by a bias-tee was connected to the input of the TIA. The differential outputs were connected via a GSSG probe to two cables of the same length and a dc-block. One of the dc-blocks was connected to the vector analyzer and the other to a 50 Ω broadband load to get the same measurement environment for both outputs.

5.7 Work Packet Objectives and Success

The strategic objective of WP3 was to realize and test balanced photoreceivers for synchronous optical RZ-QPSK transmission with polarization division multiplex using standard DFB lasers:

- Balanced photoreceivers
  - 9.5...12.5 GHz bandwidth
  - ≥0.85 A/W responsivity
  - 9 pA/√Hz input noise current density
  - InP substrate

The achievements meet the strategic objectives. However, the yield and the repeatability are very low. Even the best receiver we have, which has 8.5±1 GHz bandwidth, does not have a smooth response curve.

6 WP 4 & 5: Signal processing components and testbed (UPb)

6.1 Objectives

Signal processing component development is lead by University of Paderborn. It contains two major objectives: The development of high speed analog do digital converters (ADCs) in SiGe technology and the development of a CMOS signal processing system. Another workpackage is deicated to a complete realtime transmission demonstration testbed containing all components developed within the synQPSK project.

6.2 SiGe ADC

During the evaluation of the SiGe chip version A (analog-to-digital converter - ADC) it was discovered that the data and clock outputs of the circuit have no connection to the bond pads due to an omission of a via in the layout of the respective output stages. This allowed only the evaluation of the basic functionality of the circuit and the measurement of the main DC parameters. Therefore it was necessary to tapeout a corrected layout of the SiGe chip version A in August 2006 (month 26), which required a repeat of the milestones M4-2 (Tapeout of SiGe chip version A), M4-4 (Delivery of SiGe chip version A) and M4-6 (Results of SiGe chip version A). Fortunately the SiGe chip development was ahead of schedule which compensated for some of the delay caused by the re-tapeout of SiGe chip version A. However there remained a delay of 13 months for the tapeout of SiGe chip version B, as UPb has to await the results of the chip version A-II to ensure all functional capabilities. The increased delay of the results of SiGe chip version A-II was mostly caused by the higher than foreseen effort for bonding and testing CMOS chip version A, which was executed by the same staff members who were also in charge of testing SiGe chip version A-II.

6.3 Signal processing CMOS chip

The final CMOS chip (version B) is an integrated digital receiver that performs polarization multiplex QPSK data recovery. In order to achieve this main objective, real-time phase estimation and polarization control for a demultiplexed data strem are necessary.

CMOS chip version B is, as well as version A, splited into a full-custom design and a standard-cell design. The complexity of the interface was doubled compared to version A because two polarizations are used. This has big impacts on the mixed signal integration and packaging, which will be described in detail later in this chapter.

The full-custom designed 5 bit 1:8 demultiplexer was completely redesigned. The layout had to be more compact to be able to integrate four 5 bit 1:8 demultiplexer instances into CMOS chip version B. A single 5 bit 1:8 demultiplexer block area has shrunk by 30%. Problems that were encountered during the test of CMOS chip version A (refer to D10b) were addressed during this redesign. The width of the power and ground lines in the demultiplexer core has being increased to avoid thermal failure and to decrease IR drop. The test output of the 1:8 demultiplexed data was redesigned by adding CMOS logic – SCFL converter and a 50 Ω output driver. The layout of the primary clock distribution module which includes clock divider modules and clock control modules was redesigned so that it is more compact. Additional substrate contacts were incorporated to suppress noise. The testing in packaged form showed that the power consumption of the full custom demultiplexer is about 1.5 W. The divide by four clock divider operates up to 6.8 GHz input frequency (5 GHz being the maximum clock input frequency). The

demultiplexer test output signal eye diagram is open up to 9.5 GBit/s input data rate with 2^7-1 PRBS input data sequence when the following DSPU switched off.

During simulations and tests in the testbed with first FPGA based implementations as well as with CMOS chip version A, we gained more detailed experience in the system simulation model and the final specifications (D2, D11). The system model was therefore adapted and refined according to these experiences.

CMOS chip version B was optimized for testability and observability. The system model was extended to include modes of operation that allow system testing with well-defined starting conditions and detailed observations of internal signals, reduced complexity. Additional components were included (e.g., built-in self-test, BER counter, PRBS checker etc., refer to D13b and D17b for more details). Simulations and test cases during all design phases were increased to improve single component and regression tests. Complexity of the interface between full-custom and standard-cell based design was targeted with additional mixed-signal simulations. Clock domain crossing issues in the debug controller were simulated as well in digital as in analog and mixed signal simulations. Increasing testability was one of the major issues in the third reporting period.

The altered system model was much more complex compared to CMOS chip version A. The polarization control and the according Jones compensator modules had to be implemented according to the system model. These modules make up the major part of the gate count of CMOS chip version B. Implementing these functionality in VHDL was the second major issue during this reporting period.

Both the system simulation model as well as the VHDL implementation are fed with input data from a simulated transmission channel. To reduce the possibility of faults in the simulation environment, much effort was spent to test the VHDL implementation under realistic conditions. Therefore, the VHDL implementation had to be mapped to Xilinx FPGA devices that could be used in the synQPSK testbed. Furthermore, for easy testing and debugging of the implementation, an emulation of the system on the RAPTOR2000 rapid-prototyping environment (Refer to D17 for more details on the RAPTOR2000 system) was desirable. This had impact on the implementation style. All components of the synQPSK system were described with no dependencies to a specific target technology. All bit-width of the system were kept generic and configurable in the VHDL implementation. As this increases design and especially verification effort (e.g., tests can not be done with full enumeration), reusability increases. The additional effort easily paid off as the system could be adapted to different target platforms like the RAPTOR2000 system, the synQPSK testbed with FPGA board or CMOS chip version B.

Synthesis and backend for the CMOS chip version B were very time consuming tasks. An operating frequency of 625 MHz is very much at the limit of the used standard cell process. Therefore, many iterations of RTL coding, synthesis and backend took place before the layout complied to the requirements. During backend, the main parts of the mixed signal integration took part. The different blocks were placed manually, and the according simulations were also performed manually. For more details on the backend process, refer to D12b.

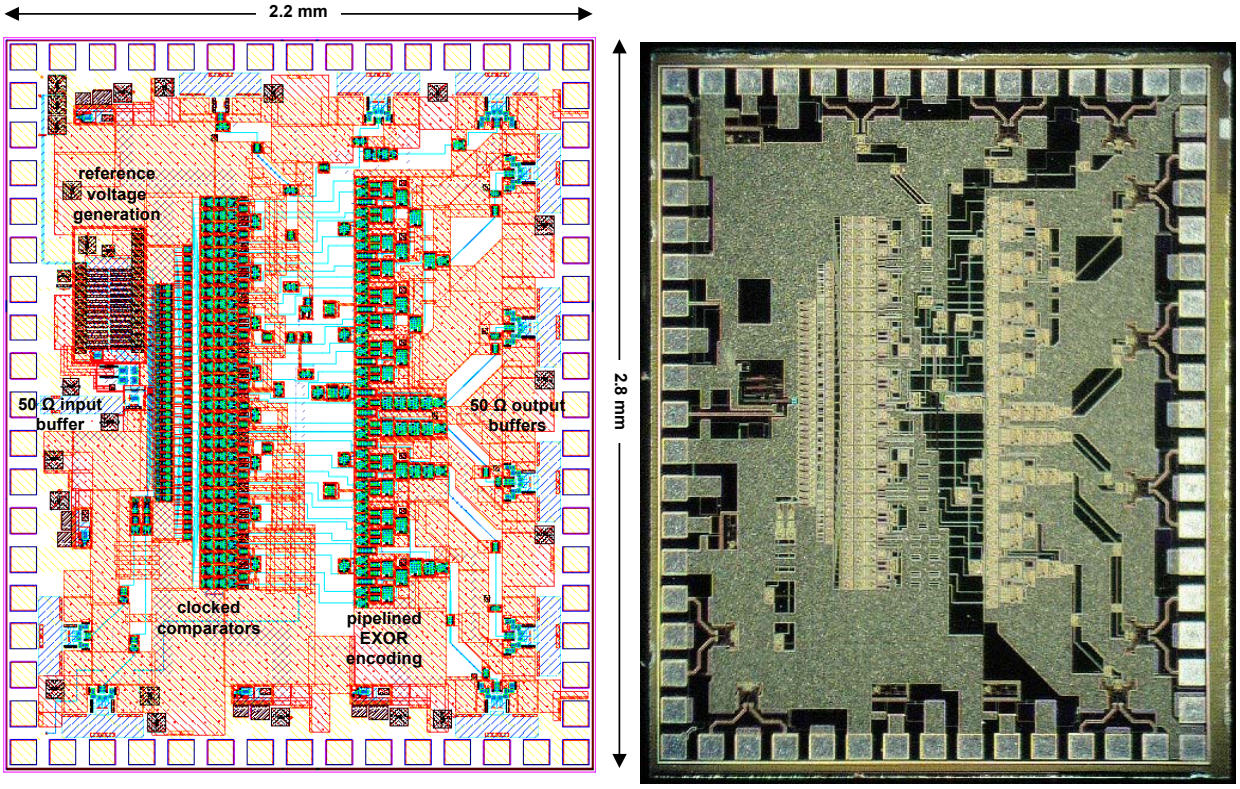
The test-plan for CMOS chip version B includes separated testing of the full-custom and standard-cell based design at first. The standard cell based design includes all components for a full featured built-in self-test. This test is used to test the functionality of the standard cell based design. For this test, a dedicated test environment was created. At first, a small number of CMOS chip version B dies were packaged in standard CQFP144 packages. The PCB that was created for the tests includes the according socket. The purpose of this PCB is the separated test of the standard cell based design of CMOS chip version B and functional tests of the complete chip at

low frequencies. For further details on the test environment and the accomplished tests, refer to D17b.

Full characterization of CMOS chip version B is only possible after integration in the synQPSK testbed because the needed input data cannot be created with other available equipment.

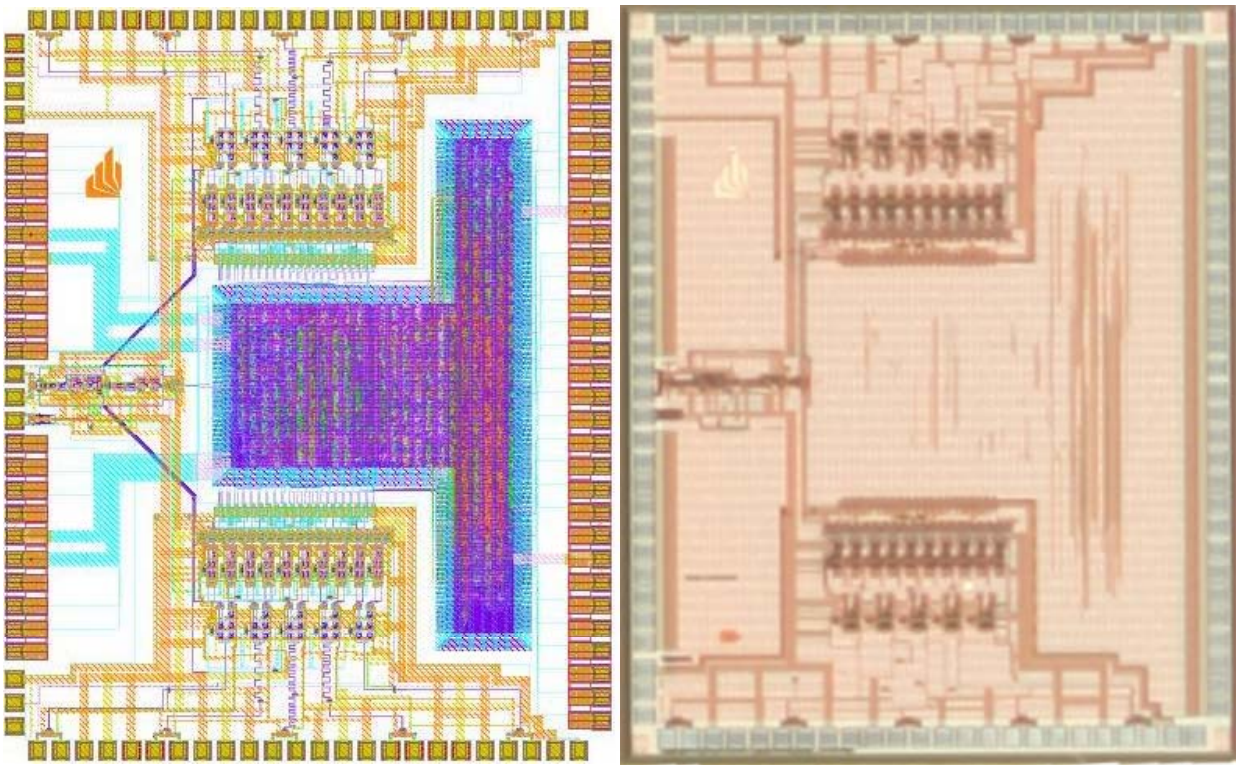
Full characterization of CMOS chip version B is performed after integration in the synQPSK testbed. Signaling between the four ADCs and CMOS chip version B is accomplished by four 5-bit wide differential lines that operate at a symbol-rate of 10GBaud. This means that 20 differential pairs have to be routed with equal lengths on a dedicated board. CMOS chip version B has to be connected to three different supply voltages, the four ADCs need an additional fourth voltage. A ceramic board was created as substrate because of its good high-frequency behavior.

CMOS chip version B is show in Fig. 33: a (layout), Fig. 33: b (chip photo), and Fig. 34: (packaged Chip). The PCB that was used for low-frequency testing of CMOS chip version B is shown in Fig. 35: . Finally, Fig. 36: shows the ceramic board that integrates four ADC version B and one CMOS chip version B for the tests in the synQPSK testbed.



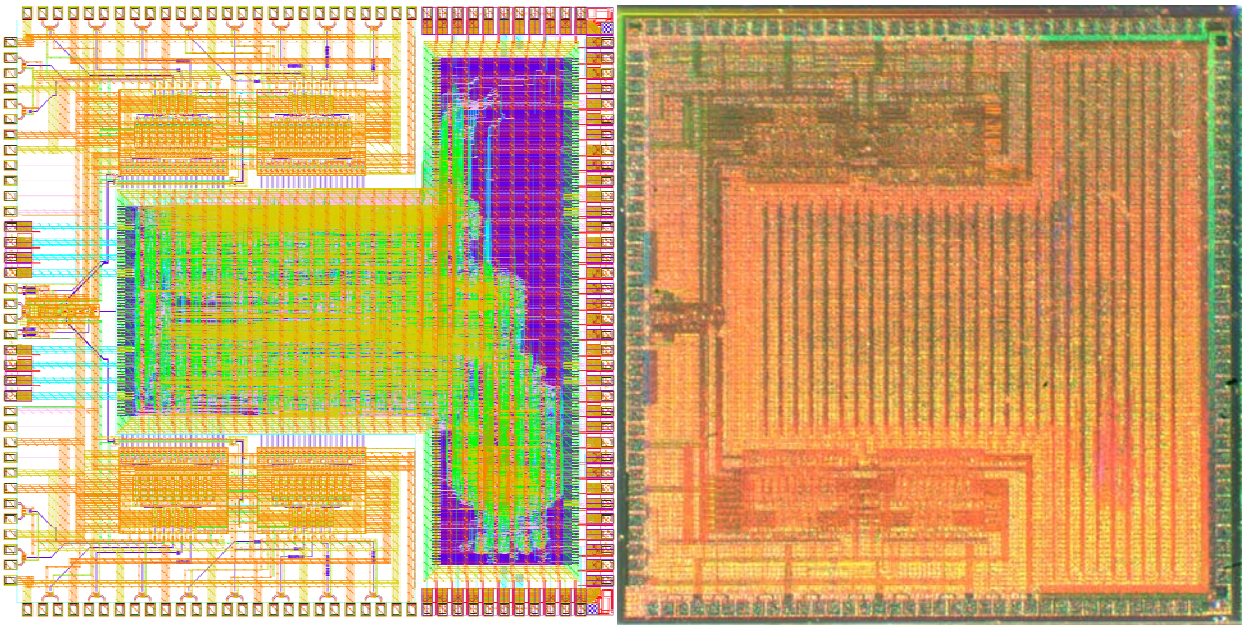
(a) **(b)**

Fig. 31: Layout and photograph of SiGe ADC version A



(b) **(b)**

Fig. 32: Layout and photograph of CMOS chip version A



(a) **(b)**

Fig. 33: Layout and photograph of CMOS chip version B

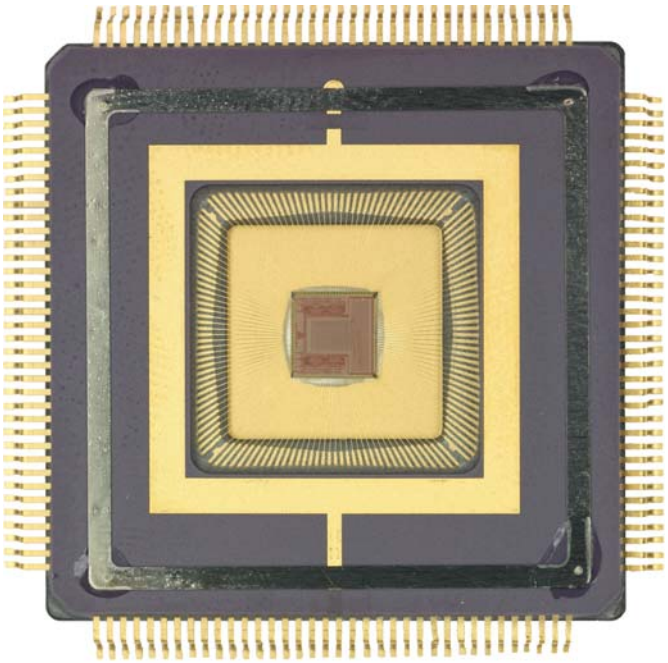


Fig. 34: CMOS chip version B in CQFP144 package

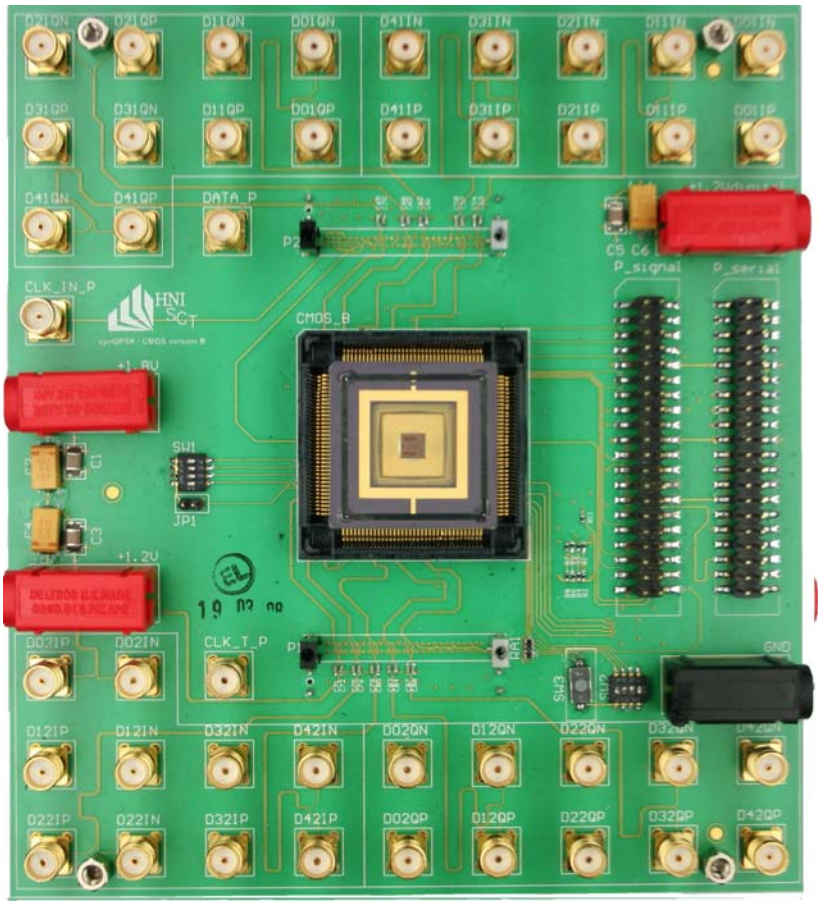


Fig. 35: Test-PCB for CMOS chip version B

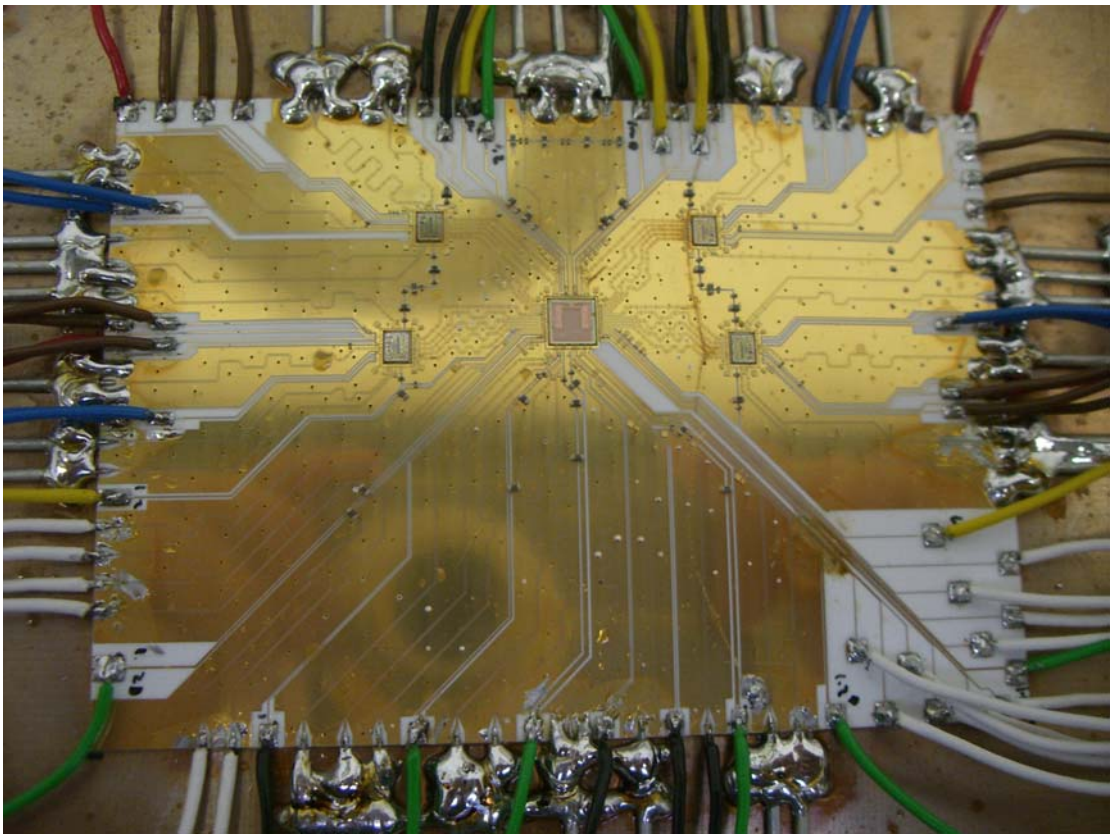


Fig. 36: Ceramic board for testbed integration of four ADC B and one CMOS B

All work of WP 4 was successfully finished. ADC version B meets the specifications. The standard cell based design of CMOS chip version B meets the specifications and the full-custom design works up to 6GBaud. Higher data rates could not be achieved in time because of underestimated power supply stabilization on the ceramic board. Higher operating frequencies will be reached after optimizing the ceramic board.

6.4 Synchronous QPSK component testbed (WP 5, UPb)

Although testbed evaluation of the components was officially split into two separate deliverables (D12 and D20) with a clear separation of which components are to be evaluated, the testbed development and experimental usage was a continuous process that required a lot of flexibility and occupied an unexpected high number of person months at the research group of Prof. Noé.

On the other hand, the continuous operation and improvement of the testbed not only served to fulfill the required evaluation tasks for all synQPSK components after delivery, separate measurements and integration into the testbed but also enabled several experiments that raised high interest within the scientific community: the first realtime QPSK transmission in 2006, the first realtime transmission with polarization multiplex in 2007 and currently (ECOC 2008) a polarization control that has ultra-high speed tracking capabilities.

All succesfully tested components developed within synQPSK (modulators from Photline, 90° hybrids from CIL, photo receivers from UDE and the ASICs from UPb) were finally evaluated in the testbed. The existence of a working realtime transmission demonstration system is also valuable for the beginning exploitation of the components. Visitors from science and industry are frequently asking for demonstration and explanation of the system.

Because of delayed availability, it was not possible to integrate the SiGe and CMOS chip versions A into the testbed, thus the first experiments had to be perfomed with commercially available ADCs and a FPGA that performed the DSP algorithms. The maximum achieved data rate of the synchronous QPSK transmission system was 1.6 Gb/s due to the limited performance of the standard components used instead. As the VHDL code used to program the FPGA was the same that was used for the synthesis of the CMOS chip, the correctness of the algorithm implemented in the standard cell part of the CMOS chip version A could be verified though.

The experience gained with this replacement for testbed A was useful because the availability of several components for testbed B was delayed. FPGA-based signal processing is still in use for experiments because modification of the VHDL-code does not require a new chip tapeout.

Full testing with all availiable components B, especially the ASICs, could only be perfomed at the very end of the projects, and the results indicate that some minor revisions would be necessary to reach the high challenge of a 40 Gbit/s system according to the specifications. The best data rate achieved with a reasonable BER was 10 Gbit/s.

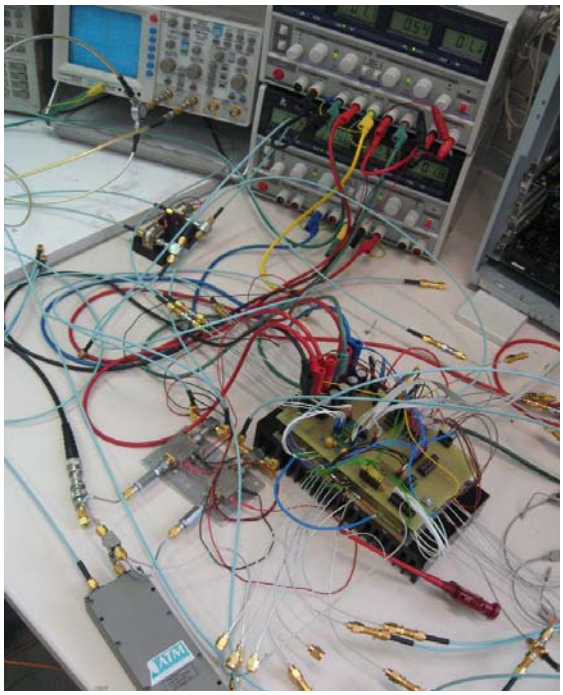


Fig. 37: SiGe and CMOS chips version B integrated into the synchronous QPSK component testbed.

Fig. 38 shows measurement results for 10 Gb/s polarization-multiplexed synchronous QPSK transmission. The distortions in the full-custom demultiplexer which are introduced by the noise from the CMOS standard cell part limit the performance of the system. If the polarization crosstalk is close to zero, the secondary diagonal elements of the polarization control matrix are close to zero, too, which reduces the switching noise in the standard cell part. In contrast if the polarization crosstalk is close to 50%, all elements of the polarization control matrix differ from zero and the switching noise increases. This is also verified by the fact that the power consumption of the CMOS chip increases, if there is crosstalk between the polarizations. The system performance with activated scrambler consequently lies in between these best case and worst case results.

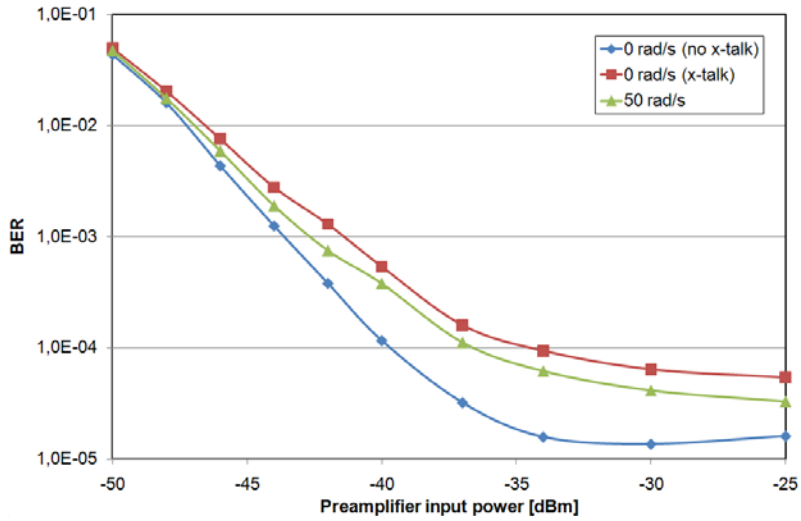


Fig. 38: Bit error rate vs. preamplifier input power for synchronous polarization-multiplexed QPSK transmission at 10 Gb/s for different polarization states at the receiver input.

6.5 Work Packet Objectives and Success

In the beginning of the project, UPb carried out system level simulations of various components to be developed in the synQPSK project. Additionally the digital feed-forward carrier recovery algorithm was optimized both in terms of hardware-efficiency and performance. On the basis of the simulated results two chips version A were developed. The SiGe chip version A was a 5 bit 10 Gs/s analog-to-digital converter (ADC). The CMOS chip version A was divided into two parts consisting of a full-custom designed 1:8 DEMUX and a standard-cell CMOS logic for carrier & data recovery. Included in the full-custom part were 50 Ω input buffers to be operated up to 10 Gb/s and a half rate (5 GHz) static clock divider. Although it was not possible to put the CMOS chip version A fully into operation, the experiences gained with the development of the chip were substantial for the design of CMOS chip version B. Additionally the VHDL code developed for the CMOS chip was used to realize the worldwide first realtime synchronous optical QPSK transmission with DFB lasers. For the experiment with a data rate of 1.6 Gb/s Photline's QPSK modulator version A, CeLight's optical 90° hybrid, commercially available photodiodes and ADCs and an FPGA for digital signal processing were employed.

7 Final plan for usage and dissemination of knowledge

This chapter presents the final exploitable results, which have a potential for industrial or commercial applications in research activities or for developing, creating or marketing a product or process. Additionally all actions of the synQPSK consortium are presented to disseminate the knowledge generated within the project.

The synQPSK consortium has assessed the market trend towards the technology that synQPSK is preferring. Based on recently published surveys, we can summarize our results as follows:

- The optical communication is moving toward 100 Gb/s, both at metro and long haul.
- There are no commercial solutions and components for 100 Gb/S. Therefore, as an interim solution; there will be in the next few years embodiment of 40 Gb/s systems.
- A major factor in the long haul communication method to be chosen is the spectral efficiency.

The need for high spectral efficiency drove the communication community to advanced modulation formats like QPSK. The most popular approach is exactly the synQPSK solution: QPSK modulation with polarization multiplexing. The efforts of the synQPSK consortium to exploit and disseminate the knowledge and products developed within the project are documented.

7.1 Photline

In the frame of synQPSK, Photline was early involved in the development of a new type of QPSK modulator. Thanks to synQPSK, Photline was able to launch rapidly a commercial product begin of year 2006.

Although the QPSK modulation format is at early stage of developments, Photline was among the first of the lithium niobate competitors to launch this product and to propose a reliable and performing solution. This product has already been supplied or sampled and tested by major actors of systems and subsystems of transmission (see post-deadline paper of Telcordia at OFC'2007).

Today, the family of modulators produced and commercialised by Photline is the following:

Modulators		**Applications**
MX-LN-10-20-40:	X-cut and zero chirp modulator 1300nm and 1550 nm wavelength f	Telecom, 10 to 40 Gbps applications
MXAN-LN-10-20	X-cut LiNbO3, titanium indiffused Analogue intensity modulator	Defence, aerospace
MXPE-LN-10	X-cut LiNbO3, proton exchange and high extinction ratio intensity modulator	Sensing, pulse shaping
MPZ-LN-10-40 and MPX-LN-05	Z-cut high speed phase modulators and X-cut OEM phase modulators	Telecom,

CMD-LN-10:	X-cut modulator co-packaged with RF GaAs driver	Telecom
QPSK-LN-40	**X-cut QPSK modulators for use at 2x10 & 2x20 Gb/s**	**Telecom**
NIR- MX-LN & NIR-MPX-LN	X-cut & proton exchange Phase and intensity modulators working at 850, 980 & 1064 nm wavelength	Industrial high power pulsed fibre lasers

Table 1: Photline's family of modulators.

QPSK modulators are one of these families of products. They represent about 12% of the sales of modulators by Photline, in 2007. QPSK is expected to be the next generation modulation format of high capacity fiber optic networks. Photline who is a recent and innovative actor in the field of lithium niobate optical components anticipates a rapid increase of the sales of QPSK modulators, which could be the replacement technology of former 10 Gb/s systems and the real alternative to standard 40 Gb/s NRZ and RZ format whose performances are highly limited by PMD and nonlinearities and cost of specific fibers. QPSK modulators are the real opportunity for Photline to become a major actor in telecom modulators.

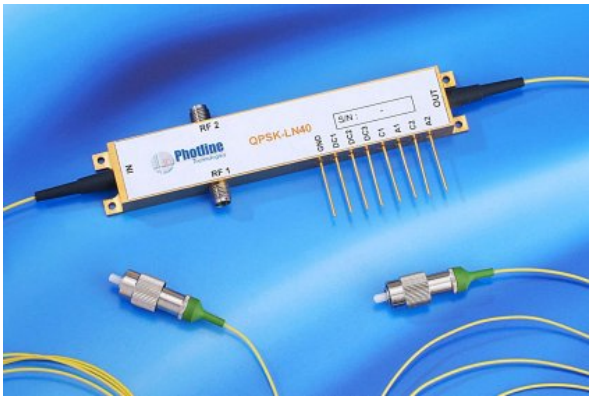


Fig. 39: Image of the commercial QPSK modulator from Photline

If QPSK systems are deployed during the next three years, this could amount to a major part of the Photline sales. Sales of 1 M€/year with 500 pieces/year can be expected when the business will really start to ramp up.

Fig. 40: Advertisement from Photline published in "Laser Focus World"

7.2 CeLight Israel

CeLight Israel is already selling the optical 90° hybrid CL-QOH-90 shown in Fig. 41, whose latest version is the result of activity within the synQPSK project. It can be used for coherent signal demodulation. The $LiNbO_3$ integrated component accepts two optical signals (S_1& S_2) and generates four output signals: {S_1+jS_2, S_1-jS_2, S_1+S_2, S_1-S_2}. By attaching two balanced receivers to the output of the hybrid, the relative phase information between the input signals can be extracted via differential detection and digital signal processing.

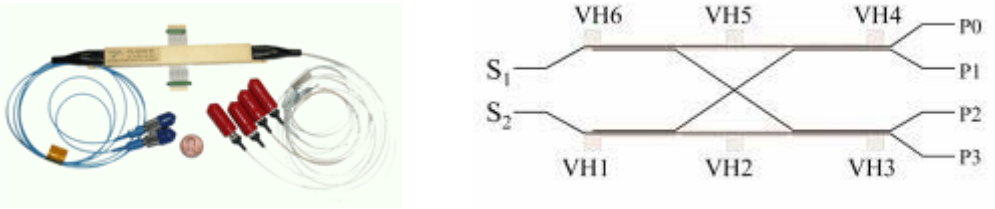


Fig. 41: CeLight's optical 90° hybrid CL-QOH-90 (left) and its schematic (right).

CIL also began advertising the coherent receiver CL-CR-10 on its website (Fig. 42). It provides an integrated solution packaging CeLight's optical 90° hybrid with commercially available balanced detectors in one compact device to provide a 10X reduction in size and dramatically higher reliability. The first model (with the non-integrated TIA) is ready as a commercial product since three months and is now being quoted. CIL is expecting a sales of 0.5 M€ with 250 pieces until 2010.

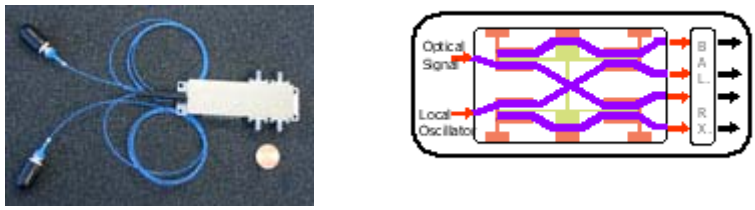


Fig. 42: CeLight's coherent receiver CL-CR-10 (left) and its schematic (right).

7.3 University of Duisburg-Essen

Within the synQPSK Project UDE improved the knowledge of developing and characterizing OEIC-circuits. Single devices are well known at UDE can be easily designed, processed and characterized, but to develop new circuits using these single devices creates new challenges. During the project UDE learned to transfer its knowledge of single device measurements to circuit measurements. Two new test setups for on-wafer characterization of rf OEIC-circuits were developed. The optical measurement techniques at high frequencies were improved. We are now able to measure pin-diodes and OEICs up to frequencies of 20 GHz which makes us attractive for the cooperation with industrial partners. One of the first industrial partners for pin-diodes with a customized layout is CeLight, other industrial partners interested in vertical pin-diodes follow.

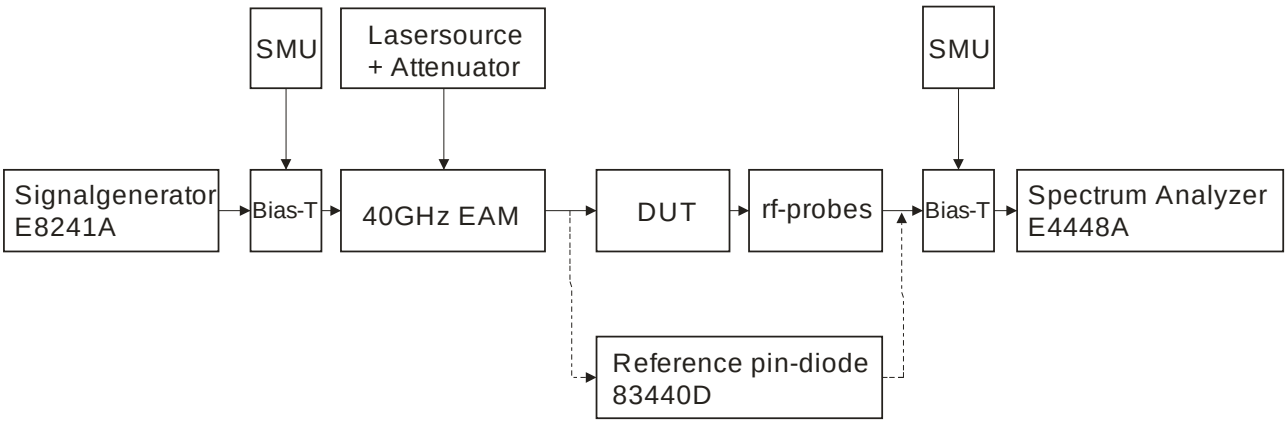


Fig. 43: Schematic diagram of the developed optical/electrical on-wafer measurement setup

One bachelor thesis on the development of optical rf-measurement setup ("Aufbau eines optischen Hochfrequenzmessplatzes") and two diploma thesis on simulation and characterization of opto-electronic receiver circuits ("Simulation und Untersuchung von opto-elektronischen Empfängerschaltungen" and "Entwicklung eines Transimpedanzverstärkers mit balanciertem Eingang") were accomplished within the synQPSK Project. The developments, designs, fabricated circuits and experimental results will form the core of the Ph.D. thesis of I. Nannen, the main project scientist.

7.4 University of Paderborn

Thanks to the first realtime synchronous QPSK transmission with digital feed-forward carrier recovery and standard DFB lasers in the year 2006 and the first realtime polarization-multiplexed QPSK transmission with electronic polarization control in the year 2007, UPb was asked to give invited presentations at various workshops and conferences all over the world. Altogether UPb published 7 invited and 14 contributed conference and workshop papers as well as 9 journal publications (see section 7.6), thus contributing heavily to the knowledge transfer within the scientific community. Two more invited presentations will follow at this year's APOC and next

year's OFC/NFOEC conference. Also further contributed conference and journal publications are planned.

In order to raise also the public awareness about the synQPSK project, UPb published four press releases (Table 2). They were composed in English and German and were sent to international optical journals and websites, but also to local newspapers. All press releases are available on the consortium website.

Release date	Content	Language
July 30, 2004	Start of the synQPSK-project	English, German
June 30, 2006	Worldwide first realtime synchronous optical quadrature phase shift keying data transmission with standard lasers	English, German
March 21, 2007	Real-time electronic polarization tracking enables optical polarization-multiplexed QPSK transmission	English, German
November 29, 2007	synQPSK selected as one of 100 products of the future	German

Table 2: Press releases published by UPb.

The analog-to-digital converter was presented to the public at an exhibition within the 1st NRW-Nano-Konferenz. Fig. 44 shows the booth of the University of Paderborn, where among other actual research results the SiGe chip version B was presented.

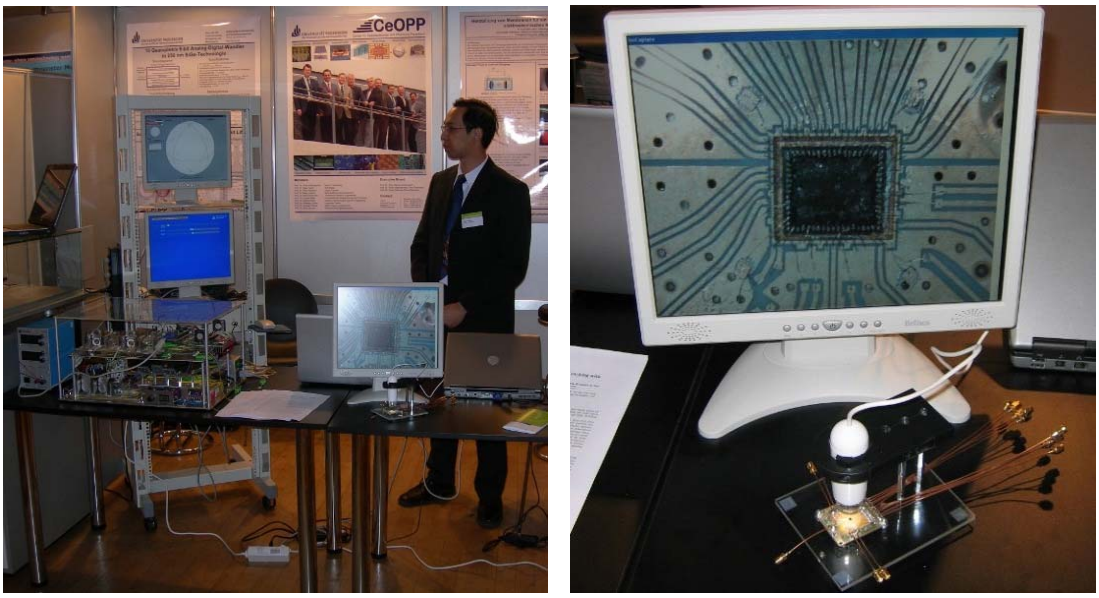


Fig. 44: Booth of UPb at the 1st NRW Nano-Konferenz (left) and the presented analog-to-digital converter module (right).

First contacts are already established concerning the exploitation of the research results. Several analog-to-digital converters developed within the synQPSK project are sold to CeLight Inc. in the USA. Other companies sent enquiries – also for the CMOS chip. UPb is subcontractor in a nationally funded project together with Ericsson and CoreOptics that in one project part extends the work of the synQPSK programme towards compensation of dispersion and nonlinear effects.

The project also contributed to educational activities through lectures, Ph.D. projects, M.Sc. graduation projects and B.Sc. graduation projects. The basics of synchronous QPSK transmission are part of the lecture “Optical Communication A”, which is addressed to Master students in electrical engineering. More specialized talks about actual research results were presented in the Graduate Lecture “Optoelectronics & Photonics”. The different graduation projects that were prepared within the synQPSK project are listed in Table 3. Three more Ph.D. projects of R. Peveling, V. Herath and T. Pfau are still running and are therefore not yet listed in Table 3.

Author	Title	Year	Type
J. Romoth	Optimierung und Implementierung einer Signalverarbeitungseinheit zur Demodulation von QPSK-Daten	2006	B.Sc. thesis
F. Samson	Entwicklung einer Polarisationskontrolle für die optische Nachrichtenübertragung	2006	M.Sc. thesis
C. Wördehoff	Optimierung einer Polarisationsregelung für die optische Nachrichtenübertragung	2007	M.Sc. thesis
S. Hoffmann	Hardwareeffiziente Echtzeit-Signalverarbeitung für synchronen QPSK-Empfang	2008	Ph.D. thesis

Table 3: Ph.D. projects, M.Sc. and B.Sc. graduation projects at the University of Paderborn.

The transmission system developed within the synQPSK-project was selected as one of 100 products of the future by a committee consisting of prominent specialists headed by the Nobel Prize winner Theodor Hänsch. The selection of the committee is published in the book “100 Produkte der Zukunft” (ISBN-13: 978-3430200356), which delivers “an impressive overview over innovative products developed in German laboratories, institutes and think tanks.” (magazine “Stern” / 27.09.2007). Fig. 45 depicts the cover of the book.

Fig. 45: Cover of the book “100 Produkte der Zukunft” (100 products of the future), published by Nobel Prize winner Theodor Hensch. The synQPSK project was selected as one of these products.

Also another Nobel Prize winner visited the laboratories at UPb. Fig. 46 shows how Prof. Noé explains the principles of coherent polarization-multiplexed QPSK transmission to Klaus von Klitzing, who won the Nobel Prize in physics for the discovery of the Quantum-Hall-Effect.

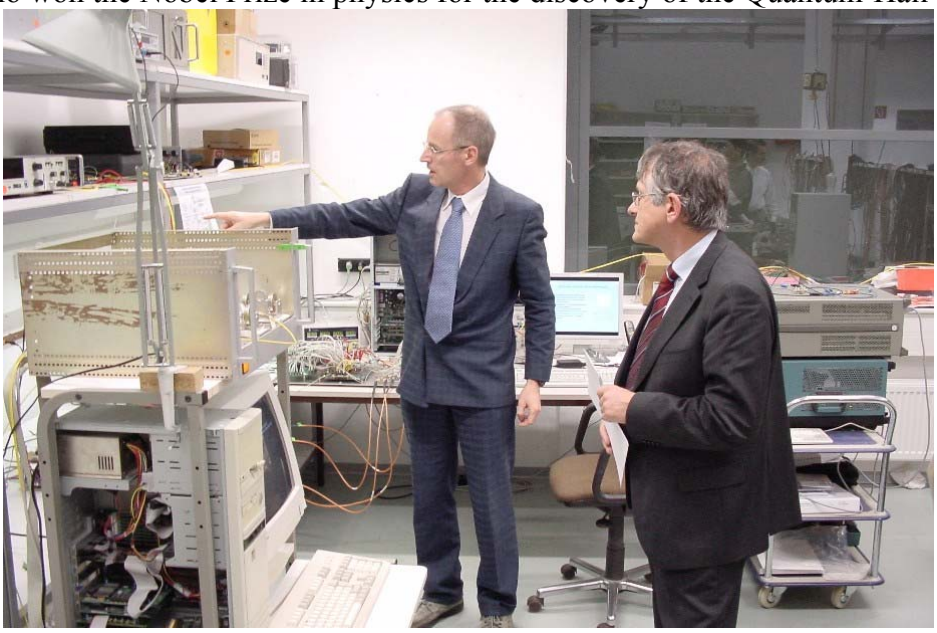


Fig. 46: Prof. Noé presents the synQPSK testbed to Nobel Prize winner Klaus von Klitzing.

7.5 Dissemination of knowledge

Planned/actual Dates	Type	Type of audience	Countries addressed	Partners responsible /involved
26-30 April 2004	Photonics Europe 2004 conference presentation	Research, industry, higher education, general public	Europe	Photline/all
12-16 July 2004	OECC 2004 conference presentation and publication [1]	Research	World	UPb
30 July 2004	Press release	General public	World	UPb/all
since July 2004	Project web-site	Research, industry, higher education, general public	World	UPb/all
Feb. 2005	Journal publication [2]	Research	World	UPb
April 2005	Journal publication [3]	Research	World	UPb
12-14 April 2005	Poster in Brussels during photonics exhibition of VDI	Research, Industry	Europe	UPb/all
June 2005	Contribution to Brochure of VDI	Research, Industry	Germany, Europe	UPb/all
Sept. 2005	Poster at Photline booth during ECOC 2005 exhibition	Research, Industry	Europe, World	Photline/all
March 2006	Journal publication [4]	Research	France	Photline
June 2006	OAA/COTA 2006	Research	World	UPb/CIL/all

Planned/actual Dates	Type	Type of audience	Countries addressed	Partners responsible /involved
	conference presentation and publication [5], [6], [7], [8]			
30 June 2006	Press release	General public	Germany, World	UPb/all
Sept. 2006	Journal publication [9]	Research	World	UPb/all
Sept. 2006	Journal publication [10]	Research	World	UPb/all
Sept. 2006	ECOC 2006 conference presentation and publication [11]	Research	Europe, World	UPb/all
Oct. 2006	FiO 2006 conference presentation and publication [12], [13]	Research	USA, World	UPb
Nov. 2006	Journal publication [14]	Research	France	Photline
Feb. 2007	Workshop presentation and publication [15]	Research, Industry	Germany	UPb
21 March 2007	Press release	General public	Germany, World	UPb/all
June 2007	IMS 2007 conference presentation and publication [16]	Research	USA, World	UPb/all
July 2007	IEEE Summer Topicals 2007 conference presentation and publication [17], [18]	Research	USA, World	UPb/all
Sept. 2007	Book publication “100 Produkte der Zukunft”	General public	Germany	UPb/all
Sept. 2007	ECOC 2007 workshop presentation and publication [19]	Research, Industry	Europe, World	UPb
Sept. 2007	ECOC 2007 conference presentation and publication [20], [21]	Research	Europe, World	UPb/Photline/all
29 Nov. 2007	Press release	General public	Germany	UPb/all
Dec. 2007	Journal publication [22]	Research	World	UPb/all
Jan. 2008	Journal publication [23]	Research	World	UPb
18-19 Feb. 2008	Exhibition at the 1st NRW-Nanokonferenz	Industry, General public	Germany	UPb
Feb. 2008	OFC/NFOEC 2008 conference presentation and publication [24]	Research	USA, World	UPb/all
June 2008	Workshop presentation and publication [25]	Research, Industry	Germany	UPb
June 2008	Workshop presentation and publication [26]	Research, Industry	Japan, World	UPb
July 2008	IEEE/LEOS Summer Topicals 2008 conference presentation and publication [27], [28], [29]	Research	USA, World	UPb/all
July 2008	COTA 2008 conference presentation and	Research	USA, World	UPb

Planned/actual Dates	Type	Type of audience	Countries addressed	Partners responsible /involved
	publication [30]			
Aug. 2008	Journal publication [31]	Research	World	UPb
Sept. 2008	Journal publication [32]	Research	World	UPb
Sept. 2008	ECOC 2008 conference presentation and publication [33]	Research	Europe, World	UPb/all
Sept. 2008	Journal publication [33]	Research	World	UPb

Table 4: Dissemination of knowledge

All disseminations of knowledge listed in Table 4 are available on the consortium website.

7.6 List of scientific publications

[1] R. Noé, *Phase noise tolerant synchronous QPSK receiver concept with digital I&Q baseband processing*, Proc. OECC/COIN2004, 16C2-5, July 12-16, 2004, Yokohama, Japan.

[2] R. Noé, *Phase Noise Tolerant Synchronous QPSK/BPSK Baseband-Type Intradyne Receiver Concept with Feedforward Carrier Recovery*, IEEE J. Lightwave Technology, Vol. 23, 2005, pp. 802-808.

[3] R. Noé, *PLL-Free Synchronous QPSK Polarization Multiplex/Diversity Receiver Concept with Digital I&Q Baseband Processing*, IEEE Photon. Technol. Lett., Vol. 17, 2005, pp. 887-889.

[4] H Porte, J. Hauden, N. Grossard, R. Noé, *Modulateur QPSK intégré dans $LiNbO_3$ pour codage 2x10 Gb/s*, Journée Optique et Micro-onde, March 24, 2006, Rouen, France.

[5] P. Cho, G. Harston, A. Greenblatt, A. Kaplan, Y. Achiam, R. Bertenburg, A. Brennemann, B. Adoram, P. Goldgeier, A. Hershkovits, *Integrated Optical Coherent Balanced Receiver*, Proc. OAA/COTA 2006, CThB2, June 25-30, 2006, Whistler, Canada.

[6] R. Noé, U. Rückert, Y. Achiam, F.-J. Tegude, H. Porte, *European „synQPSK" Project: Toward Synchronous Optical Quadrature Phase Shift Keying with DFB Lasers*, Proc. OAA/COTA 2006, CThC4, June 28-30, 2006, Whistler, Canada

[7] T. Pfau, S. Hoffmann, R. Peveling, S. Bhandare, S. Ibrahim, O. Adamczyk, M. Porrmann, R. Noé, Y. Achiam, *Real-time Synchronous QPSK Transmission with Standard DFB Lasers and Digital I&Q Receiver*, Proc. OAA/COTA2006, CThC5, June 28-30, 2006, Whistler, Canada

[8] S. Hoffmann, T. Pfau, O. Adamczyk, R. Peveling, M. Porrmann, R. Noé, *Hardware-Efficient and Phase Noise Tolerant Digital Synchronous QPSK Receiver Concept*, Proc. OAA/COTA 2006, CThC6, June 28-30, 2006, Whistler, Canada

[9] T. Pfau, S. Hoffmann, R. Peveling, S. Bhandare, S. K. Ibrahim, O. Adamczyk, M. Porrmann, R. Noé, Y. Achiam, *First Real-Time Data Recovery for Synchronous QPSK Transmission with Standard DFB Lasers*, IEEE Photon. Technol. Lett., vol. 18, Sept. 15, 2006, pp. 1907-1909

[10] T. Pfau, S. Hoffmann, R. Peveling, S. Ibrahim, O. Adamczyk, M. Porrmann, S. Bhandare, R. Noé, Y. Achiam, *Synchronous QPSK Transmission at 1.6 Gbit/s with Standard DFB*

Lasers and Real-time Digital Receiver, Electron. Lett., vol. 18, Sept. 2006, pp. 1175-1176

[11] T. Pfau, S. Hoffmann, R. Peveling, S. Bhandare, O. Adamczyk, M. Porrmann, R. Noé, Y. Achiam, *1.6 Gbit/s Real-Time Synchronous QPSK Transmission with Standard DFB Lasers*, Proc. ECOC 2006, Mo4.2.6, Sept. 24-28, 2006 Cannes, France.

[12] R. Noé, T. Pfau, *Synchronous Demodulation of Optical Phase Shift Keying in Coherent Systems with DFB Lasers*, Proc. FiO 2006, FMF3 (invited), Oct. 8-12, 2006, Rochester, NY, USA.

[13] R. Noé, T. Pfau, Y. Achiam, F.-J. Tegude, H. Porte, *Integrated Components for Optical QPSK Transmission*, Proc. FiO 2006, FMF4, Oct. 8-12, 2006, Rochester, NY, USA.

[14] N. Grossard, J. Hauden, H. Porte S. K. Ibrahim, S. B., R. Noé, *Modulateur QPSK en niobate de lithium coupe X pour modulation 10Gb/s en mode RZ-DQPSK*, submitted to Journées Nationales d'Optiques Guidée JNOG'2006, Metz, November 2006

[15] S. Hoffmann, T. Pfau, R. Peveling, S. Bhandare, O. Adamczyk, M. Porrmann, R. Noé, *PLL-free coherent optical QPSK transmission with realtime digital phase estimation using DFB lasers*, Workshop der ITG Fachgruppe 5.3.1, Modellierung photonischer Komponenten und Systeme, Feb. 12-13, 2007, Lehrstuhl für Nachrichtentechnik, TU München, Germany

[16] R. Noé, T. Pfau, O. Adamczyk, R. Peveling, V. Herath, S. Hoffmann, M. Porrmann, S. Ibrahim, S. Bhandare, *Real-Time Digital Carrier & Data Recovery for a Synchronous Optical Quadrature Phase Shift Keying Transmission System*, Proc. IMS2007, TH2E-01 (invited), June 3-8, 2007, Honolulu, HI, USA.

[17] T. Pfau, O. Adamczyk, V. Herath, R. Peveling, S. Hoffmann, M. Porrmann, R. Noé, *Realtime Optical Synchronous QPSK Transmission with DFB Lasers*, Proc. IEEE/LEOS Summer Topicals 2007, Ma3.2 (invited), July 23-25, 2007, Portland, OR, USA

[18] T. Pfau, R. Peveling, S. Hoffmann, S. Bhandare, S. Ibrahim, D. Sandel, O. Adamczyk, M. Porrmann, R. Noé, Y. Achiam, D. Schlieder, A. Koslovsky, Y. Benarush, J. Hauden, N. Grossard, H. Porte, *PDL-Tolerant Real-time Polarization-Multiplexed QPSK Transmission with Digital Coherent Polarization Diversity Receiver*, Proc. IEEE/LEOS Summer Topicals 2007, Ma3.3, July 23-25, 2007, Portland, OR, USA.

[19] S. Hoffmann, R. Peveling, O. Adamczyk, T. Pfau, R. Noé, *Realtime coherent QPSK transmission: comparison of two carrier phase recovery approaches*, Workshop 5, ECOC 2007, Sept. 16-20, 2007, Berlin, Germany

[20] T. Pfau, R. Peveling, F. Samson, J. Romoth, S. Hoffmann, S. Bhandare, S. Ibrahim, D. Sandel, O. Adamczyk, M. Porrmann, R. Noé, J. Hauden, N. Grossard, H. Porte, D. Schlieder, A. Koslovsky, Y. Benarush, Y. Achiam, *Polarization-Multiplexed 2.8 Gbit/s Synchronous QPSK Transmission with Real-Time Digital Polarization Tracking*, Proc. ECOC 2007, 8.3.3, Sept. 16-20, 2007, Berlin, Germany.

[21] H. Porte, J. Hauden, N. Grossard, S. Ibrahim, R. Noé, P. Mollier, *Low chirp QPSK modulator integrated in poled Z-cut LiNbO3 substrate for 2 x MultiGb/s transmission*, Proc. ECOC 2007, 10.3.5, 16-20 Sept. 2007, Berlin, Germany.

[22] T. Pfau, R. Peveling, H. Porte, Y. Achiam, S. Hoffmann, S. K. Ibrahim, O. Adamczyk, S. Bhandare, D. Sandel, M. Porrmann, R. Noé, *Coherent Digital Polarization Diversity Receiver for Real-Time Polarization-Multiplexed QPSK Transmission at 2.8 Gbit/s*, IEEE Photon. Technol. Lett., Vol. 19, No. 24, Dec. 15, 2007, pp. 1988 - 1990

[23] T. Pfau, S. Hoffmann, O. Adamczyk, R. Peveling, V. Herath, M. Porrmann, R. Noé, *Coherent optical communication: Towards realtime systems at 40 Gbit/s and beyond*, Optics Express, Vol. 16, No. 2, Jan. 21, 2008

[24] T. Pfau, C. Wördehoff, R. Peveling, S. Ibrahim, S. Hoffmann, O. Adamczyk, S. Bhandare, M. Porrmann, R. Noé, A. Koslovsky, Y. Achiam, D. Schlieder, N. Grossard, J. Hauden, H. Porte, *Ultra-Fast Adaptive Digital Polarization Control in a Realtime Coherent Polarization-Multiplexed QPSK Receiver*, Proc. OFC/NFOEC 2008, OTuM3, Feb. 24-28, 2008, San Diego, CA, USA

[25] S. Hoffmann, T. Pfau, R. Peveling, S. Bhandare, O. Adamczyk, M. Porrmann, R. Noé, *Hardwareeffiziente Frequenz- und Phasenschätzung für QPSK-Intradynempfang*, Workshop of VDE-ITG-FG 5.3.1, June 12-13, 2008, Kiel, Germany

[26] T. Pfau, R. Noé, *Realtime Digital Coherent QPSK Transmission: Algorithms and Technologies*, Proc. HDOC-WS 2008, pp. 83-88, June 25-26, 2008, Tokyo, Japan

[27] R. Noé, S. Hoffmann, T. Pfau, O. Adamczyk, V. Herath, R. Peveling, M. Porrmann, *Realtime Digital Polarization and Carrier Recovery in a Polarization-Multiplexed Optical QPSK Transmission*, Proc. IEEE/LEOS Summer Topicals 2008, MC2.1 (invited), July 21-23, 2008, Acapulco, Mexico

[28] T. Pfau, M. El-Darawy, C. Wördehoff, R. Peveling, S. Hoffmann, B. Koch, O. Adamczyk, M. Porrmann, R. Noé, *32-krad/s Polarization and 3-dB PDL Tracking in a Realtime Digital Coherent Polarization-Multiplexed QPSK Receiver*, Proc. IEEE/LEOS Summer Topicals 2008, MC2.4, July 21-23, 2008, Acapulco, Mexico

[29] O. Adamczyk, R. Noé, *5-bit 12.5 Gsamples/s Analog-to-Digital Converter for a Digital Receiver in a Synchronous Optical QPSK Transmission System*, Proc. IEEE/LEOS Summer Topicals 2008, TuC3.2, July 21-23, 2008, Acapulco, Mexico

[30] S. Hoffmann, T. Pfau, O. Adamczyk, C. Wördehoff, R. Peveling, M. Porrmann, R. Noé, S. Bhandare, *Frequency Estimation and Compensation for Coherent QPSK Transmission with DFB Lasers*, Proc. COTA 2008, CWB4, July 13-16, 2008, Boston, MA, USA

[31] O. Adamczyk, R. Noé, *13 Gsample/s 5-bit analogue-to-digital converter for coherent optical QPSK receiver*, Electron. Lett., vol. 44, 2008, pp.895-896

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[33] M. El-Darawy, T. Pfau, C. Wördehoff, B. Koch, S. Hoffmann, R.Peveling, M Porrmann, R. Noé, *Realtime 40 krad/s Polarization Tracking with 6 dB PDL in Digital Synchronous Polarization-Multiplexed QPSK Receiver*, Proc. ECOC 2008, We.3.E.4, Sept. 21-25, 2008, Brussels, Belgium.

[34] M. El-Darawy, T. Pfau, S. Hoffmann, R. Peveling, C. Wördehoff, B. Koch, M. Porrmann, O. Adamczyk, R. Noé, *Fast Adaptive Polarization and PDL Tracking in a Realtime FPGA Based Coherent QPSK PolDM-QPSK Receiver*, IEEE Photon. Technol. Lett., accepted for publication. Lett., accepted for publication.

[35] I. Nannen, A. Poloczek, A. Matiss, W. Brockerhoff, I. Regolin, F.-J. Tegude, *InP-HEMT-TIA with Differential Optical Input Using Vertical High Topology PIN-Diodes*, IPRM07, May 2007, Japan

7.7 Conclusion

During the last three years, the members of synQPSK were the main contributors to open discussion in the technology and to the presentation of the enabling components, including the essential algorithms and its embodiments. synQPSK was the first to show a real-time

polarization multiplexing, optical coherent receiver and a chirp-free Z-cut lithium Niobate QPSK modulator. synQPSK is the only group that successfully employs standard DFB low-cost lasers together with its advanced phase recovery algorithms and thus reduce the cost of the end units.

The QPSK modulator from Photline is not only subject of scientific publications (see section 7.6) but is also available as a commercial product now, independent from the other synQPSK components (see section 7.1). CeLight is already selling the CL-QOH-90 Optical Hybrid, whose latest version is the result of activity within the synQPSK project and will soon begin to advertise the Coherent Receiver on its website (see section 7.2).

While most of the commercial companies that are now trying to develop the optical QPSK technology keep their effort secret, synQPSK published the approach and demonstrated how the main elements of the method are working. synQPSK was and is the public focal point to the proof of concept, and thus realized the dissemination an exploitation of QPSK knowledge – one of the main project's targets.

During the last few month the two commercial companies, Photline and CeLight Israel see a surge in the request for quotations for their QPSK components – an indicator for commercial products that will be an output of the project. The modulator of Photline is a stand-alone product. The coherent receiver needs cooperation between CeLight Israel and UDE. CeLight Israel and UDE are discussing the establishment of a commercial entity that will reside at UDE fab and will fabricate the diode arrays for CIL, an entity similar to that of IPAG.

UPB has been asked for additional samples of the ADCs developed within synQPSK by Celight. Celight plans to exploit these components for several related commercial applications. Huawei, the leading chinese telecom company, has asked UPB for signal processing components.

8 Project summary

The synQPSK project has yielded commercially available components (QPSK modulator, 90° hybrid, 90° hybrid with photoreceiver), pre-commercial research samples (SiGe 10-Gs/s-ADCs, CMOS signal processing chip, evaluation boards for these), the worldwide first realtime synchronous QPSK transmission with DFB lasers, the worldwide first realtime polarization-multiplexed synchronous QPSK transmission and electronic polarization control, also with DFB lasers, the (until now) worldwide fastest experimental demonstration of electronic polarization control (40 krad/s) and the worldwide second (after Nortel) set of synQPSK ASICs (SiGe, CMOS). Regarding LiNbO3 components (QPSK modulators, 90° hybrids) expectations have been fully reached. Regarding InP photoreceivers there is presently a yield problem, still caused by a photoresist supplier. All the same CIL trusts UDE and intends to go into a commercial venture with them. Regarding SiGe ADCs, UPb has not fully reached the desired sampling frequency and accuracy. Reasons for this are known and can be overcome (see below). Regarding CMOS signal processing, UPb has reached individual demultiplexer performance to a good degree, and full-custom CMOS signal processing at full speed, but their joint execution is limited by suboptimal chip mounting (see below). Beyond that, UPb has found an algorithm that allows transmitting synchronous 16-QAM and similar schemes also with standard DFB lasers, in contrast to current international efforts where external-cavity lasers are used. UPb has also extended its electronic polarization control for PMD compensation. In addition to the commercial success of Photline and CIL, UPb has won national research contracts for further investigation into synchronous QPSK transmission, has won an international contract for ADC delivery and is about to sign a contract for further ADC development. All have contributed to about 9 invited and a number of regular conference and journal publications as well as press releases with international reach.

Most partners have gathered in an – unfortunately declined – follow-up proposal “synQAM” with the targets of 100 GbE transmission and 16-QAM transmission with DFB lasers. We believe the project goals set up there continue to be valid and will try to submit another similar proposal in the future. Many of the mentioned possible improvements are also being undertaken, as far as resources permit, at own initiative and funded by national and international partners.

9 List of figures and tables