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1. Executive summary

The main objective of PLAT4M was to bring existing silicon photonics research foundries to a level of maturity high enough to enable a seamless transition to industry. These foundries addressed several applications fields, both for low volume manufacturing as well as for medium/high volume manufacturing. Three different but complementary platforms were set up in the time frame of the project:

- The imec R&D facility in Leuven, based on 200mm pilot line, enabling passives, detectors and modulators, with additional process modules optimized for sensing. The ISIPP25G technology was consolidated and several critical new functionalities were developed. The technology is accessible through PDK's available in IPKISS and Phoenix software. In collaboration with Mentor Graphics imec has also explored LVS verifications to reduce design errors and LFD to improve the patterning predictability.
- The CEA-LETI R&D facility in Grenoble, based on 200mm pilot line, on which passives, detectors, modulators and integrated lasers can be fabricated, with a focus on high bandwidth devices. A new silicon photonic platform based on a 310nm silicon film on top of an 800nm BOX on a high-resistivity silicon substrate was developed. Since the targeted applications for the project were O-band transceivers and receivers, most of the developed devices are suitable for 1310nm operations. CEA-LETI has developed 3 PDKs which are dedicated to Multi Project Wafers (MPW) runs on this silicon photonics technology which is now offered via the brokers CMP and Europractice.
- The ST-FR-CR2 industrial facility, based on 300mm industrial line, with passives, detectors and modulators. ST has developed the DAPHNE silicon photonics platform aimed at being an evolutionary R&D tool which generates and nurtures application specific production nodes. It is a multi-level silicon patterning (300nm, 150nm, 50nm, 0nm), a selective germanium epitaxial growth, a series of silicon and germanium implants and a back end of line consisting of 3 interconnection copper layers, 1 thick copper RF line and 1 thick Al RF & pad layer.

The consortium partners have worked closely together on an integrated electronics/photonics co-design workflow. This has been accomplished by building on existing tool-sets wherever possible and developing new technologies when required. Well known EDA solutions Pyxis and Calibre from Mentor Graphics have been improved and extended to 'understand' photonics. Interfaces have been developed between these tools and OptoDesigner from PhoeniX Software to create integrated design flows (re)using the best practices from both photonics and electronics design and finally more complete PDKs have been developed, incorporating new components, added models and fabrication information.

Packaging played a key role in the development of the project demonstrators. The skills and processes developed and refined during the various packaging tasks also advanced the development of the Silicon Photonic packaging toolkit. This toolkit establishes standardised packaging processes for optical fibres, active devices, electronic components and thermo-mechanical systems to ensure that PICs can be more easily packaged in a timely and cost-effective way. A design rule document has been prepared and made available through EuroPractice by Tyndall.

A 4×25G Transceiver chosen as a Telecom application for demonstration of LETI and ST platforms was demonstrated. The functionality of such a device are compatible with 100GBase-LR4 standard that means a transmission of signal over 4 WDM channels, spaced by 800 GHz around 1310 nm window, one fibre out and one fibre in.

Using the imec technology with new processing steps, TNO has demonstrated a multi-channel ring resonator based sensor system. Polytec demonstrated the operation of Multichannel Laser Doppler Vibrometer. THALES has demonstrated an integrated FMCW LiDAR system with 8 switchable output channels, enabling to scanning directions as well as a coherent beam combiner with 16 beams.

2. A summary description of project context and objectives

Context

Silicon photonics i.e. the way to mix the power of integrated photonics and CMOS technologies, has seen a tremendous increase in research output over the last years. This evolution is largely based on the vision that silicon as a mature integration platform can bring photonic integrated circuits to mass-market applications as it has done for electronic circuits, driven by the economy of scale of generic wafer-scale integration technologies. Huge progress has been made in silicon photonics, where a wide variety of high-performance passive and active electro-optical building blocks are now available. Silicon Photonics is presently mainly studied in the ICT world for datacenter interconnections, telecom infrastructure and consumer electronics interfaces but its potential is so strong that many other application areas will embrace and exploit the technology: these include environmental and bio-sensing, avionics as well as automotive.

In Europe, several research laboratories and universities have demonstrated a strong international leadership with both new scientific discoveries and excellent CMOS photonics R&D facilities, as well as establishing a leading Silicon photonics community where design capability, training sessions and multi-project wafer run are being established. This is in particular the case for imec and CEA-LETI, who have developed silicon photonics technology on 200mm SOI wafers in the frame of previous projects (PICMOS, PHOLOGIC, WADIMOS, HELIOS, ePIXnet…).

Most of the efforts have been devoted so far to the development of elementary photonic building blocks, but the fabrication of complete Photonic Integrated Circuit (PIC), i.e. combining tens of different components such as waveguides, lasers, photodetectors and modulators, had to overcome the a proof of concept stage. Various architectures have been investigated for each building block, each of them having its own pros and cons.

However the next step of denser integration and reliable fabrication is a crucial step to support the large potential markets which silicon photonics can address. For bringing the existing platforms to a level of maturity compatible with industrialization, it is now essential to put efforts on streamlining and stabilizing the design and process flows, by taking into account design robustness, process variability and process integration constraints. Reaching a maturity and yield level similar to microelectronics standards is mandatory for the adoption of silicon photonics technology by users and allows the introduction of standard design flows supported by advanced design environments. Moreover, a complete supply chain covering design, process and packaging must be created.

The European environment is very favourable to the development of this technology with a combination of excellent research laboratories, CMOS foundries already involved in the "More than Moore" field with top-level 200mm and 300mm facilities, optoelectronic components manufacturers, CAD-tools vendors and end-users for telecoms, datacoms or sensing applications. The goal was to reinforce European position in silicon photonics to prepare its massive adoption, by exploiting, at proper yield and quality, the large scale semiconductor manufacturing infrastructure and tools chain that would allow a commoditized use of the Silicon Photonics technology, as presently happens for traditional VLSI market.

Objectives

The main objective of PLAT4M was to bring existing silicon photonics research foundries to a level of maturity high enough to enable a seamless transition to industry. These foundries have addressed several applications fields, both for low volume manufacturing as well as for medium/high volume manufacturing. Three different but complementary platforms were set up in the frame of the project:

- The imec R&D facility in Leuven, based on 200mm pilot line, enabling passives, detectors and modulators, with additional process modules optimized for sensing.

- The CEA-LETI R&D facility in Grenoble, based on 200mm pilot line, on which passives, detectors, modulators and integrated lasers can be fabricated, with a focus on high bandwidth devices.
- The ST-FR-CR2 industrial facility, based on 300mm industrial line, with passives, detectors and modulators

Each of these platforms are generic in nature, in the sense that they support silicon photonics for a range of applications. Still, each platform has its particular strengths. This is not unlike electronics, where the basics principles of CMOS are generic, but platforms have evolved for different applications (low-power, high-voltage, high speed …).
A particular distinction is that imec and CEA-LETI run silicon photonics in an R&D environment, which enables flexibility, but where production bandwidth is limited to low-volume production.
Even though processing requirement for silicon photonics are different than for CMOS electronics, there is still an advantage in using state-of-the art technology. This is possible within this consortium, to ensure scalability for next technology generations, advanced processes such as immersion lithography and heterogeneous laser integration will be evaluated on the 300mm platform.

To achieve this there needs to be innovation on three fronts:

1. **Make technologies and tools mature:**
    - At design level, Process Design Kits (PDK) will be established for each platform, thus enabling the design of PIC by fabless users. The design environment will also enable Electrical-Optical co-design.
    - At process level, a reduced set of elementary building blocks will be stabilized on each platform. Much efforts will be devoted to process integration to improve the manufacturability (i.e. the ability to manufacture a circuit within specifications with relative ease at minimum cost and maximum reliability) of complex PICs
    - Testing procedures will be defined to have a common characterization methodology and to provide the required data for device modelling work
    - At packaging level, packaging processes that can be transferred to high volume manufacturing will be developed
2. **Validate each platform through application-driven test vehicles**:
    - Demonstrators representing various applications fields will be fabricated, thereby involving companies active in these application markets. Different complex PICs will be fabricated in order to validate the complete flow at different levels:
        - At design level, to validate the generic design flow
        - At process level, to validate the performance of elementary building blocks as well as their integration in circuits
        - At packaging level, to validate the photonic/electronic integration as well as the packaging concepts developed within the project.
3. **Prepare the next generation platform by assessing potential roads**
    - Advanced processes will be evaluated to ensure compatibility with future technology nodes as well as scalability for higher integration complexity
    - the performance boundaries of a generic platform will be explored to assess a roadmap for platform flavours development

The major outcome of PLAT4M will be the availability of a complete supply chain based on three technology platforms supported by a unified design environment:

- The CEA and the imec ones, well suited for prototyping and low volume manufacturing. Both provide generic building blocks as well as a small number of specific features, such as integrated laser on LETI platform.
- The ST-FR-CR2 one, well adapted to medium to high volume manufacturing, based on 300mm state of the art industrial line.

An important goal is establishing a full photonics design flow capable of handling more than 1000 components in a design environment used by typical CMOS designer, to be able to quickly introduce photonics into the CMOS world. As such this design flow should support mature design transfer from the research facilities into an industrial facility. A second target which relates to this is the shortening of a design cycle time from idea to mask tape-out. A typical design cycle for a relatively simple silicon photonic circuit takes about 4-6 months, with about 50/50 split between circuit design and validation/mask prep. An automated workflow and integrated simulation should at least reduce this by 50%, with a target of 2 months.

The elaboration of a fully integrated photonic sub-system without the laser source requires roughly 100 process steps whereas the average need to produce electronic ICs is a bit above 200 steps. Thus, we already estimate that the photonic platform must be able to handle a process flow which is at least equivalent to half that of a traditional CMOS fab. For an emerging technology, this is an integration challenge in terms of reliability and robustness of the process steps and of the control of their inter-related impact.

The innovative unified approach that will be developed by the partners will lead to significant breakthroughs in terms of design environment, process stability and modularity, and yield:

- In order to demonstrate the versatility of the platform it is the objective of this project to establish a modular integration flow that serves different applications using different modules but within a single design / fabrication cycle. For this, the project will demonstrate that at least two applications requiring different sets of modules can be served in a single “foundry” run.
- The project will demonstrate the silicon photonics platform by designing / fabricating complex photonics chips requiring between a few tens and a few hundred’s of components.
- The project will demonstrate that it is possible to co-integrate all required components with less than 10% performance degradation compared to the isolated device fabrication
- The project will demonstrate that it is possible to achieve a process control for a within-chip device matching. Device matching metric for photonics are different than for electronics. For wavelength filters we will attain spectral signature matching within a nanometer (without active tuning enabled). For active devices, such as modulators and photodetectors, we will measure device matching based on modulation efficiency, bandwidth, conversion efficiency and dark current, where we will allow no more than 5% uniformity.

The major outcome of PLAT4M will be the availability of a complete supply chain based of three technology platforms supported by a unified design environment:

- The CEA-LETI and the imec ones, well suited for prototyping and low volume manufacturing. Both provide generic building blocks as well as a small number of specific features, such as integrated laser on CEA-LETI platform.
- The ST-FR-CR2 one, well adapted to medium to high volume manufacturing, based on 300mm state of the art industrial line.

3. A description of the main S&T results/foregrounds

Development of the imec platform with associated pdk

Throughout the course of the PLAT4M Imec has consolidated its ISIPP25G technology and developed projects several critical new functionalities to further enhance the performance of its 200mm silicon photonics R&D platform. A platform performance tracking infrastructure was put in place to monitor the process stability of the technology against specifications by monitoring systematically the same dimensions and thicknesses on all process lots. This methodology enabled the monitoring of the process capability for each process module. In total more than 140 parameters are automatically tracked and monitored through the wafer processing. An example of such automatic process performance trendchart is given in Figure 1 for the important parameter of the top silicon layer thickness of the SOI wafers at the start of the process.

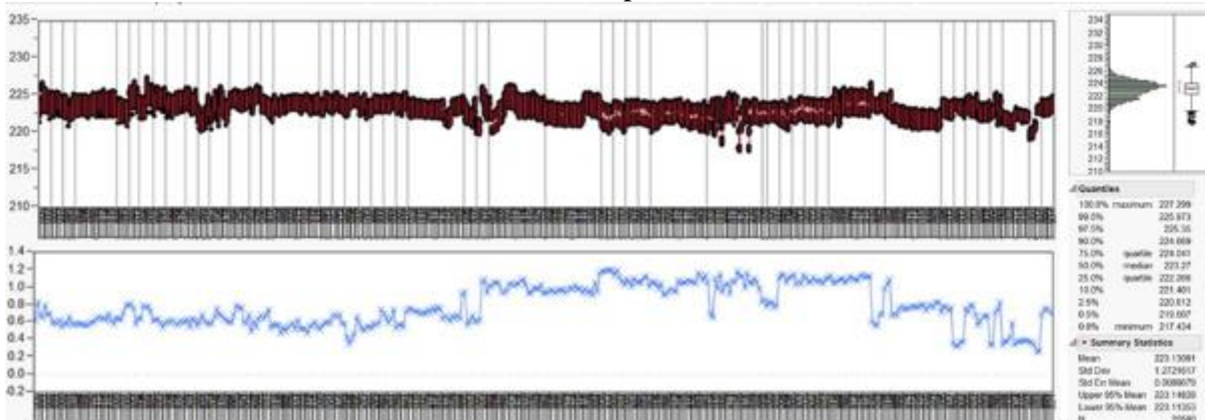

Figure 1. Example of process performance metrology trendchart: starting top silicon layer thickness of the SOI substrate at process start.

The devices performance is also tracked with end-of-line electrical, optical and electro-optical characterization at wafer scale. Each critical function layer is characterized to ensure that each module has the expected functionality (implanted layer and metal sheet resistance, diode capacitance and leakage, waveguide loss). Final each critical library component (modulator, detector, MMI's, couplers, splitters) is sampled at wafer scale and analysed with a systematic data extraction method.

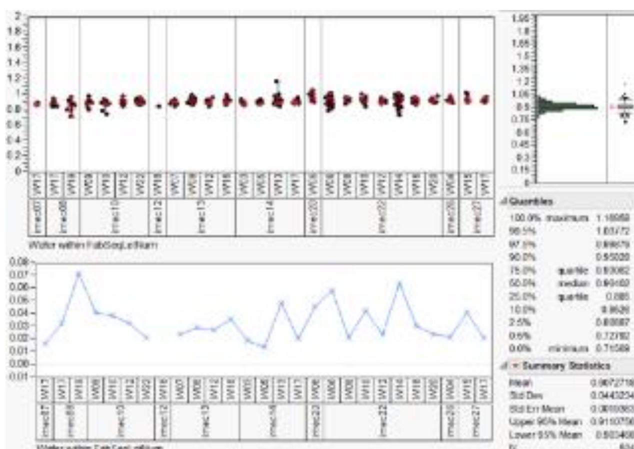

Figure 2. Example of the end-of-line optical device performance trendcharts: Vπ-Lπ of MZ modulators @0V, C-band in ISIPP25G technology

The wafer-scale characterization method was developed to ensure that the induced measurement error is significantly lower than the device performance variability. With this in-line and end-of-line monitoring infrastructure in place imec has also improved its process quality by eliminating process problems that caused variability, mostly for waveguide loss which now stable and <2dB/cm for the fully etched waveguide (median = 1.5dB/cm over 13 lots and 73 wafers measured).

Besides this maturity step-up effort, imec has also developed new critical modules to enable improved functionalities. A first module that locally undercuts the substrates, improves heater efficiency by a factor of 4. A second module allows the addition of a metal heater above the silicon waveguide that is a suitable alternative to the doped silicon heater for the very compact components such as microring resonators. Finally imec developed a module to re-open the BEOL dielectric stack and expose the silicon waveguide top surface for sensing application with minimal waveguide loss impact (<3dB/cm penalty). These modules are illustrated in Figure 3.

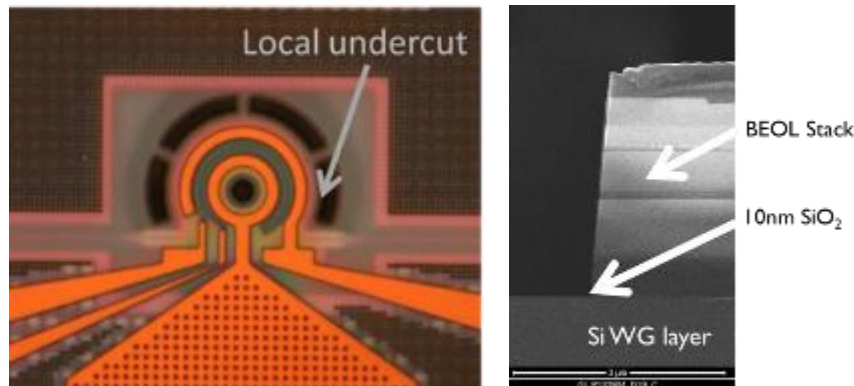

Figure 3. Illustration of the new modules introduced for enhanced functionalities: (left) local substrate removal (undercut) with metal heater for reduced thermal power consumption and (right) BEOL dielectric layers removal above the silicon waveguide layers for sensing applications.

The device designs have also improved, primarily for the depletion-based modulators with various design and doping options to realize application-specific insertion loss – efficiency – bandwidth trade-offs. Some passive components have been demonstrated for the first time (grating coupler - star coupler) or have been improved (~2dB TE grating coupler insertion loss after full integration).
With this mature technology imec together with its partners (Tyndall, TNO, Thales and Polytec) has completed successfully, within the four years of the PLAT4M project, three full prototype development iterations (application specific component and circuit design, fabrication, pre-assembly wafer & die test, packaging, module test) allowing systematic improvements from one iteration to the next.
Today's imec technology offer has evolved beyond what was used and developed in PLAT4M. It now contains:

- Low-loss waveguide based O-Band & C-Band passive library using 193nm lithography
- Edge and Surface Grating couplers (<3dB insertion loss)
- Three 50Gb/s modulator options (MZM, MRM, GeSi EAM)
- Five Germanium photodetectors options (25Gb/s to 100Gb/s data rates or high efficiency (>90%) monitor diode)
- Two level of Cu interconnect metals
- W metal heaters with local undercut

This technology now serves as the basis for new functionalities exploration and for industrial prototypes development. A subset of the technology called ISIPP50G is offered in Multi-Project Wafer service offered by EuroPractice

- http://www.europractice-ic.com/SiPhotonics_technology_imec_ISIPP50G.php
- http://www.imec-int.com/en/integrated-silicon-photonics).

The technology is accessible through PDK's available in IPKISS and Phoenix software (Figure 4). In collaboration with Mentor Graphics imec has also explored LVS verifications to reduce design errors and LFD to improve the patterning predictability. These features are expected to be added in future versions of the PDK.

Figure 4. Imec ISIPP50G PDK.

The future evolution of the platform will be towards improve passive functions (reduced loss, reduced variabilities, reduced dimensions, reduced thermal dependencies) and active functions (III-V like performances). As a first step in this direction, imec has explored within the project the potential of using immersion lithography and 300mm wafer processing to improve significantly the propagation loss of fully etched single mode Si waveguides as low as 0.6dB/cm (Figure 5) which was the state-of-the-art at the time of publication (2013). Another benefit of more advanced processing tools was realized with the within-wafer waveguide width control 30% to 40% improvement compared to the 200mm processing.

Figure 5. Ultra-low loss single mode 220nmx450nm silicon waveguide using 300mm processing, including immersion lithography.

Development of the CEA-LETI platform with associated pdk

CEA-LETI has specifically developed a new silicon photonic platform in the frame of PLAT4M project. Wafers are fabricated in a fully CMOS compatible 200mm fabrication line at CEA-LETI. Starting materials are SOI substrates featuring a 310nm silicon film on top of an 800nm BOX on a high-resistivity silicon substrate. A modular approach is used to build the process flow that supports various sets of devices.

Figure 6: Schematic cross-section of CEA 200mm silicon photonic platform

The simplest process flow is a passive device-only technology, whereas the full process includes active devices such as photodiodes, modulators as well as tuning capability using a thermal heater option. A 2 metal interconnect level BEOL is also supported. Process flexibility allows device tuning with respect to the application needs.

Since the targeted applications for the project were O-band transceivers and receivers, most of the developed devices are suitable for 1310nm operations. An extensive set of passive devices has been developed and is now available.

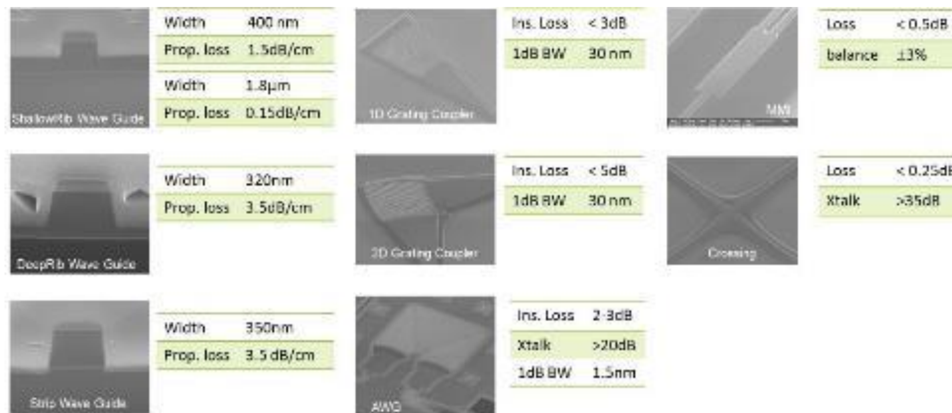

Figure 7. Some basic passive devices with their main characteristics.

Photodiode has been integrated for the first time in CEA-LETI new platform developed for PLAT4M project. Two kind of architectures have been evaluated: a conventional full Ge diode and a SiGeSi heterojunction device. In both case, Germanium is used to form the butt-coupled PIN photo diode active area. Ge selective epitaxy is realized within a silicon-etched cavity. Conventional devices use n-type and p-type implantations into the germanium layer leading to a full-Ge device whereas, these implantations are made into the silicon for the SiGeSi diode thanks to a width reduction of the Ge cavity. The final device features a double Si/Ge/Si heterojunction. In this case, the implantations can be shared with the modulator which enable only one additional mask to form the photodiode instead of three for the conventional device. Another advantage of the Si/Ge/Si structure is the use of the silicide area for the device contact leading to better access resistance, which is difficult to achieve with a full Ge device. The Figure 8 presents cross-section schematics and FIB SEM pictures of both architecture.

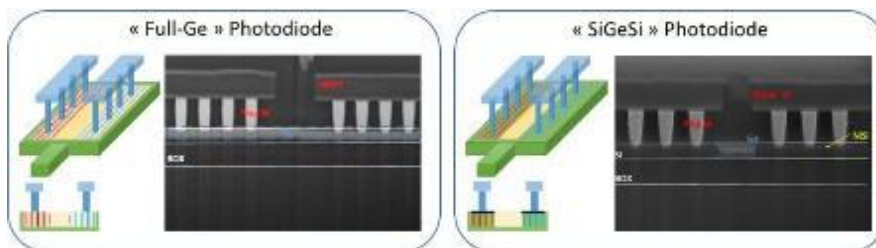

Figure 8: Full-Ge and SiGeSi photodiode Fib SEM cross-sections and schematics

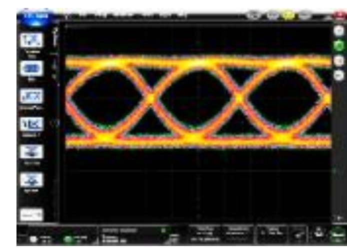

Figure 9: 1µm width Germanium photodiode eye diagram at 30Gb/s

For both device, the responsivity is larger than 0.8A/W (slightly better for SiGeSi photodiode), dark current is less than 10nA @-1V which is very low and indicated the low defect density of the Ge epitaxial layer. O/E bandwidth of a 1µm width device is larger than 20 GHz at 1310nm wavelength which is sufficient for 25 Gb/s operation. Finally the Figure 9 shows a reception test of a 1µm width device modulated by a NRZ signal at 30 Gb/s with a perfectly opened eye.
Traveling-wave modulators have been fabricated using CEA-LETI platform. In order to find the optimal design, different MZM parameters have been tested: two waveguide types (standard rib waveguide and deep rib) and four junction doping types (interdigitated or continuous and standard or counter-doping). In total, 8 different types of MZM were designed and fabricated in three different

lengths (2mm, 3mm and 4mm). Finally, by sweeping the doping levels of the junction, we have come to an optimized FOM [Vpi.Lpi x IL] of 12.5dB.V for the best doping level and configuration and for the best waveguide type. The corresponding average Vpi.Lpi and IL are 1.9V.cm and 6.5dB/cm respectively. The RF bandwidth for the best modulator type and found around 35GHz for a 2mm long MZM, 28GHz for 3mm and 25GHz for 4mm. For NRZ modulation, an extinction ration around 10dB was obtained with -4V reverse bias (the bias was slightly increased to improve the RF bandwidth of the MZM). An open eye is obtained without needing any pre or post signal distortion. For PAM4, also an open eye is obtained but only after applying some de-emphasis on the transmitter side.

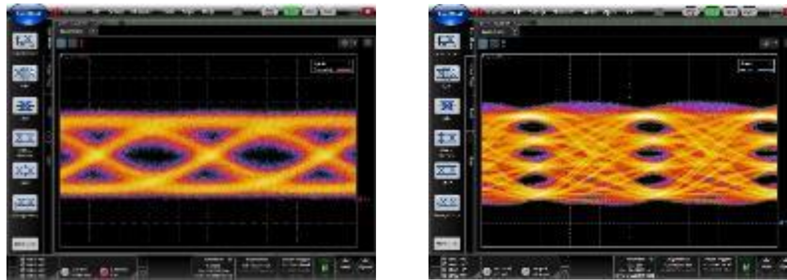

Figure 10: Left: 52Gbps NRZ eye diagram; Right: 28GBaud PAM4 eye (after CTLE 4dB applied and using de-emphasis on the TX side)

At the end of PLAT4M, all the main devices and process modules needed to design advanced photonic circuit at 1310 nm are available. EDA support of the device library will be described in the next section. Platform evolution roadmap exists in order to enlarge the device offer.

For internal purpose, CEA-LETI design tools are mainly based on the Cadence Virtuoso platform for schematic and layout. Mentor Graphics tools are used for all verification steps in the photonic design flow. This choice is based on the necessity of using maturity and experience of the Electronic Design Automation (EDA) tools. Since a few years, those companies have made some relevant progress by their own or by teaming up with other photonic software players like Lumerical or PhoeniX Software. They are now able to offer a new release of their tools to tackle photonic design constraints. Phoenix software is still widely used and appreciated by component designers. This PDK contains a complete set of devices with varying levels of maturity and their layout and model parameters range are unrestricted for internal purpose. The sketch here after presents the updated CEA-LETI Photonic Design Flow with each tools version for each step

Figure 11: CEA-LETI photonic design flow

In addition to this internal PDK, CEA-LETI has developed 3 others PDKs which are dedicated to Multi Project Wafers (MPW) runs on silicon photonics technology. A new partnership with the broker CMP widens the dissemination of this PDK, while the PDK for CEA-LETI photonic passive technology is still distributed by Europractice to another audience for the same MPW runs.

The first of these 3 PDKs is Cadence based and is aligned to our internal PDK in terms of design tools but the device set (building block and model) provided is slightly circumscribed in order to ensure more robustness and reliability.
The second one is the result of a fruitful collaboration with Mentor Graphics to set up a new PDK based exclusively on their CAD tools: Pyxis, Calibre and Eldo. This development will be covered in section “**Erreur ! Source du renvoi introuvable.**”.
The final one is a result of a collaboration with Phoenix Software in order to update and expand the existing PDK version with the latest characterisation silicon results and new devices. From our latest MPW run, Phoenix PDK was the most asked by academic or research customers.
CEA-LETI is also offering a 3D compatible post-process technology through our new broker. 3D packaging allows optical interconnect closer to the electronic chip. The benefits are many:

- Stacking electronic/photonic circuits
- Photonic interposer
- Network on Chip
- High density Photonic/electronic circuit

The flyer of MPW run for CEA-LETI photonic technology is widely disseminated by CMP.

Figure 12: CMP flyer for MPW CEA-LETI Photonic technology

CEA LETI platform will be enhanced with the addition of a full device offer for C-band applications. It will be supported by a dedicated library in the PDK future releases.

Other optional modules will be developed and stabilized:

- SiN optional layer with vertical coupling on top of the SOI
- Amorphous silicon routing layer for 3D photonic integration
- Edge coupling for large band application

One main task that III-V Lab has performed is the reliability study of hybrid III-V/Si lasers. More than 15 hybrid III-V on silicon lasers have been selected, mounted and tested. Among those lasers, 5 lasers have suffered from thermal shock (air to air) by increasing the temperature from 0°C to 100°C during15min with 50 cycles, and then under dry heat at 175 C during 500 hours. No degradation was observed on the laser performance. Other lasers have been tested under 150 mA at 70°C for more than 5000 hours. Less than 5% of variation on threshold current and on the output power level is observed on those lasers. However, the junction voltage showed an increase of 20% after 5000 hours. Investigation is ongoing, in order to understand the mechanisms behind this phenomenon.

In collaboration with CEA, III-V Lab has designed, fabricated and characterized integrated hybrid III-V/Si DFB laser, electro-absorption modulator (EAM) and semiconductor optical amplifier (SOA) chip operating at the wavelength window at 1.3 µm. This device structure is show in Figure 13.

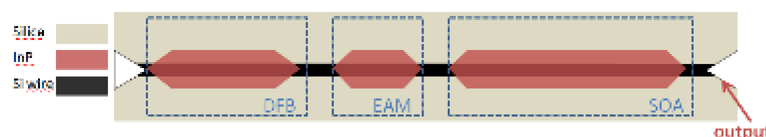

Figure 13. A schematic of the hybrid III-V / SOI ILM (Integrated Laser Modulator): the white triangles represent the VC

The DFB laser operates on a single mode at 1320nm with side-mode-suppression-ratio >45dB. The static extinction ratio of the EAM is 15dB for a voltage varying from 0 to -2 V. Figure below shows the BER and the eye diagrams at 10 G (left) and 25 G (right). One can observe that the extinction ratio stays above 9dB for both 10 G and 25 G. At the BER level of 10^{-3}, the penalty is less than 1.5 dB at 10 G for transmission distance up to 50 km, and less than 0.5 dB at 25 G for transmission distance up to 25 km. Those are the state of the art results for the heterogeneeous III-V/Si devices.

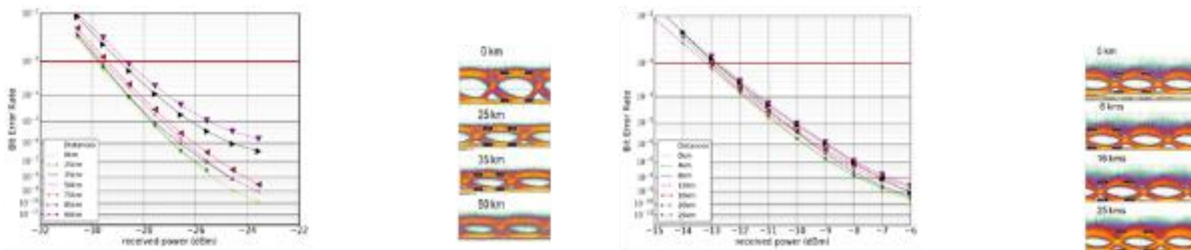

Figure 14. BER and eye diagram at 10Gb/s (left) and 25Gb/s(right)

In parallel of these new developments, a progressive migration of the photonic platform on 300mm Fab line will be initiated in 2017. The first step will be the fabrication of the entire O-Band and C-band passive device library in Q3 2017. The active devices, including the hybrid integrated laser, will be demonstrated in the first part of 2018.

Development of the ST platform with associated pdk

In the course of PLAT4M-FP7 project, ST has developed the DAPHNE silicon photonics platform in its 300mm wafer foundry. The technology is aimed at being an evolutionary R&D tool which generates and nurtures application specific production nodes. New process building blocks and devices are first evaluated in DAPHNE and then transferred in a technology if the feasibility study reveals successful. Consequently, more flexibility is available in DAPHNE for R&D without affecting the standard procedures applied during the qualification and maturity ramp up of a production flow.

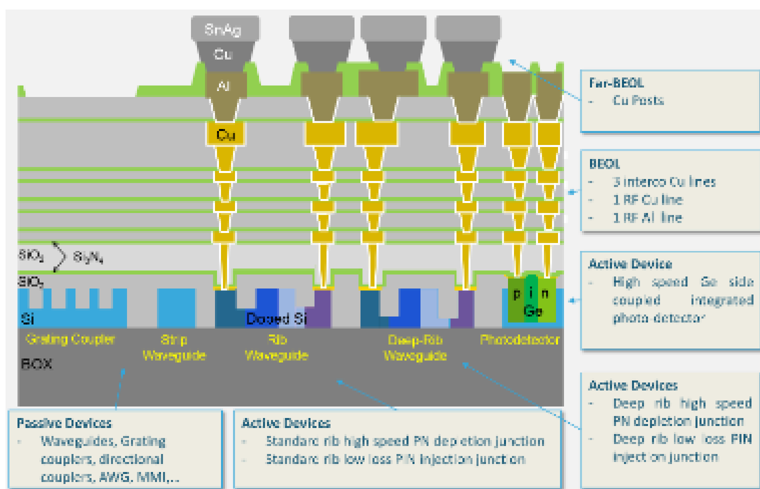

Figure 15: Schematics of a typical photonics IC (PIC).

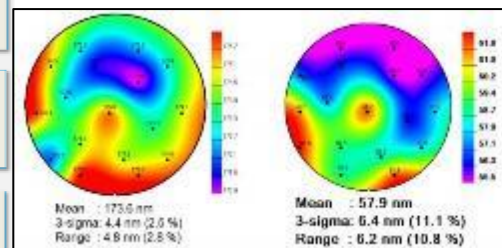

Figure 16: Wafer-level mapping of partially etched silicon uniformity.

The base offer accessible in DAPHNE is a multi-level silicon patterning (300nm, 150nm, 50nm, 0nm), a selective germanium epitaxial growth, a series of silicon and germanium implants and a back end of line consisting of 3 interconnection copper layers, 1 thick copper RF line and 1 thick Al RF & pad layer (Figure 15).

The PIC fabrication process uses state-of-the-art tools which guarantee a partially etched silicon uniformity range of 4.8nm for the 150nm slab and 6.2nm for the 50nm slab. Since the base wafer has a SOI non-uniformity of about 2nm, the additional range due to partial etch is consequently very low. Besides having access to a library of essential device cells for data-communication applications, designers can also include in circuits the layout of custom engineered devices. We have a robust layout verification flow which ensures that both the mask fabrication and silicon processing won't be affected by the inclusion of designs which are not qualified (Figure 17).

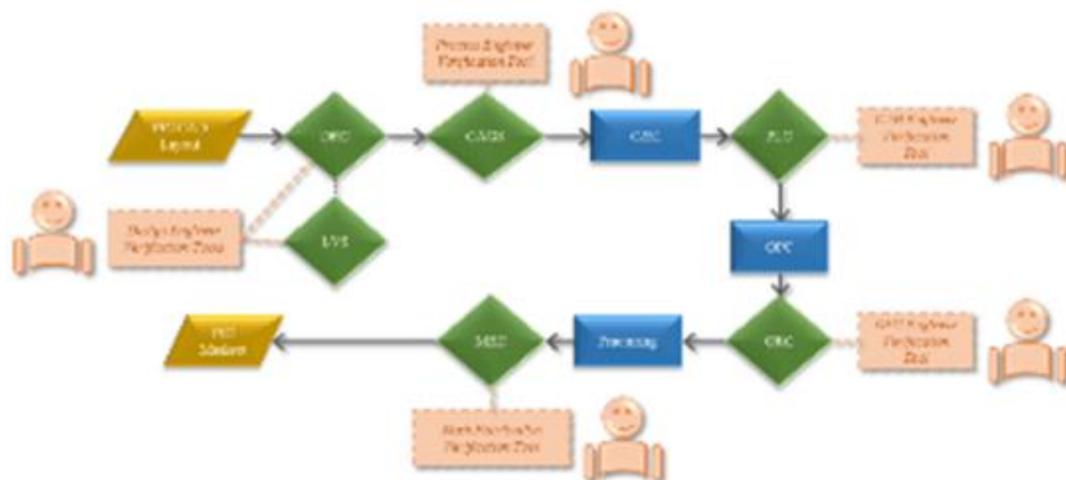

Figure 17. Layout and verification flow during tape-out for mask fabrication.

The flow is built up using standard CMOS foundry verification tools which are adapted to silicon photonics device verification. The objective is to make feasible the study of new devices while using a robust and frozen fabrication process flow. Statistical analysis of device robustness and reliability is thus feasible. In parallel and within the same technology, process evaluations can be launched on short-loops which affect neither the production flows nor the advanced device studies.

An example of passive device analysis done using DAPHNE is the development of Mux/Demux solutions for the 100GBase-LR4 standard. Two options were explored in parallel: AWGs and cascaded MZI. Both approaches have their respective pros and cons. Typically, an advantage of the AWG is its process and temperature stability. However, an AWG tends to experience higher insertion losses. The cascaded MZI on the other hand undergoes less transmission losses but is usually not stable with respect to environmental temperature fluctuations. Both devices were developed and benchmark and, indeed, we obtain a nice transmission spectrum for the AWG when no band flattening is applied (Figure 18). The insertion loss is of about 1.2dB. However, the AWG devices which are designed with larger optical bands have at least 2dB more losses.

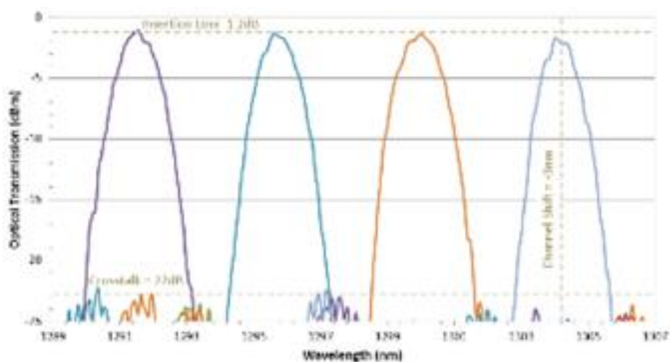

Figure 18. Transmission spectrum of an AWG

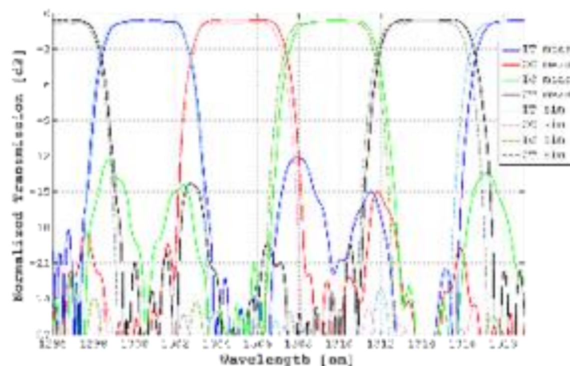

Figure 19. Transmission spectrum of a cascaded-MZI.

On the other hand, we developed a cascaded MZI with a channel width of 2.1nm and the optical transmission characterization results revealed losses of < 2dB (Figure 19). Thus, depending on the chosen system assembly, either solution could be used. Typically, in the 100GBase-LR4 transceiver demonstrator of PLAT4M, a temperature stabilization and control system is available at package level. Consequently, the cascaded MZI would perfectly fit that demonstrator.

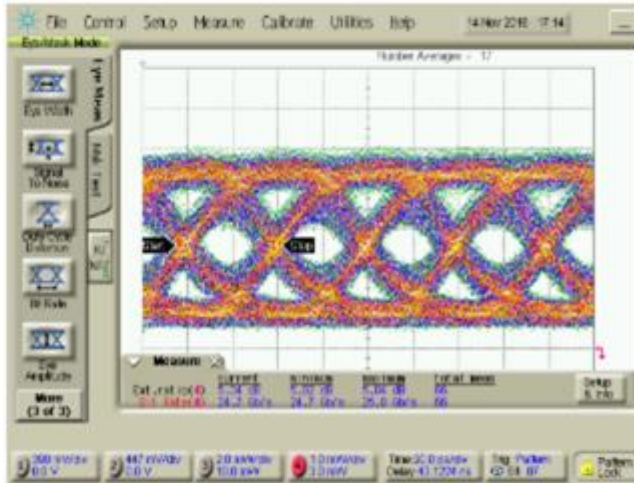

Figure 20. Eye diagram of a 25Gbps channel transmission.

Finally, a few active devices were explored for signal modulation and detection. Various pn-junctions in Mach-Zehnder circuits were benchmarked in silicon for signal modulation @ 25Gbps and several pin junctions were evaluated in germanium photodiodes for signal detection. A typical eye diagram of a 1mm long pn-junction placed in a push-pull Mach Zehnder configuration is shown in

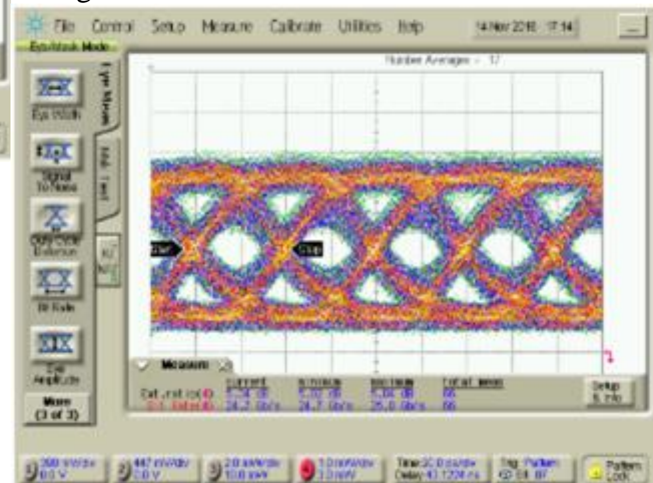

Figure 20. So in conclusion, the devices present in DAPHNE and fabricated in the process flow can result in various Datacom demonstrators.

Tools for design and maskset

Within PLAT4M the consortium partners have worked closely together on an integrated electronics/photonics co-design workflow, filling an important gap in the design software landscape. This has been accomplished by building on existing tool-sets wherever possible and developing new technologies when required. Well known EDA solutions Pyxis and Calibre from Mentor Graphics have been improved and extended to ‘understand’ photonics. Interfaces have been developed between these tools and OptoDesigner from PhoeniX Software to create integrated design flows (re)using the best practices from both photonics and electronics design and finally more complete PDKs have been developed, incorporating new components, added models and fabrication information.

The Pyxis Custom Design Platform from Mentor Graphics is a complete environment for creating custom ICs, 3D ICs, MEMS, TFTs (Thin Film Displays) and silicon photonics. The platform includes solutions for both design creation and implementation as well as interfaces to Mentor’s industry-

leading simulation and verification solutions (including: Questa ADMS, ELDO Premier, ADiT, and Calibre).

With Pyxis Schematic, users can create a schematic that contains both device and language model (SPICE, HDL) descriptions, this information can be used to drive the simulation environment (including dedicated photonics simulations) for design validation. Once the design is complete and verified at the device level, one can start the physical implementation of the design.
With the Pyxis Layout suite, users can create the physical mask layout implementation. The suite provides a single source solution for floor planning, editing, schematic-driven layout, chip assemble, and custom routing. On completion of the physical design, it can be seamlessly exported to the Calibre Suite for verification and sign-off. Most important for silicon photonics is the fact that Pyxis is not limited and provides true all-angle layout capabilities. Mentor Graphics worked together with both IMEC and CEA-LETI PDK teams to release a Pyxis compatible PDK and are currently in the process of maturing it.
Further the Pyxis team has also collaborated with PhoeniX Software to develop an enhanced/dedicated Si-Photonic design environment. This methodology has been called the “unified flow”, enabling EDA and PDA tools to seemingly communicate together. Hence the end goal for the user would be to call the OptoDesigner engines from the Pyxis environment in order to directly leverage PhoeniX Sofware’s Si-Photonic design features.

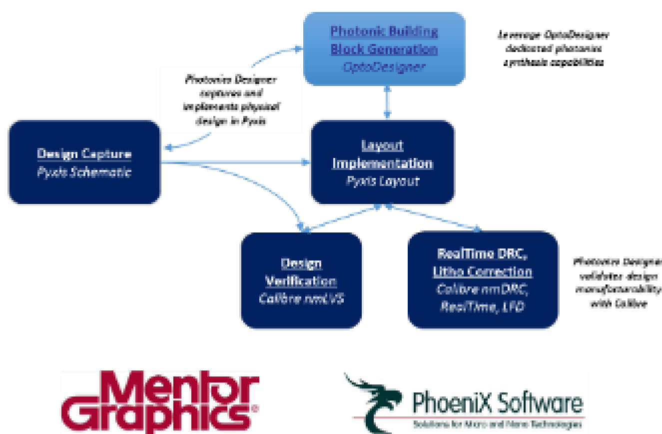

Figure 21. Pyxis Schematic screenshots

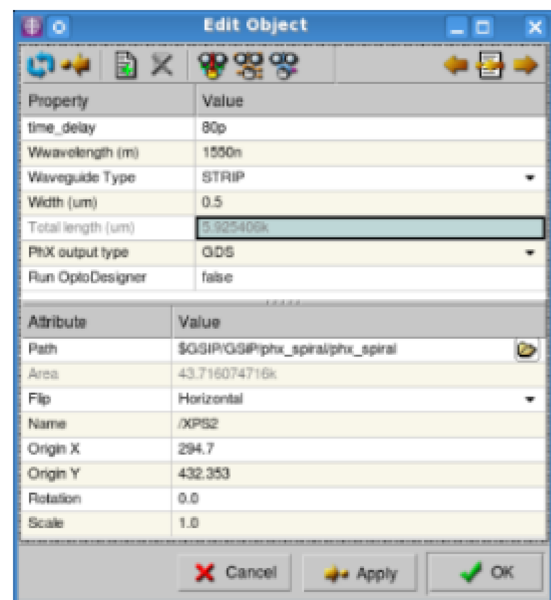

Figure 22: Parameter dialogue driving the layout generation.

Figure 23. Pyxis Layout screenshots, including the phx_spiral example

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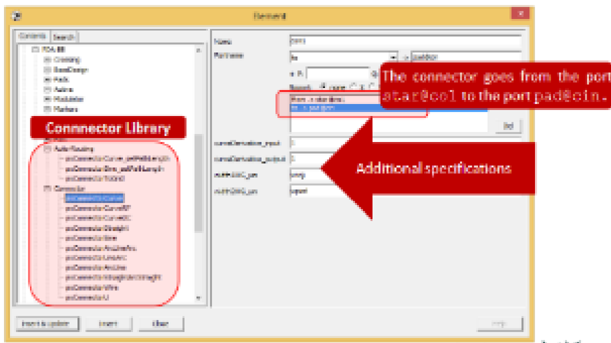
OptoDesigner is PhoeniX Software's market leading photonic integrated circuit chip design solution providing a flexible and integrated toolset that offers best-in-class control without compromising creativity. It covers the complete design flow, from integrated photonics simulations, process visualization to mask layout. Moreover, OptoDesigner incorporates Process Design Kit (PDK) plugin's, providing access to leading photonic integration platforms (InP, silicon photonics and TriPleX) at most of the integrated photonics foundries offering designers the opportunity of exploring the full technology and market potential of their product ideas. In this project PhoeniX Software has been working together with the Pyxis team at Mentor Graphics to interface its tool to enable advanced photonic component layout generation and waveguide routing. In addition PhoeniX Software has been working with PSUD to incorporate compact models of silicon photonics modulators into its environment. Finally, work has been done with imec, CEA-LETI, ST and Tyndall to develop and provide PDKs, packaging templates and advanced photonic building block design tools.

Waveguide routing and Photonic Building Blocks

In contrary to most electronic chip designs, the interconnections in photonic ICs have to be considered a device with a function instead of just a connection. Many functions in photonic components are created by playing with geometries and phase relations. To automate the implementation of waveguide connections, PhoeniX Software has developed a whole family of generic connectors. Connectors do what their name implies: they connect two ports in a design to each other. The designer can enter any ports: the right connection is then generated automatically. The user does not need to bother about the coordinates of the ports these may even be unknown. The designer often has extra requirements for the connector, like a minimum bend radius, or a specific optical path length.



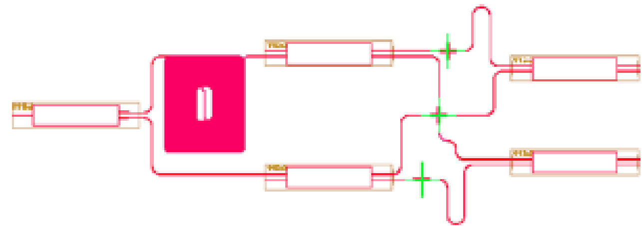


Figure 24. 90 degree hybrid, including 1-symbol delay

A simple example of a Photonic Building Block is a spiral that acts as a delay-line, however the actual implementation of such a spiral is a combination of waveguide elements: straights, bends, couplers etc. These are heavily dependent on the actual wavelength (frequency) of the signal and the fabrication technology and cannot therefore be hardcoded as P-cell. The core technology within OptoDesigner ("Photonic Synthesis") has been further developed and utilized to create a whole family of generic photonic building blocks and advanced waveguide connectors and routing capability. The Figure 24 illustrates this with a, so called, 90 degree hybrid. Purpose is to measure the phase difference between two optical signals to reconstruct complex phase modulated signals used in optical transceivers. The interconnecting waveguides need to be defined very accurately to create a 90 degree phase-shift in one of the arms to obtain the correct behaviour. The constrained connectors as implemented in the OptoDesigner environment take care of this automatically, by taking designers intent, reading PDK information and synthesising a correct by construction layout.

In addition to these activities PhoeniX Software has been working on enhancing process variability analysis and yield estimation simulations. For this purpose the circuit simulation software package Aspic, developed by Filarete and commercialized by PhoeniX Software, has been utilized. Its methods for parameter sensitivity analysis are very advanced. Aspic allows a designer to use variables in a design - for example, the waveguide width and height - that are 'fuzzy': they have a statistical distribution around a nominal value. Then, Monte-Carlo techniques, together with advanced Bayesian statistical analysis, enables direct calculation of yield - how many of the, say, 1000 samples that are created will satisfy certain given quality checks - as well as figures that indicate the importance of the variance on each variable on the yield. This helps designers quickly to estimate circuit yields, given fabrication variations and enables process engineers to focus on improvements that will really impact manufacturing yield.

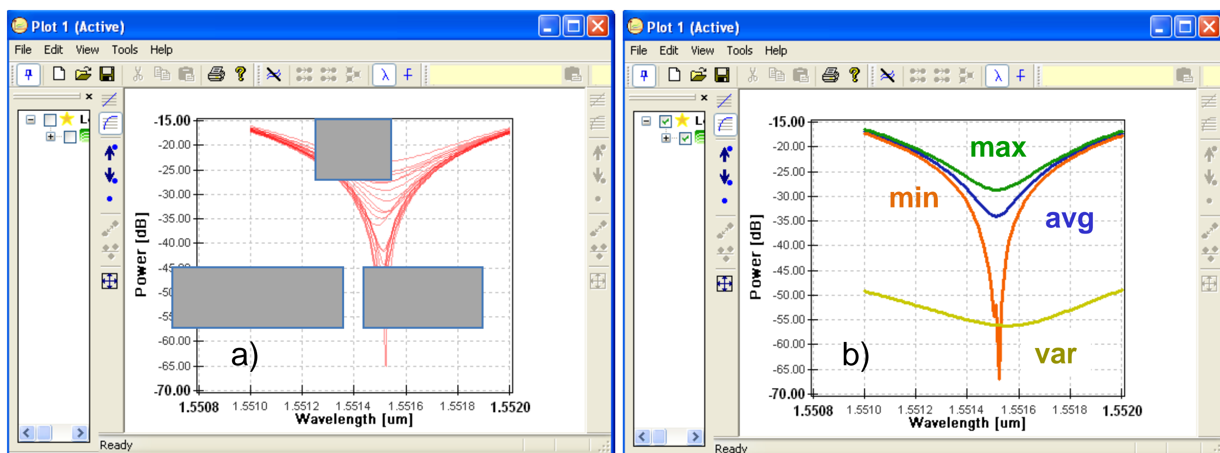


Figure 25. Monte-Carlo simulation of the notch of a Mach-Zehnder. b) Maximum, minimum, average and standard deviation of the output intensity. The grey areas define the " Mask" for the yield estimation.

For more than a decade now Calibre has been the EDA dominant tool for signoff verification. All major CMOS foundries are offering Calibre decks and are considering Calibre are their "golden" signoff verification tool. The objective of this PLAT4M project for Calibre was to be more exposed to Si-Photonic specific challenges and to verify that the tool capabilities could address them. For that purpose Mentor Graphics hired a phD student to study these specific verification flows.

Physical Verification tools (DRC/LVS)

Performing DRC on a Si-Photonic design is significantly different than performing it on a CMOS design: it contains mainly curvilinear shapes. While traditional DRC coding styles might have issue with this. Mentor demonstrated that by leveraging "equation based DRC" (eqDRC), a satisfactory results can be achieved: the number of false errors will be reduced to the minimum. In the D210 deliverable were described these various solutions based on eqDRC :

- Conditional DRC result Post-Filtering

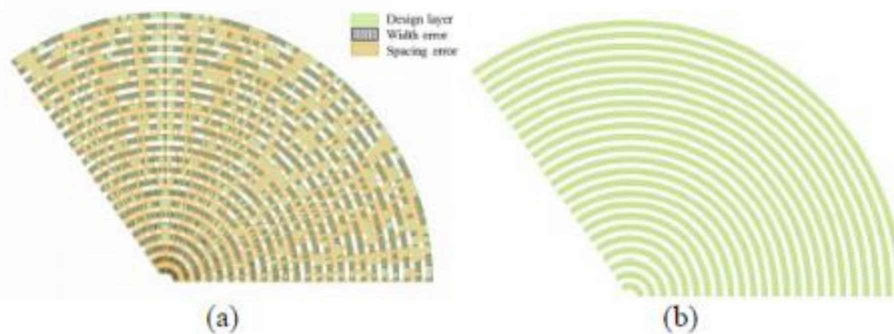


Figure 26. (a) Layout design of concentric arcs with false DRC width and spacing violations highlighted (courtesy Imec); (b) False errors filtered by eqDRC.

- Multi-Dimensional Rule Check

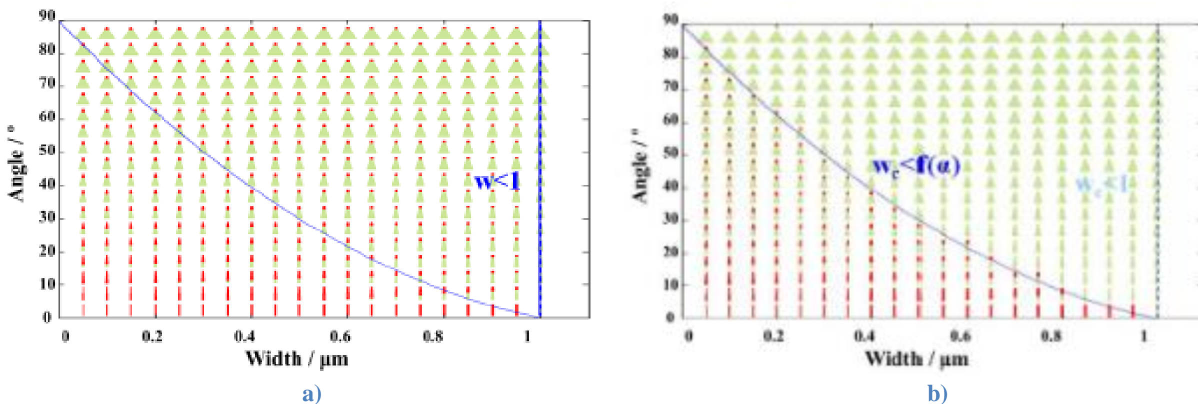


Figure 27. Layout trapezoid-like test structures arranged in a 2D array, placed with its width and angle value as coordinates. DRC results are highlighted in red, given by (a) traditional single-dimensional DRC rule; and (b) Multi-dimensional DRC rule integrated

- Enable measurement on Non-Conventional dimensions : curve lenght/radius checking

On the LVS (Layout versus Schematic) side, several approached have been considered: the traditional one based on marker layers enabling the device recognition. This approach is currently under development in the LETI PDK. Another R&D approach that Mentor introduced was a "Marker-less" methodology involving Calibre PERC.

Calibre PERC is a Tcl-based tool originally used for programmable ERC and electrostatic discharge (ESD) checking in IC designs by analyzing the source and layout netlist. With the extension of the LDL flow, PERC can perform layout geometry measurement and checks based on topology selection and filtering. The verification flow starts with a classical LVS comparison, where the circuit topology is validated. If the classical LVS passes, the PERC-LDL flow is invoked to perform the source and layout analysis, the described curvilinear feature computation, and parameter validation. The key database interfaced with the tools is the DFM database, where various source and layout elements are stored and manipulated by the PERC-LDL.

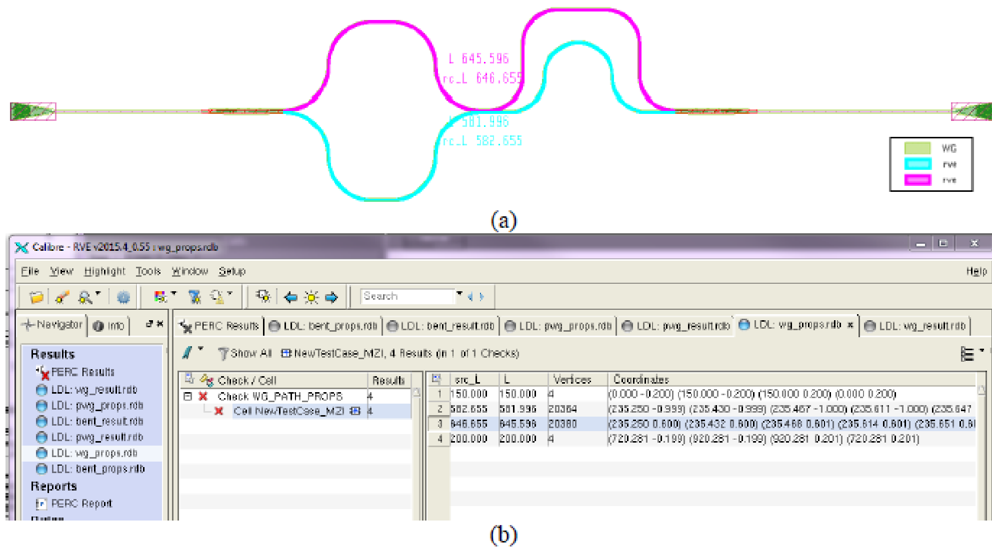


Figure 28. (a) Layout design of an Mach-Zehnder Interferometer (MZI) circuit. The two MZI arms are highlighted (rve layer) and annotated with computed properties. (b) The Calibre RVE result viewing environment which displays the measurement results from the MZI c

Design For Manufacturing (SmartFill/LFD/OPC)

- Regarding Fill strategies: To optimize, stabilize and improve our Silicon Photonic platform, CEA-LETI have developed in collaboration with Mentor Graphics a new way to address the tiling generation. By using Calibre® YieldEnhancer's SmartFill capabilities, the tiling generation are now controlled by optimizer function to get a result aligned with density constraints.

FE DUMMIES
BE DUMMIES
Dummy fill
SmartFill result

Figure 29. Difference between Dummy Fill and SmartFill results

Calibre® LFD™ (Litho Friendly Design) is the first production-proven EDA tool to address the urgent issue of how to manage lithographic process variability in the early stages of design creation. Calibre LFD accurately models the impact of lithographic processes on “as-drawn” layout data to determine the actual “as-manufactured” dimensions of fabricated gates and metal interconnects. By accurately simulating the effects of the lithographic process on “as-manufactured” layout geometry, the Calibre LFD tool enables designers to make trade-off decisions early, resulting in a design that is more robust and less sensitive to the lithographic process window.
Mentor and IMEC have collaborated to create a first Calibre LFD (Litho Friendly Design) Kit version that can be used to experiment it on various design and potentially detect design weaknesses from a manufacturability.

Regarding Optical Proximity Correction (OPC): Various OPC flows have been evaluated @ST based on Calibre OPCPro, nmOPC and pxOPC. Following this, a complete methodology have been described in D209 showing promising results and demonstrating that OPC will soon become a mandatory step for Si-Photonic design in order to improve overall circuit yield and performance. It will also prevent fabs from doing too many DOEs (Design of Experiment) which can become very expensive in terms of Silicon area/development time.

Paris-Sud University has worked on the development of models for silicon modulators. As a main result, a modulator simplified model has been developed, that enables a substantial reduction on computation effort in the analysis and design of modulators. The model is summarized in Figure 30. The complete physical analysis of a modulator is shown in (a), whereas the simplified model developed by Paris-Sud University is in (b). In terms of computational effort, the simplified model exhibits one order of magnitude reduction for a modulator based on a lateral PN junction. Moreover the reduction grows up to two order of magnitude in modulators based on interdigitated junctions.

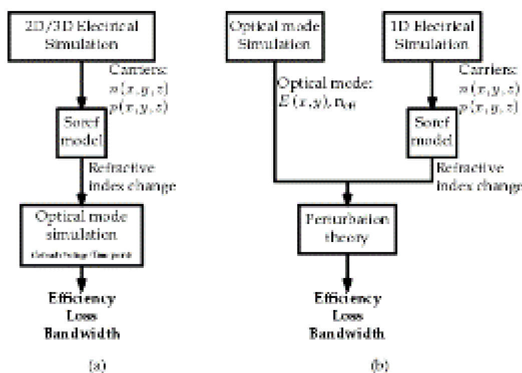


Figure 30. Modelling of silicon modulators.

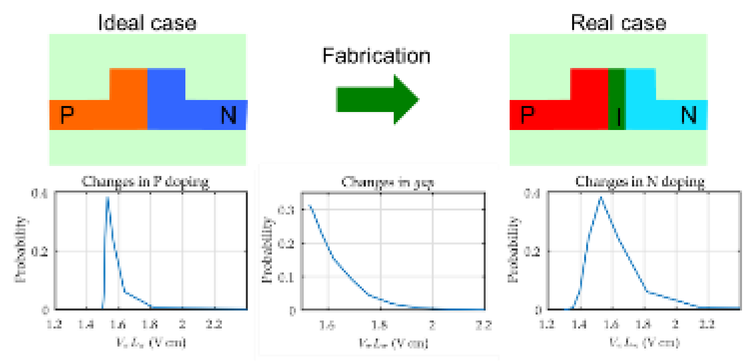


Figure 31. Influence of fabrication parameters in modulator efficiency

Paris-Sud University has used this model to provide four different modulators designs based on four different specifications (high-speed, low-loss, high-efficiency and ultra-high-efficiency). Furthermore, the simplified model has been leverage to evaluate the influence of fabrication deviations on the overall modulator performances, an example of Figure 31 shows the calculated probability density function of the efficiency when changes in doping and mask mismatch occur. This model is currently being implemented in Optodesigner from Phoenix software.

Tools for packaging

In PLAT4M, packaging played a key role in the development of the project demonstrators in WP6 and WP7. While the packaging of the demonstrators was vital in enabling project partners to test their device designs, the skills and processes developed and refined during the various packaging tasks

also advanced the development of the Silicon Photonic packaging toolkit. This toolkit establishes standardised packaging processes for optical fibres, active devices, electronic components and thermo-mechanical systems. A significant part of this toolkit is the design rules developed during the project. These design rules are used by device designers to ensure their PICs can be more easily packaged in a timely and cost-effective way; which is crucial for making silicon photonic packaging more accessible. A detailed design rule document has been prepared and made available through EuroPractice, outlining essential rules which must be followed to facilitate effective packaging. These design rules cover a number of fundamental areas of photonics packaging and some examples will be discussed in the following pages. A detailed design rule document is available at http://www.europractice-ic.com/docs/EuroPractice%20DOCUMENT%20V1%203%20PDF.pdf.

Design rules

Fibre-to-grating coupling

Grating coupling allows more relaxed alignment tolerances in comparison to edge coupling to single mode silicon waveguides. Typically ±2.5 µm of misalignment results in approximately a 1dB reduction in coupling efficiency. The angle of incidence (AOI) which light is launched into the grating coupler is critical. A deviation from the designed AOI of the grating-coupler causes a shift in the coupling spectrum away from target-wavelength by approximately 10nm per degree. As Tyndall uses index matched epoxy this impacts on the AOI compared to probing the chip with fibre-air and air-TOX interfaces. Therefore it is vital that designers take this into account when designing grating couplers.

To enable the active alignment process, which is carried out when coupling fibres or fibre arrays to grating couplers, it is essential that chip designers include a shunt waveguide on their Si-PICs. Coupling to an array of waveguides is best achieved using this additional shunt waveguide which are actively monitored during the fibre alignment process. For example an 8-channel waveguide system has two additional outer shunt waveguides as shown in Figure 32. It is also essential that grating couplers are designed with a pitch of either 127µm or 250 µm and that this information is communicated prior to packaging.

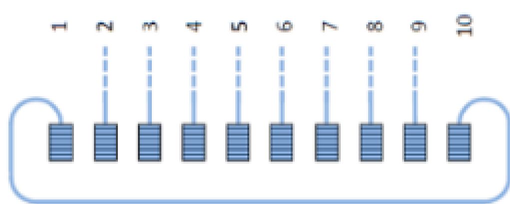


Figure 32: Array of grating couplers with shunt waveguide

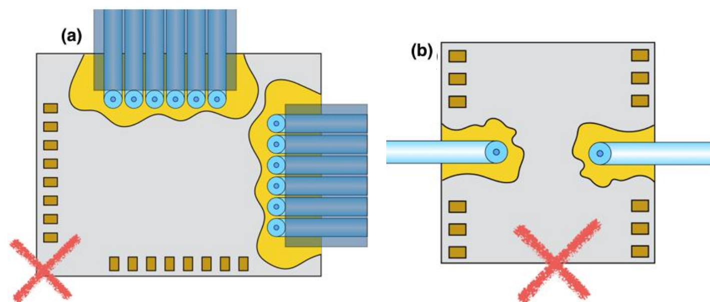


Figure 33: PIC designs which are not compatible with EuroPractice packaging

PIC Layout

The layout of the electrical bondpads and grating couplers is another important consideration. There are many configurations which are not compatible with the packaging processes available at Tyndall. For example orthogonally oriented coupling of fibres is not permitted as shown in Figure 33 (a). Fibre coupling also cannot be made from a PIC edge that also needs wirebonding as shown in Figure 33 (b).

Electrical connections

The integrated electrical components on Si-PICs require electrical connections and therefore wirebonding is a requirement for packaging of all Silicon Photonic PICs. To ensure that wirebonding is possible and can be done in a fast and cost effective way, it is vital for device designers to ensure their bondpad footprint, pitch and layout are compatible with packaging processes. For example bondpads must have a minimum pitch of 150µm, and be located between 50µm and 500µm from the edge of the PIC as shown in Figure 34(a). It is also not acceptable for bondpads to be staggered as shown in Figure 34(b).

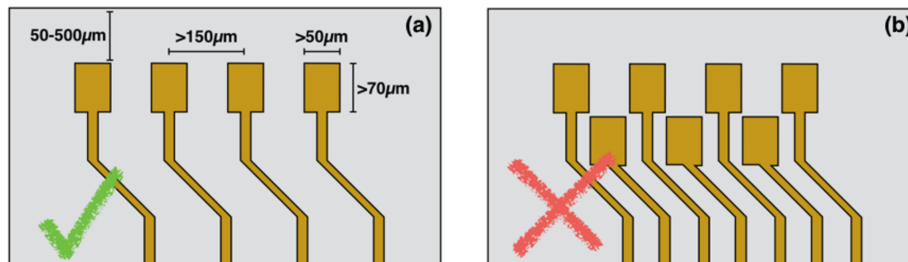


Figure 34: Design rules for bondpads on PICs

The collaboration between Tyndall-UCC and Phoenix has also led to the design rules being incorporated into their software library so that they are implemented in designs using the Phoenix software. This is significant outcome which will greatly help in ensuring PIC designs can be more easily packaged.

Packaging process development

Electronic integration

The packaging of the 4x25Gb/s transceiver for WP6 resulted in the development of new techniques for the packaging of such devices. This included a custom flip-chip process which was developed for the hybrid integration of the microelectronic integrated circuit (EIC) onto the Si-PIC. The flip-chip bonding is carried out using the Finetech flip-chip bonder. The bonding is done by means of a solder reflow process using no clean flux and the application of a bonding force to the upper chip. Figure 35Figure 35 shows the transmitter for APP1 after the EIC has been flip-chipped onto the PIC. This flip-chip process is now a standard process offered by Tyndall.

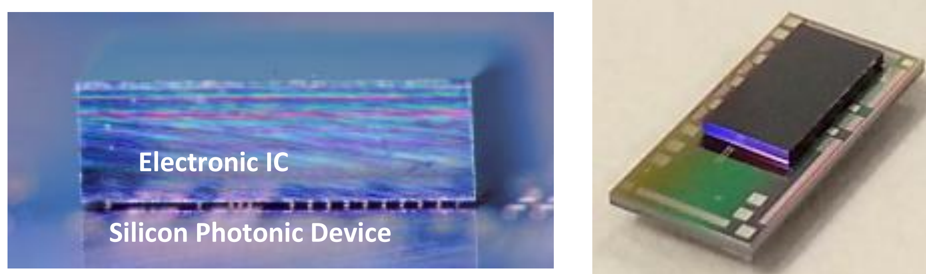


Figure 35: WP6 transmitter after flip-chip process

The use of carefully designed alumina interposers to expand the pitch of closely spaced RF signal lines on the Si-PIC was also further developed and implemented during the project. These ceramic interposers require detailed design and simulation to ensure maximum signal transmission and minimum reflections this is normally carried out in software such as Agilent ADS or ANSYS HFSS. An example of pitch expansion using the ceramic interposer is shown in Figure 36 below.

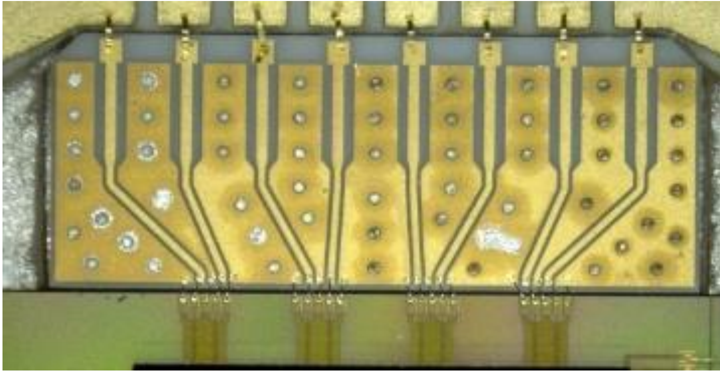


Figure 36: Ceramic interposer used to expand pitch of the Si-PICs RF bondpads

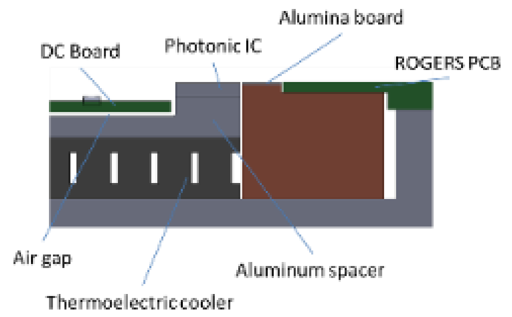


Figure 37: Assembly cross-section showing the solution implemented for the thermal management of the 4x25Gb/s transceiver

Thermal management

Temperature drift generates wavelength shift in the response of photonic devices. As the transceiver of APP1 will operate on the WDM grid a very robust thermal management scheme was required. The scheme developed is show in Figure 37. The PIC is mounted on top of a thermoelectric cooler with no physical contact between the PIC and the external PCBs, except the wire bonds. This ensures the best possible control of the PIC temperature can be maintained as the thermoelectric cooler is not required to cool other components such as the PCBs or copper block supporting the ROGERS PCB. Software such as COMSOL can be also be used to model the thermal behaviour of a package and ensure the best design is implemented.

APP1: Transceiver demonstrator

A 4×25G Transceiver was chosen as a Telecom application for demonstration of LETI and ST platforms. The functionality of such a device are compatible with 100GBase-LR4 standard that means a transmission of signal over 4 WDM channels, spaced by 800 GHz around 1310 nm window, one fibre out and one fibre in. Different versions of Demonstrator are reported in following pictures.

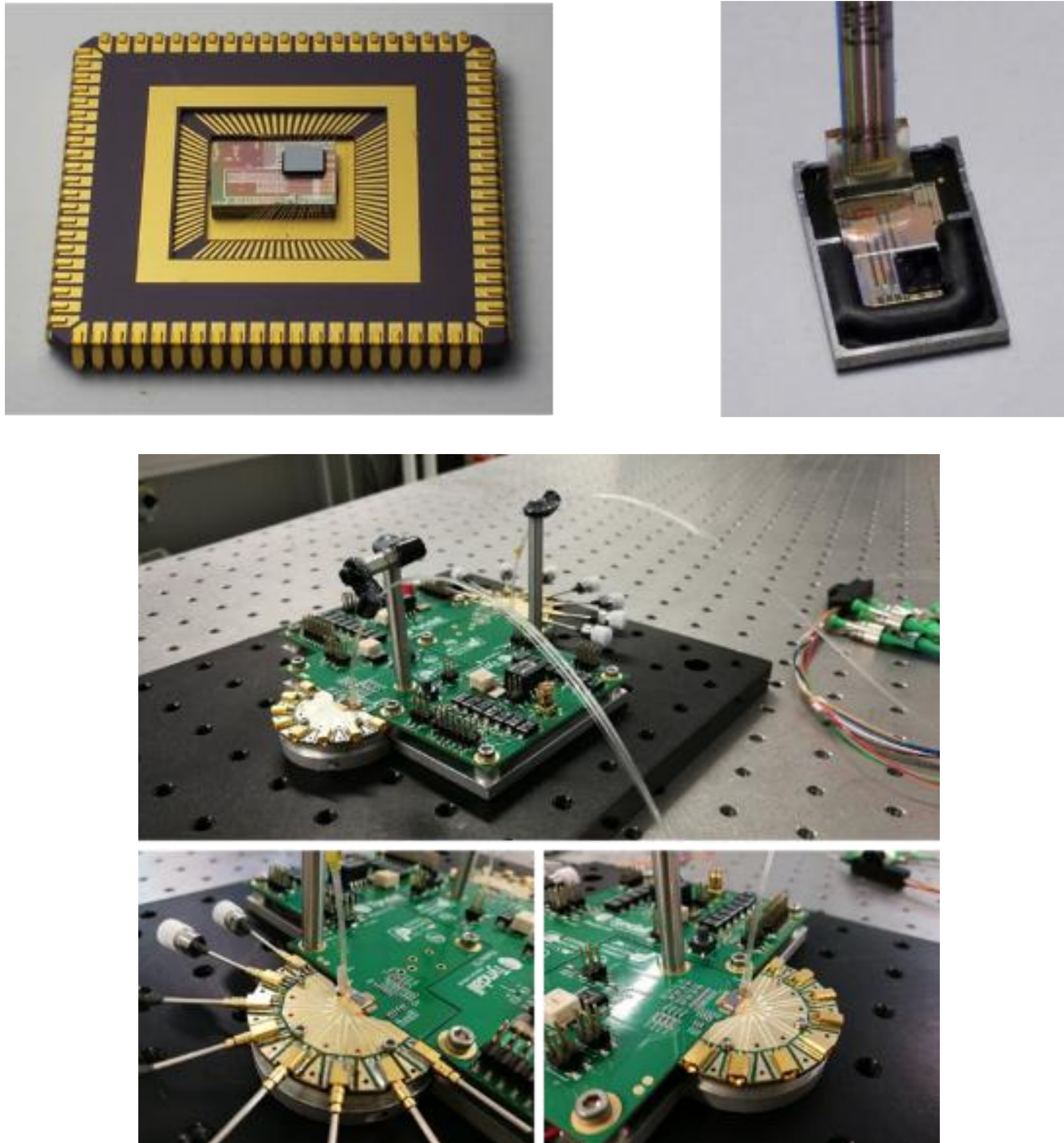


Figure 38. Transceiver demonstrator views

The transmitter comprises a ribbon of 4 SM PM fibres to bring the CW optical source to the OIC, 4 single polarization grating couplers, 4 MZ-modulators each one with its electronic driver, 4:1 WDM multiplexer, a single polarization grating coupler for the output single mode fibre. Each Mach-Zehnder Modulator (MZM) makes use of a multi-stage architecture designed in push-pull configuration, with 3mm length, segmented into 500µm-long sections to minimize rise and fall times, ensuring an ER larger than 4dB with 2.5Vpp driving signals.
The receiver comprises one SM fibre coupled to the Rx OIC through a polarization splitter grating coupler, two identical 1:4 WDM demultiplexers, one for each polarization state, 4 Ge PIN photodetectors with low

parasitic capacitance, each one coupled to a trans-impedance stage followed by a limiting amplifier (LA) and a 100Ω output buffer allowing 25-28Gbps operation.
The electronic functions for both Tx and Rx chains are realized on two separate dice using standard processes.
The transmitter and receiver optical paths are integrated on 3D-compatible silicon-photonics platform, which implements only optical devices in the front-end of line (FEOL).
The electronic ICs, realized in 65nm bulk CMOS technology for the RX and 55nm BiCMOS technology for the TX, are 3D-assembled on top of the photonic IC by means of 20μm-diameter copper pillars, minimizing the interconnection parasitic capacitance.
All the photonic components have been chosen and optimized for low loss and high bit rate performances.
The WDM Multi-Demultiplexer has been designed with a low loss and flat transmission optical bandwidth and high isolation among different channels.
The optical and electronic dice are interconnected through 'copper pillars': this kind of 3D integration allows the minimization of parasitic elements and therefore guarantees maximization of performances and high reproducibility in the production phase.
Transmitter and receiver have been realized on two different 3D assemblies.

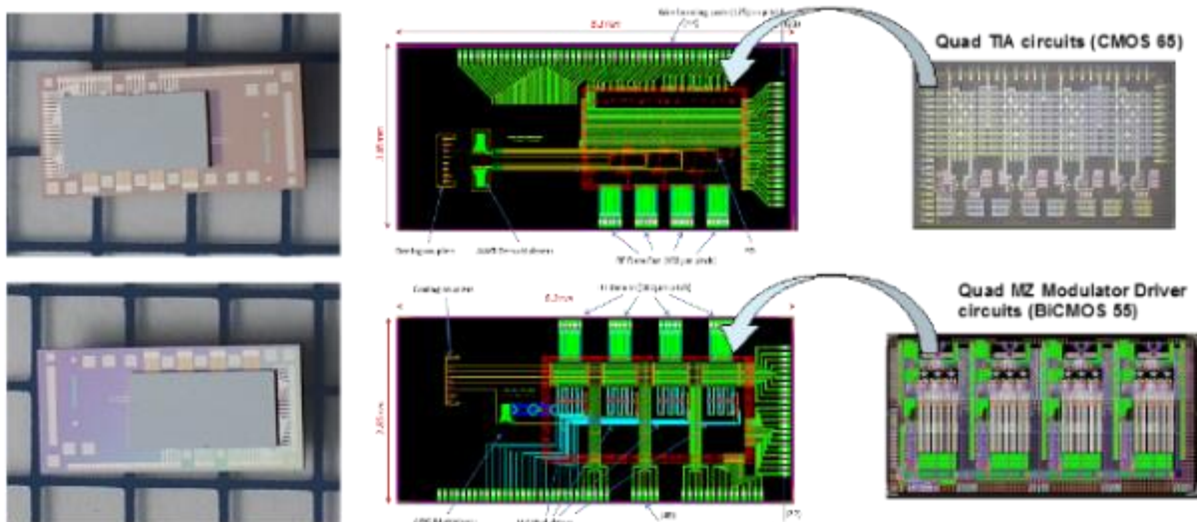


Figure 39. Images of the assembled chips

The first version of the Demonstrator has been realized for single wavelength operation, and the characterization has been done successfully at 25Gbps while the WDM filter has been characterized separately.
A WDM MUX/DEMUX test structure, based on cascaded Mach-Zehnder lattice filter, has been realized with good performances, compliant with filtering characteristics needed by the transceiver. Main characteristics of this filter are: VII + V Order WDM Filter, wide and flat response (ripple below 0.2dB), low losses (1-1.5dB) and good crosstalk (> 15dB). Figure 40

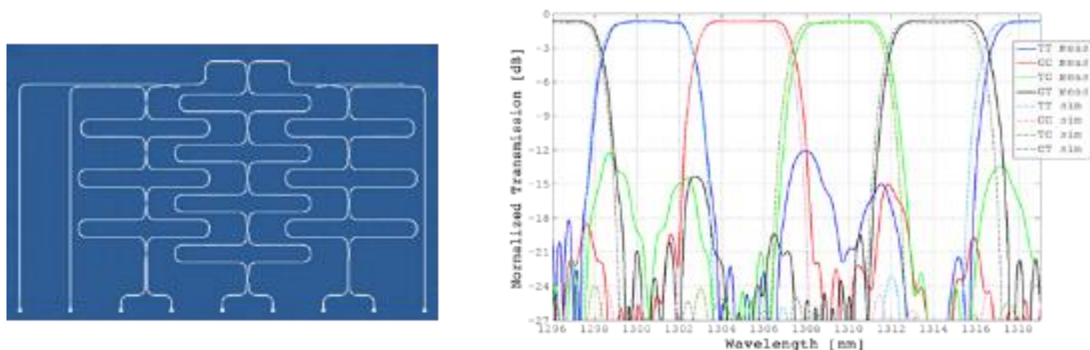


Figure 40. A WDM MUX/DEMUX test structure, based on cascaded Mach-Zehnder lattice filter

In the following figures are shown respectively the RX measured output eye diagram at 25Gbps and at receiver sensitivity, and the TX Eye diagrams at quadrature (simulation vs. measurement) with the 100GBASE-LR4 mask superimposed while the main parameters are reported in the next table.

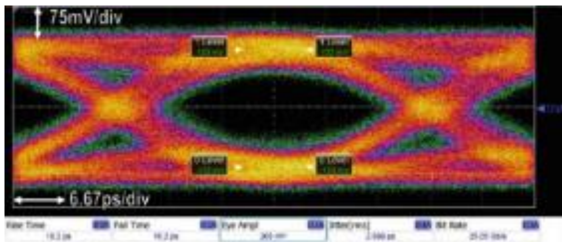


Figure 41. RX: eye diagram at 25 Gbps

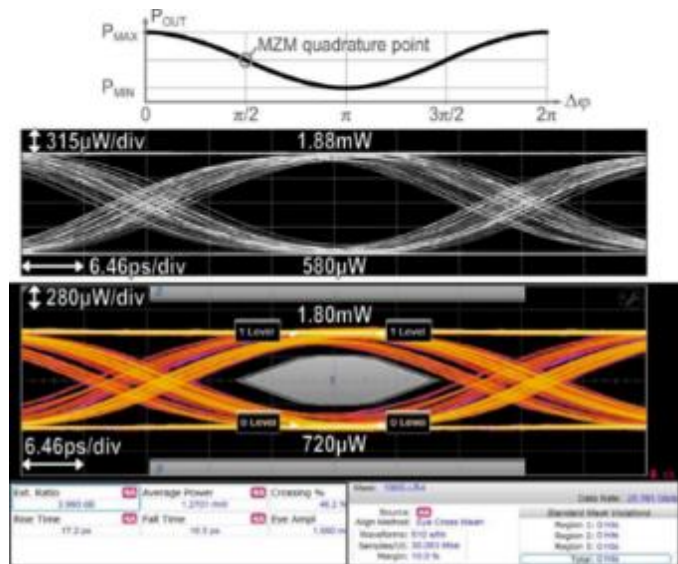


Figure 42. TX: eye diagram at 25 Gbps

Eye ampl.	265 $mV_{pp\text{-}diff}$
Jitter	2.7 ps_{rms}
Bit Rate	25 Gb/s
OMA	-11.3 dBm

RX: main parameters

Data Rate	25.781 Gb/s
Ext. Ratio	4 dB
Rise Time	17.2 ps
Fall Time	16.5 ps

TX: main parameters

APP2 Gas sensor

During the development of Application 2, the aim was to demonstrate a multi-channel sensor and sensor read-out system. As demonstration of this multichannel sensor, a gas sensor was developed, targeting applications for environmental monitoring. The sensors are based on ring resonators, which are sensitive to ambient gas concentrations as result of the employment of a chemical coating on top of the ring resonators. The coating provides the chemical sensitivity and selectivity, as a change in the coating refractive index in response to binding of particular gas molecules is detectable with the ring resonators. Figure 43 shows a schematic overview of the chip that was developed. The total number of sensors that can be individually coated is four. A reference sensor for ambient temperature is incorporated as well. The interrogator consists of a wavelength scanning source, an integrated wavelength tracker, a set of integrated photodiodes and the required electronics for read-out. The advanced integration technology offered in the PLAT4M project allows the integration of the key optical components of the read-out unit on the sensor chip, including the detectors, while at the same time many sensors can be included. Each sensor can be coated with a dedicated coating, in order to screen for a particular chemical compound. The aim was a small, robust, stand-alone device with high sensitivity, that could provide simultaneous information on multiple chemical compounds, which can be mass-produced in high volume at low cost.

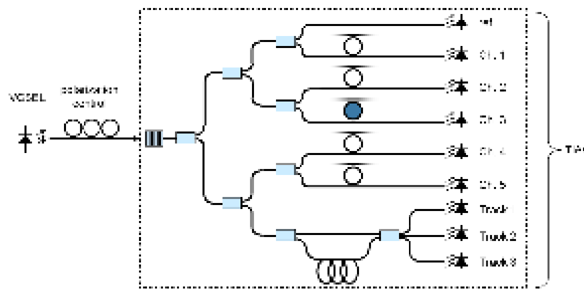


Figure 43: Schematic overview of the chip design.

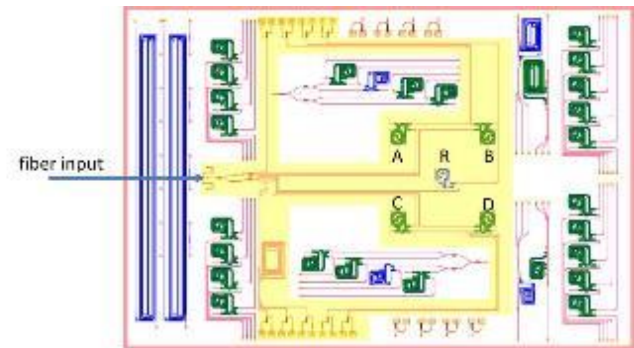


Figure 44: chip layout. The yellow part is the main circuit, all other components are test structures. Rings A-D are sensor rings, ring R is the reference ring which is covered by the dielectric stack. It serves as a temperature reference.

One of the key challenges in this demonstrator relates to the integration technology. The chip must contain integrated detectors in order to be cost effective. These detectors require the presence of a dielectric layer stack of considerable thickness (several microns). The ring resonator sensor elements, however, must be exposed to ambient, so that the dielectric stack needs to be removed locally, in a reproducible manner. If any dielectric material remains on the ring resonator, this will compromise the sensitivity, and lead to sensitivity variations. It took considerable effort, in particular from IMEC, to tackle this challenge. Combined efforts have resulted in the realization of a functional demonstrator.

Chip design

The design of the chips for all three runs was performed at TNO. Consequently, participating in PLAT4M has increased TNOs knowledge on component-, circuit- and system design, which is an important added benefit. Moreover, TNO acted as an early user of the PDKs under development, and so provided additional proofing of the PDKs. The collaboration between TNO, IMEC and Phoenix in the design process has been fruitful. A screenshot of the chip lay-out is shown in Figure 44. The yellow part is the main circuit, all other components are test structures. Rings A-D are sensor rings that are exposed to ambient and can be coated with chemical coatings. Ring R is the reference ring, which is covered by the dielectric stack and serves as a temperature reference. An optical input is used, to which a fiber can be attached (work performed by Aifotec). The rows of bond pads, used to electrically connect the integrated photodiodes, are shown in the top and bottom of the figure in yellow.

Chip performance

Typical ring resonator transmission graphs are shown in Figure 45. Especially the TE performance is very good, and the performance parameters match very well with the design. This means that the device fabrication has been very accurate. The ring resonators are expected to have higher sensitivity for TM polarization. The TM devices have higher bend losses, causing wider resonances. The devices have sufficient performance for sensor application, but further optimization of the TM circuits is recommended. It should be noted that, due to the special socket waveguide structure, the TM devices work only in high ambient index. When exposed to air, the devices do not work properly, and also on that aspect there is good agreement with theory and experimental data.

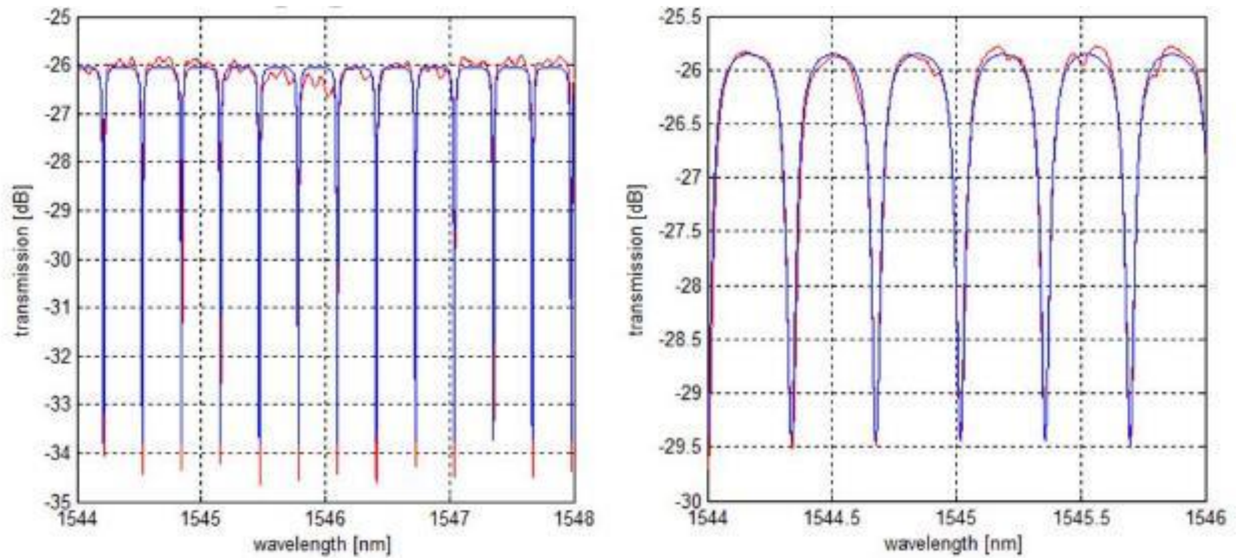


Figure 45: ring resonator transmission for TE polarization (left) and TM polarization (right). The measured data is in red, blue is the theoretical fit to the data.

The integrated detector performance was found to be adequate for short wavelengths at both polarizations, such that the chips are suitable for use in the demonstrator.

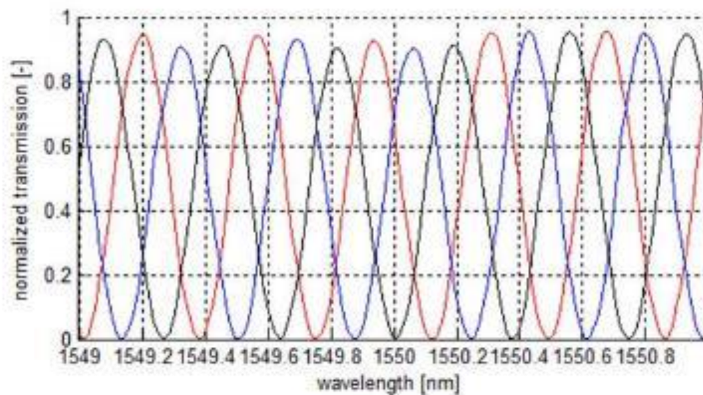


Figure 46: interferometer transmission

Key element in the read-out system is a 3-port interferometer, shown in the bottom part of Figure 43, which is used to track the wavelength of a low-cost scanning laser in real-time. A representative transmission measurement of the three outputs as function of wavelength is shown in Figure 46, with the sinusoidal outputs having a mutual phase difference of $2\pi/3$, as intended.

Sensor read-out system

A demonstrator read-out system was designed, realized and tested for the demonstrator. The demonstrator comprises a miniaturized interrogator for read-out of the demo chip attached at the top. The miniature interrogator is shown in Figure 47. The left part of Figure 47 shows the demonstrator electronics (miniature interrogator) that was developed in this project. The right part of Figure 47 shows the custom made demo software GUI. The top graph shows the ring response of one of the ring resonators. The bottom graph shows the resonance shifts as function of time.

Initially, the set-up was performance-tested with a chip that was positioned on top of the demo board housing. This chip was fully functional, but had no open sensing windows. Tests performed with the demonstrator showed that the sensor read-out system is fully functional and shows excellent performance in terms of noise and drift. The wavelength tracking functionality works well and the conversion from ring-response-as-function-of-time to ring-response-as-function-of-wavelength is correctly implemented. Based on the latter, the resonance shifts are calculated in real-time and displayed by the GUI. Two demonstrators were realized, and later used to demonstrate CO2 sensing.

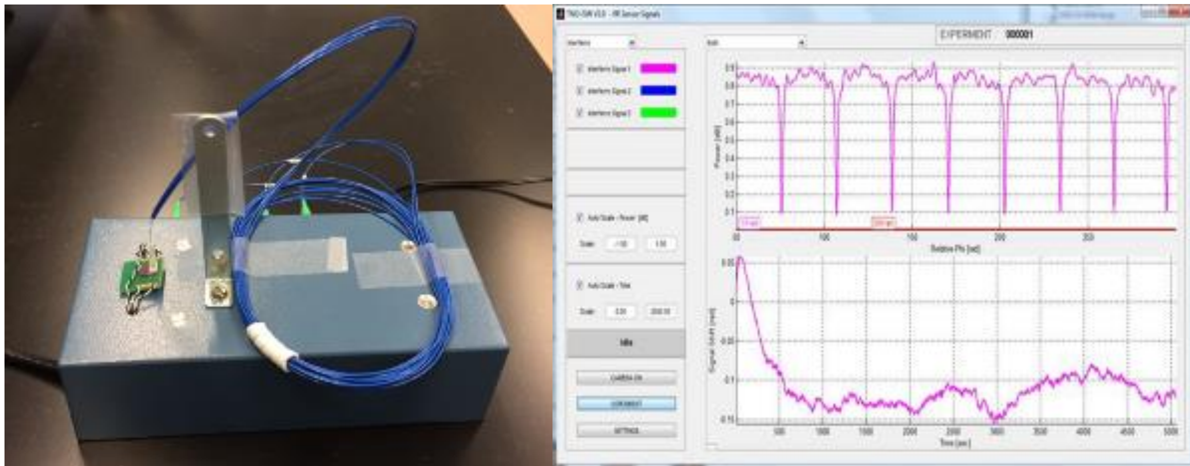


Figure 47: Sensor Read-out system and GUI of the sensor read-out system.

Demonstrator

In order to demonstrate gas sensing, a demonstration set-up was realised. TNO has printed a polyimide-based CO2-sensitive coating on the chips. After coating, the chips were mounted on a PCB submount (designed and fabricated by Aifotec) for wire bonding of the detectors (performed by Tyndall). Subsequently, Aifotec mounted the fiber array. Then, a gas flow cell was mounted on the chip, wires were soldered to the PCB submount and connected to the demonstrator electronics. Finally, PEEK tubing was glued to the flow cell to enable well-controlled gas in- and outlet. The demonstrator was then installed in the Gas Exchange Box. The entire gas handling system is computer controlled and relative humidity is constantly monitored. The measured sensitivity to CO2 was 40 pm / 100%.

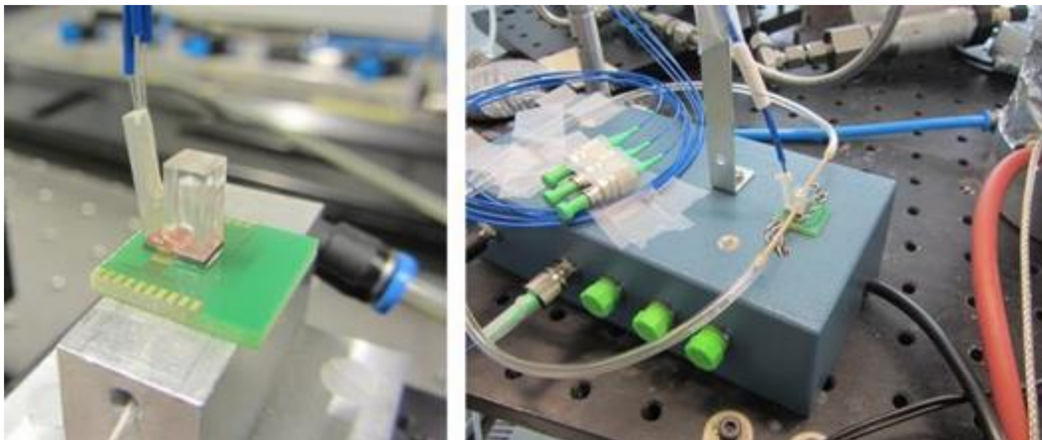


Figure 48: chip adhered and wirebonded to submount, with input fiber and flow cell attached (left), and with tubing on the demo electronics (right).

So in conclusion, we have demonstrated a multi-channel ring resonator based sensor system. The integration technology developed at IMEC enabled us to have sensitive ring resonators, stable reference ring resonators, and stable wavelength trackers on a single chip, with integrated photo diodes. In combination with the miniaturised read-out unit and dedicated signal processing, this platform is very well suited to measure small index changes caused by gas interaction in selective coatings. Though the coating that we have applied has a lower sensitivity than anticipated, sensitivity was clearly demonstrated. We believe that by tailoring the coating chemistry, accurate sensors can be realized. This integrated optics technology allows us to expose multiple coatings to the same sample volume, and to shrink device size. Moreover, this technology enables us to integrate the key optics of the read-out unit, thereby reducing sensor system costs significantly.

APP3 Coherent detection modules

Application 3 deals with coherent detection modules, and in particular focus on Doppler vibrometer and LiDARs.
The first run was dedicated to the validation of various key building blocks, such as balanced photodetectors and frequency shifting architectures. For balanced photodetection, we started with tunable 2x2 couplers, either based on wavelength tuning (unbalanced MZ structure) or thermal tuning. For the frequency shift operation, we investigate the serrodyne approach with a carrier depletion phase modulator, and a 4 branch MZ structure.
After fabrication (imec) and packaging (TYNDALL) of the test vehicles, the characterizations indicated that very good performances of the balanced photodiodes, both in thermal and wavelength tuning scheme. The simplest structures (2x2 passive MMI) also behave nicely, with a common mode rejection ratio sufficient for LiDAR applications. On another hand, the frequency shift operation was not conclusive for run 1, with to high spurious for the serrodyne, and an unsufficient operability for the 4 branch design.
The second run was intended to design and fabricate the first demonstrators generation. From run 1 outcome, it was decided to exclude the frequency shift operation from the demonstrator (performed externally), and to use either thermal or passive balanced PD scheme. Then several demonstrators were designed and fabricated:
1: 16 channels Laser Doppler Vibrometer (POLYTEC)

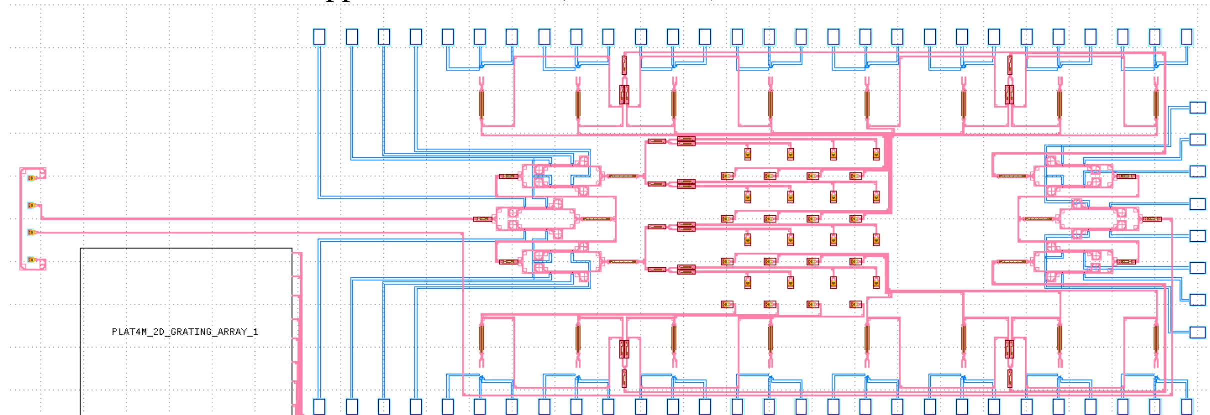


Figure 49 : mask layout of the 16 channel parallel interferometer.

2: Switched Serrodyne frequency shifter (IMEC)
3: 4 branch frequency shifter (IMEC/THALES)

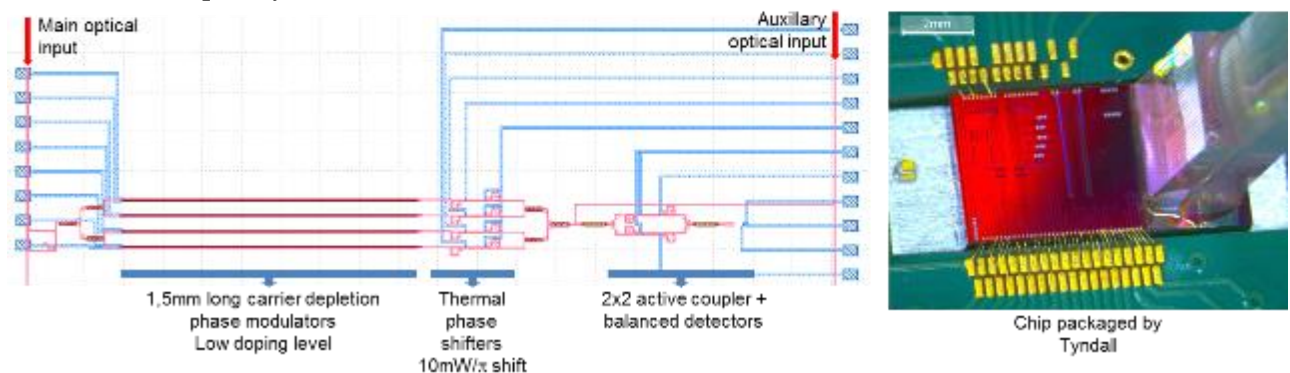


Figure 50 : Mask layout of the 4-branch frequency shifter (left) and fabricated demonstrator packaged by Tyndall (right).

The 4 branch frequency shifter was characterized and frequency shift up to 410 MHz was achieved with nearly 30 dB rejection of the spurious peaks (see Figure 51). A maximum conversion efficiency of ~8.5dB at 70 MHz shift was obtained. These performances could be compatible with LiDAR requirements, but this structure could not be implemented as is in the last demonstrator of the project because the phase biases of the 4 branch interferometer had to be adjusted manually without mean of control. Instead, in the last run, an improved 4 branch structure was designed, including monitoring photodiodes for automatic bias adjustment.

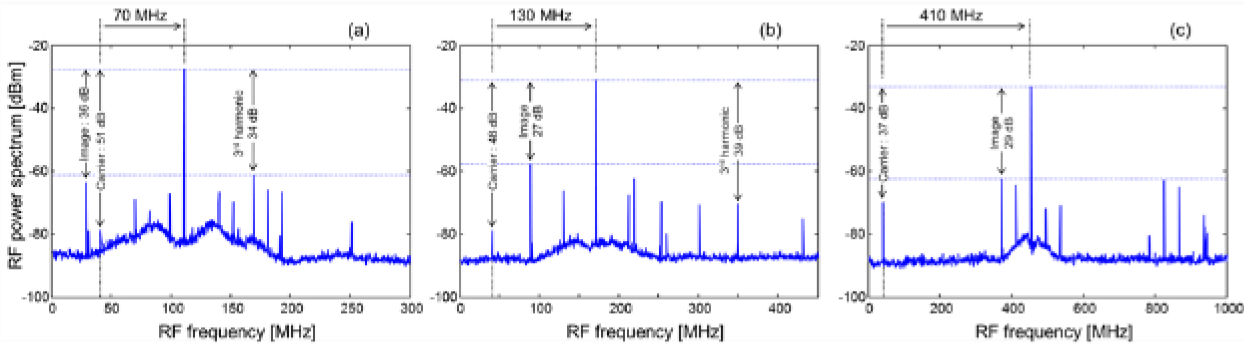


Figure 51 : Electrical power spectrum measured at the output of the balanced detectors for a frequency shift of 70 MHz (a), 130 MHz (b) and 410 MHz (c). Suppression ratio for the image, carrier and third harmonic are indicated, and range from 27 to 51 dB.

In the final run, a frequency modulated continuous wave (FMCW) LiDAR was designed, fabricated and tested. The advantage of the frequency modulation LiDAR scheme is to avoid the use of a frequency shifter. In FMCW LiDAR, range and speed information are therefore obtained by applying a chirp waveform to the laser by modulating its driving current.

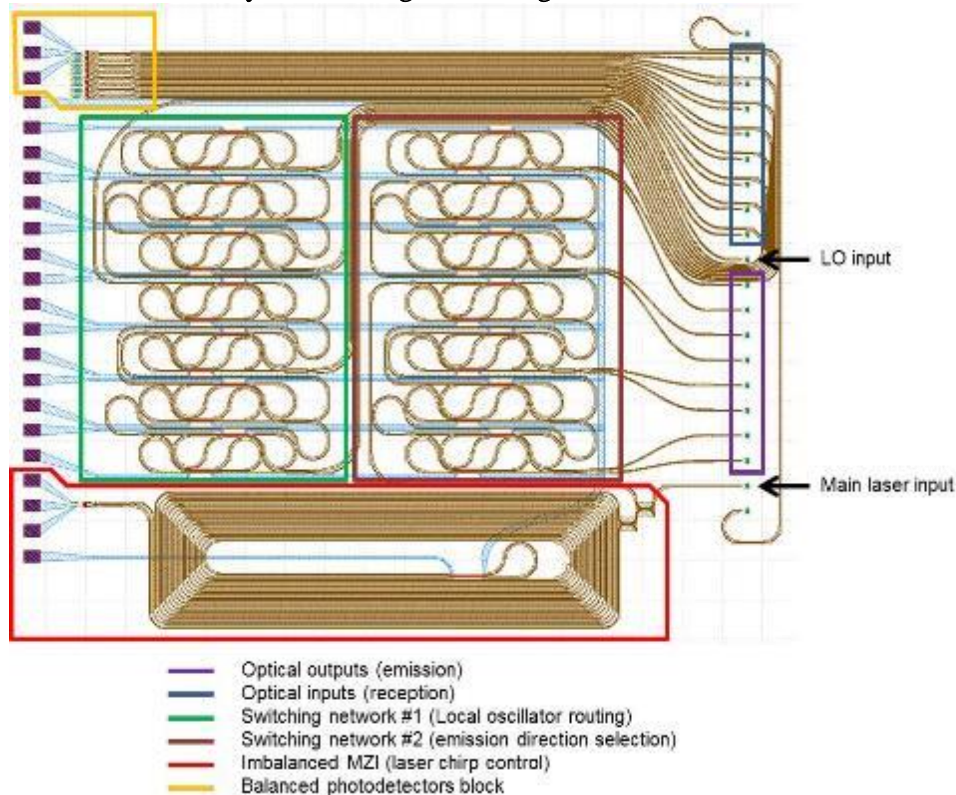


Figure 52 : Mask layout of the FMCW LiDAR module.

The demonstrator photonic circuit is designed to manage 8 different emission directions as described in the figure. A switching network (SN2) routes the main laser input to one of the 8 collimation lenses which point in 8 different directions. 8 external fibered optical circulators redirect the collected

backscattered light back to the chip on 8 input ports (different from the emission ports). In parallel, another switching network (SN1) routes the local oscillator (sampled from the master laser outside of the chip) to the balanced photodetector on which the back-reflected signal is incoming.
Finally, a delay line interferometer is integrated on the chip to measure and control the frequency modulation waveform of the laser.

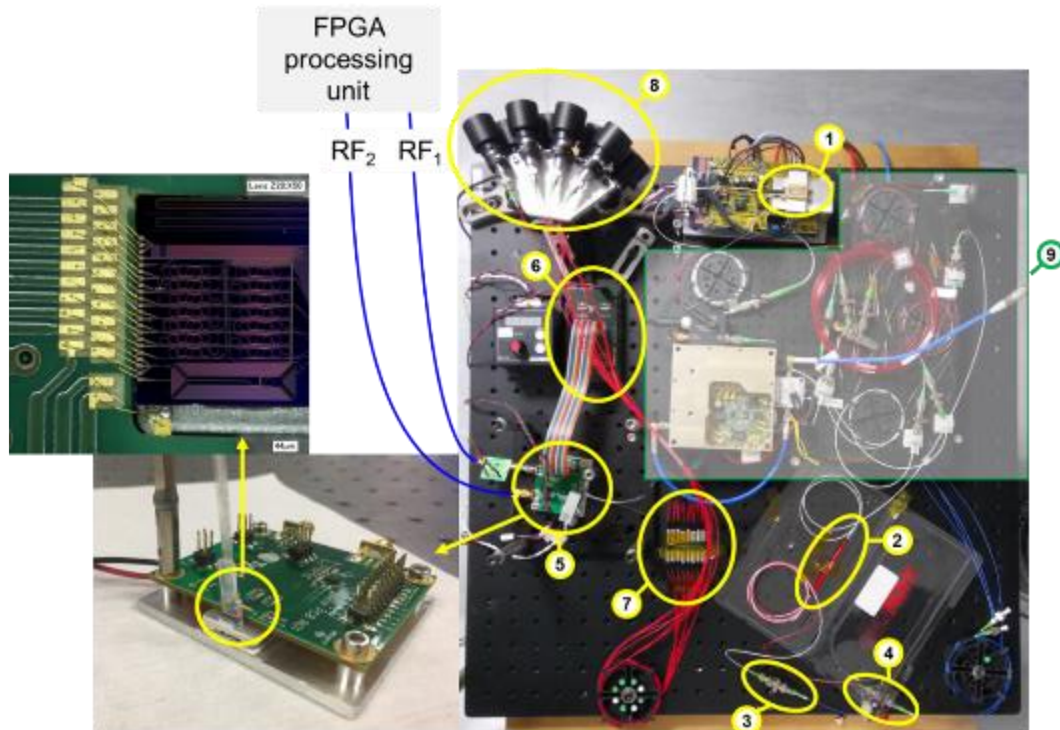


Figure 53 : FMCW LiDAR set-up. 1: DFB laser; 2: 90/10 splitter; 3: LO input; 4: main laser input; 5: Photonic chip PCB board; 6: switch network controller board; 7: optical circulators; 8; collimated outputs; 9: previous set-up, now included in the PIC.

We demonstrated an integrated FMCW LiDAR system with 8 switchable output channels, enabling to scanning directions. The IMEC platform enabled integration on the chip of the 2 switching networks for emission and reception paths routing, a 1 ns delay line interferometer for the FMCW chirp waveform calibration, 8 pairs of balanced photodetectors connected in serial. For this kind of sensing application, power budget is critical, and especially the amount of power that can be finally emitted by the device. To that purpose, IMEC's shallow waveguide profile showed very good performances, with nearly 30 mW of emitted power before significant nonlinear loss. This is very promising for practical use of PIC Lidar devices, where long detection range, or low visibility are envisaged. Another critical aspect for FMCW systems is the chirp waveform quality, which in the present demo was a little underperforming, compared to long, fibered delay line interferometer. Range and speed measurement was demonstrated in the 30m distance range with 5 mW of emitted optical power. The limitation was the insufficient FMCW waveform calibration due to the short integrated delay line. With a longer external delay line interferometer, we demonstrated range and speed target detection at up to 70m distance. Above this range, the DFB laser coherence length makes the peaks processing difficult and only distance information is accessible. Still with only 5 mW of emitted power, we then detected a building at 180 m distance. Finally, the 8 switchable outputs were all functional, with similar performances.

APP4 Coherent beam combining (*CBC*)

The context of application 4 is the coherent beam combination (CBC) of laser beams. CBC is an attractive solution to reach power levels that cannot be obtained by a single laser, by using a large number of fiber amplifiers fed by a single master oscillator, and then to coherently combine the output

of each of these amplifiers. The limitations of an individual amplifier (damage threshold and nonlinear effects in fibers) are then overcome by distributing the power among the large number of amplifying channels. Furthermore, once the output beams are coherently combine, the CBC system offers beamforming capability, useful for many applications, as free space communications, or LiDAR.
The targeted demonstrator for the CBC application includes a 1 to 16 splitter, with then one phase shifter per channel. The outputs of the 16 channels are then coupled through a grating to a fiber array. The major challenges for this demonstrator are first the connectivity complexity, either on electrical and optical side, and also the high optical power that circulates in the device. For the previously mentioned applications, output powers of 1 to several tens of mW are desired, which means input power in the Watt range, well above what a single mode waveguide can handle.

In a first run, a 1x16 binary splitter tree was implemented, followed by thermal or carrier depletion phase modulators.

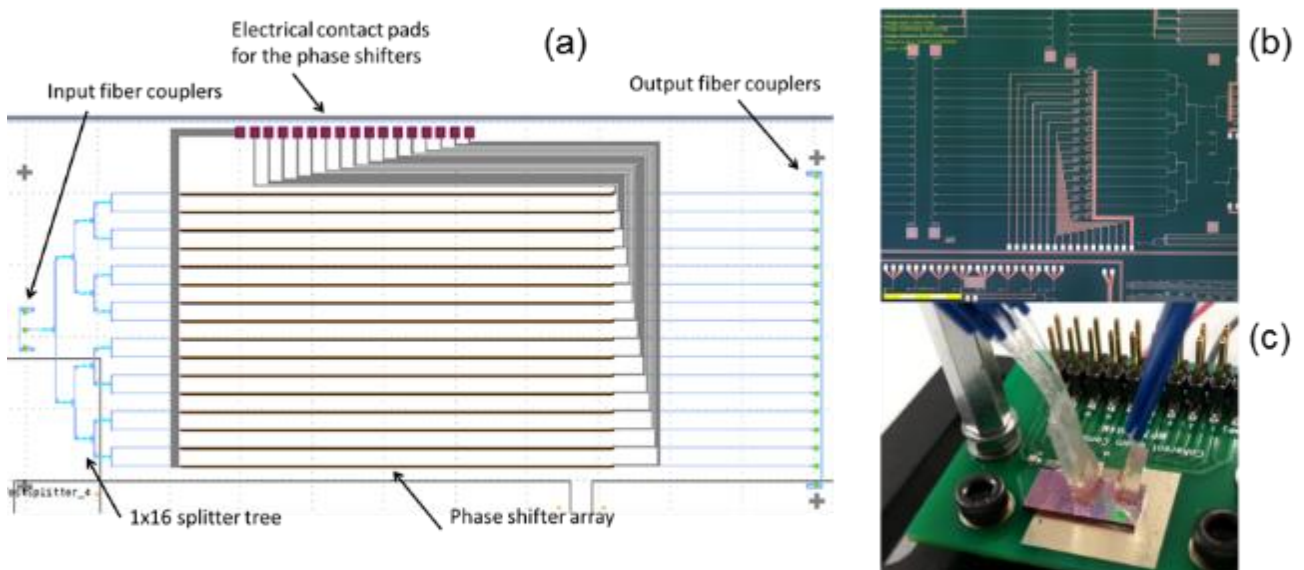


Figure 54 (a): Run1 CBC mask design; (b) fabricated chip; (c) packaged CBC device.

The conclusions for this first run were the following:

- Thermal modulator design is preferred for runs 2 and 3 because of a better power handling (reduced nonlinear losses compared to carrier depletion) and reduced spurious amplitude modulation. All specifications are already reached in terms of phase modulation performances and insertion loss.
- Device packaging was very good, with excellent fiber array coupling uniformity, and electrical connectivity.
- Main issue is the maximum input power limited to 13dBm. For the next runs, a new grating design will be implemented to reach W-level.

The major design improvement in the run 2 was the addition of a new building block which combines the functions of input light coupling and splitting. With this new device, the input power is immediately split when entering the chip, and is never entirely confined in a single waveguide. Preliminary measurements on a test sample shown in Figure 55(b) indicate 3dB nonlinear losses are reached for 30 dBm (1 W) of input power.

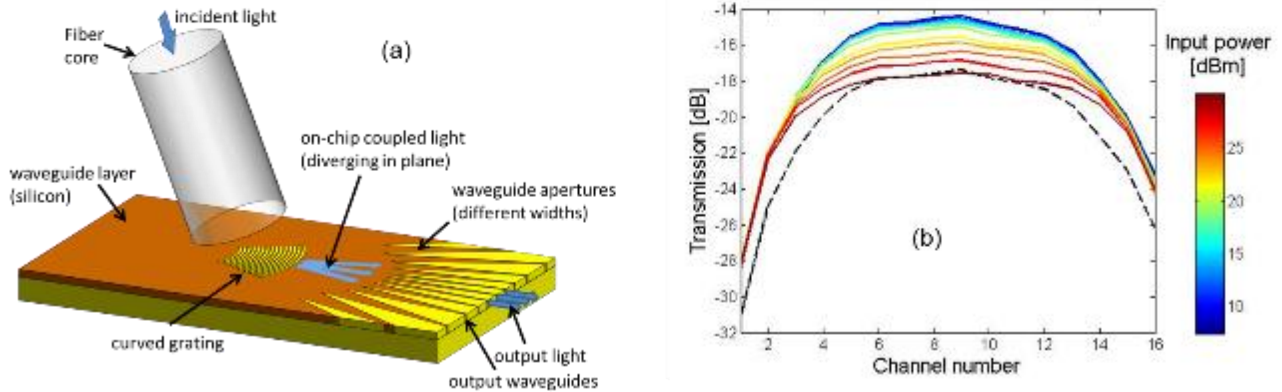


Figure 55 : (a) Grating coupler/splitter schematic design; (b) experimental transmission of the coupler/splitter as a function of input power for all of the 16 channels.

Figure 56 shows the fabricated chip, and its opto/electrical packaging carried out by AIFOTEC. Although the packaged device shows a remarkably good power handling, the channel transmission distribution is not as uniform as expected, with about 10 dB maximum variation. This was finally attributed to mode mismatch at the grating location, and compensated in final runs using a thicker glue layer for the attachment of the input fiber array.

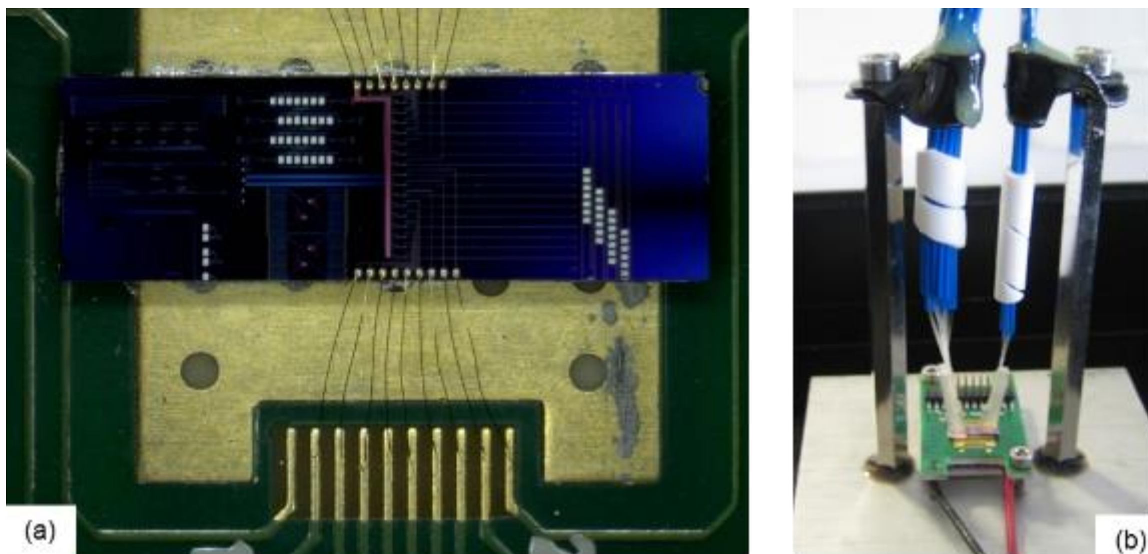


Figure 56: (a) The fabricated run 2 CBC chip with electrical contacts wire-bonded to the PCB host board. (b) Photograph of the optically packaged run 2 device.

The experimental demonstrator CBC set-up was implemented with run 2 device as detailed in Figure 57. On the left, it shows the near field image of the 16 output beams, after the collimation microlens array. As discussed previously, using a fiber bundle, the 16 in-a-row outputs of the photonic chip is transformed into 4 x 4 beams. On the right hand side of Figure 58 is shown the experimental far field pattern of the CBC set-up, with the combined 16 beams. Measurement showed that 50% of the total power is contained in the main central lobe of the far field pattern, indicating an excellent beam combination quality.
A further packaging run (still with fabrication run 2 chips) was performed to improve the channel transmission uniformity and validate the power handling of thicker glue layer. These experiment were conclusive, showing CBC performances identical to those shown on Figure 58, but with ~2 dB channel uniformity (instead of 10 dB).

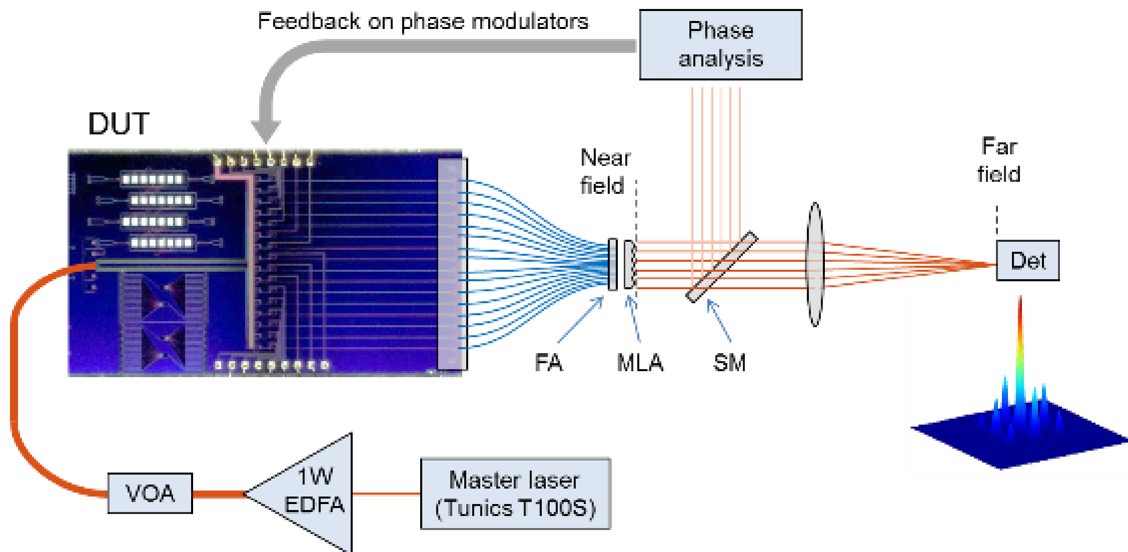


Figure 57 : CBC experimental set-up: EDFA: Erbium doped fiber amplifier; VOA: variable optical attenuator; FA: fiber array; MLA: collimating microlens array; SM: sampling mirror; Det: detector (IR camera or powermeter).

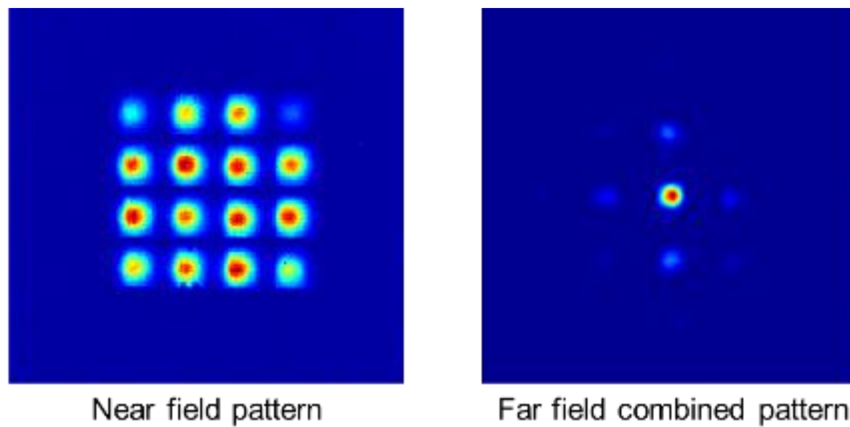


Figure 58 : Experimental near field image (at the output of the collimating microlens array) and far field image of the combined beams.

Major improvement in run 3 is a design variation based on shallow etched waveguide profile. This low confinement waveguide profile should allow to reach even higher input power level. The chip were successfully fabricated, but have not been tested so far. However, power handling tests were carried out on other shallow etched samples, showing a 3dB saturation power of 22 dBm, so more than 10 dB higher than for the deep etch waveguides used in runs 1 and 2.

In conclusion, all along the project we improved our CBC demonstrator design, to show in the end the successful and efficient combination of 16 beams with an optical input power of 27 dBm on the chip, and 14 dBm contained in the far field central lobe. These performances were due to the new grating coupler/splitter design implemented in the run 2 and 3, which offers a 14 dB improvement on the saturation power of the device compared to run 1 device. Further improvement of the saturation power is expected for the final devices based on the shallow etched waveguide profile. The experiments conducted so far indicate that at 30 dBm of input power, the propagation on the chip would still be in the linear regime, with overall losses so in the -6 dB range (coupling loss). We could then expect 21 dBm in the central far field lobe, so a further 7 dB improvement.

4. The potential impact (including the socio-economic impact and the wider societal implications of the project so far) and the main dissemination activities and exploitation of results

PLAT4M will to a large extent contribute to standardization and technology convergence in order to overcome fragmentation of the technology landscape.

The impact of PLAT4M on the European photonic industry will be manifold:

- It will prepare the supply chain for silicon photonics technology, from chip-level technology to packaged circuits.
- It will make accessible integration technologies for a broad circle of users in a foundry-like, fabless way
- It will contribute to the development of an adequate design environment to facilitate photonics/electronics convergence
- Through optoelectronic integration, the key added value in components will be retained in Europe, with little added value in offshore assembly.
- It will move the emphasis from the component to the architecture, and thus concentrate the efforts on new products or new functionalities rather than on the technology level

Silicon Photonics enables high-volume, low cost production manufacturing of optical components for a wide range of applications: from broadband communication to consumer electronics, environmental sensing, medicine, biosensors and imaging.

In the communication field, low cost, low power consumption links will facilitate the emergence of new products/services necessitating intense data traffic, such as the Internet of Things. Silicon Photonics technology looks promising to eliminate the bottleneck introduced by bandwidth limitations and power dissipation in high-density, high-speed interconnection lines presently encountered in the implementation of Computing, Datacom and Telecom equipment and systems.

The potential markets for Silicon Photonics in general are:

- Data Communication: Data Centers, Active Optical interconnects
- Telecom: Metro and long haul applications
- Consumer: Optical replacement of PC interconnects, Display interfaces, HDTVs
- Special silicon photonics sensors in Medical, Industrial and Military applications

Short distance links are mainly used for data center applications. It is becoming a huge market that most silicon photonics players are addressing. It is expected that the market size for data center applications will be several billions of dollars in 10 years.

Coherent transceivers are being introduced in the metropolitan networks. Silicon photonics based coherent transceivers have a number of advantages such as small size, low power consumption and low cost. The market size is not as big as that for data centers, but the coherent transceivers have high added values.

The expected time to market of optical communications product can be categorized as:

Now:
- AOCs for HPC (Already exists)

Short term (1-2 yrs):
- Active Optical Cables for Data Centers

Medium term (3-4 yrs):
- Active Optical Cables (Consumer)
- Fiber Optics Networks FTTx
- Medical
- Fiber Optics Network Metropolitan
- Fiber Optics Networks Long Haul

Long term (4-6 yrs):
- Telecom/Datacom
- Board-to-board
- Chip-to-chip
- Very High Speed Telecom

According to the findings of Yole, the gas sensor market is showing a 7.3% CAGR for the 2014–2021 period. This positive scenario might be possible if gas sensors are widely adopted in consumer products. Several drivers will contribute to the growth:

- Better energy management in buildings.
- Search for very high sensitivity for asthma attack sensors or oxygen sensors for breath control.
- Consumer applications (wearables/smartphones) are driving the development of new highly integrated gas sensors.
- Desire for better outdoor air quality control, the environmental market will grow.
- The transport market is driven by oxygen sensors and future depollution applications.

There is a strong growth in Point-of-Care (PoC) diagnostic tests in Europe, compared to a flat performance of centralized laboratories. This trend is driven primarily by two factors. Firstly, the demand is to reduce costs. The second driver towards more PoC testing is improved clinical outcome. A clear example is early detection of tumors, even before symptoms occur. Early diagnosis in general results in more effective treatment.

Markets for multi-parameter sensing (physical, chemical, and/or bio parameters) are:

- Oil and gas industry (e.g. oil quality, water / salt content, gas analysis, …)
- Environmental monitoring (e.g. smart building, smart road, water quality,…)
- Food / agricultural (quality control based on gas sensing)
- Medical/bio/pharma (e.g. point of care diagnostics)
- Process industry (e.g. gas/liquid analysis, pressure, refractive index, temperature, flow, …)
- Automotive (e.g. motor management, exhaust monitoring)
- High-end production equipment (see process industry)

Multi parameter sensors and sensor networks are suitable for many different applications. The most promising niche markets to start in are:

- Applications which require small, low-cost multi parameter sensors with better performance (sensitivity, dynamic range) than possible with currently applied technologies. Smart building is a good example, where various gas concentrations should be monitored by means of small low-cost sensors.

- Applications where multiple parameters need to be measured in a small sample volume. Good examples are point-of-care diagnostic tests, where multiple biomarkers need to be simultaneously detected in a single drop of blood.
- Applications which require spark free measurements, such as flammable gases and liquids, oil, and explosive detection), or which require EMI insensitivity (in particular in various medical applications which require MRI compatibility

Full-field vibration measurements with an industrially suited sensor are still an open task. Solutions based on bulk optics are quite complex and require a difficult alignment procedure. Therefore, the possible number of channels that could be realized in an industrial system is rather low (< 20). This number does not meet the potential customer requirements of a minimum of 120 channels. Integrated Photonics Chips may enable the realization of vibrometer sensors with a substantially high number of channels (> 100). A complete multichannel-vibrometer measurement station with software could have a market prize in the range of 100.000 € to 150.000 € and should have a market volume of 40-50 systems per year. Light-weight vibrometers with low-power consumption are also possible with Integrated Photonics Chips. This will enable new portable sensors with applications in industrial production automation and in medicine. The potential markets are in the range of tens of M€.

A current typical air data system is composed of probes and pressure sensors. It delivers parameters for the aircraft's flight such as air speed, angle of attack and altitude. The use of laser technology in ADS (Air Data System) is seen as an alternative solution to improve in the future the operation by the main air framers as it is not affected by icing/rain environment and no programmed maintenance operation is foreseen. These systems are built around a 3 axis Doppler LIDAR function as a primary air data channel on civil aircraft and there is a need for size, weight and cost reduction, and provide therefore the high level of cost efficiency and reliability expected by civil air transportation.
Landing assistance for helicopter is a rather niche market but LiDAR characteristics could be quite similar to the one required by mass market application. LiDAR is clearly identified as a key sensor for self-driving cars. It has for example been stated that this sensor would have allowed a recent fatal accident to be avoided. The work performed in PLAT4M also enables the development of range finder / velocimeter using FMCW (frequency-modulated continuous-wave) LIDAR scheme. Compared to pulsed LiDAR (nearly) available on the market, this scheme allows the measurement with reduced peak power leading to optical architecture compatible with PIC. This architecture also brings the following advantages for mass market:

- The LiDAR is not affected by glare in sunlight thanks to a narrow linewidth and spectral filtering
- This architecture leads to better sensitivity in difficult conditions (especially fog in which pulsed LiDARs are blinded by the backscattering on clouds). This also arises from the use of longer wavelength
- The LIDAR is more resistant to Jamming / Hacking which can be of importance for self-driving cars.

For automotive application, the FMCW LIDAR will have to make progress on the number of resolved directions and the field of view which are two of the important characteristics besides resolution. Car and helicopter applications also differ on the distance and speed ranges. These parameters impact the laser power, the calibration delay line length as well as the detection bandwidth, car application corresponding to the tightest specifications (high relative speed, high accuracy and long distance range).

The major outcome of PLAT4M project is the availability of a complete silicon photonics supply chain based on three technological platforms, being supported by a design environment. The potential

impact of the project is the maturation of the technology in order to address a wider range of applications and thus develop the market and the raise of new companies in the field.

Imec has enriched its silicon photonics platform and now offers access to its photonics platform through (1) multi-project wafer (MPW) fabrication services or (2) bilateral development projects for which a modified process flow and/or a full reticle size is necessary. There are two versions of MPW shuttles: simple passives and full actives. Each version is offered twice a year and is managed by Europractice.

CEA-LETI also proposes MPW service for its new photonic platform developed during the project. A dedicated PDK for this activity as well as stabilized process building blocks are proposed. The first MPW call has started in Q1 2016 and the second addressed the full process flow in Q2 2017. MPW services are managed through Europratice or CMP depending of the flow.

ST offers complementary services with respect to LETI. Depending on the maturity level of the proposal and application targeted, the development will be handled by either ST or LETI. For applications bearing a relatively good maturity level, ST makes one-to-one agreements with the partner and develop the proposed prototype. For low maturity level applications, due to the design complexity and partner inability to have access to industrial layout tools, LETI develops the prototype in engineering mode. It is not yet planned by ST to open foundry services to direct customers (universities, SMEs) through CMP services as done for more standard processes like the ones being used for the electronic part of the Photonic systems : 28 nm FDSOI CMOS28FDSOI, 130 nm BiCMOS9MW…

The packaging activities carried out by Tyndall-UCC for the PLAT4M project demos have led to a number of key developments for silicon photonic packaging. One of the most important advances has been the skills and processes developed during the packaging of the project demonstrators. The packaging of a high speed transceiver has resulted in the development of new techniques for the packaging of such devices, including a custom flip-chip process which was developed for the hybrid integration of the microelectronic integrated circuit (EIC) onto the Si photonic integrated circuit (Si-PIC). The use of carefully designed alumina interposers to expand the pitch of closely spaced RF signal lines on the Si-PIC was also developed and implemented during the project. The optical fibre coupling tasks required for the demonstrators have also led to the development of new fibre coupling processes and mechanical packaging techniques to enable the demonstrators to be packaged successfully and enable project partners to validate their device designs. These processes and techniques have considerably strengthened the packaging capabilities of Tyndall-UCC and will allow the provision of more advanced packaging capabilities to its users, enabling them to produce state-of-the-art silicon photonic based ICT, medical device and sensing systems.
Another important output for Tyndall-UCC was the development of a photonic packaging toolkit. This toolkit establishes standardised packaging processes for optical fibres, active devices, electronic components and thermo-mechanical systems. A key part of this toolkit is the design rules developed during the project. These design rules are used by device designers to ensure their PICs can be more easily packaged in a timely and cost-effective way and are crucial for making silicon photonic packaging more accessible. A detailed design rule document has been prepared outlining essential rules which must be followed to facilitate effective packaging, including optical fibre coupling and electrical packaging. The collaboration between Tyndall-UCC and Phoenix has also led to the design rules being incorporated into their software library so that they are implemented in designs using the Phoenix software. The range of demonstrator applications in PLAT4M will also give valuable input to the design of standardised generic packages for silicon photonic based high speed communication and sensing applications.

The demonstrator led by ST-I focused on an advanced transmission module, operating at 100Gbps. The know-how acquired in the framework of PLAT4M project for the design of transceiver circuits has been applied by STMicroelectronics design team to the development of new generation silicon photonics products addressing higher data rate optical communications. ST today's product roadmap targets communication requirements for intra data centres and supercomputing systems (<2km transmission distances), for which transceiver modules operating at 100 Gbps are the current standard. The work performed in PLAT4M will open to the upcoming standards at 400 Gbps and 1 Tbps. Note that such transceivers are in space division multiplexing (SDM) made up of several fibers in parallel. Some new developments will also be needed to improve the performances, especially in view of the 1 Tbps transceivers, which the COSMICC-H2020 project will help to develop.

The studies on the multichannel vibrometer demonstrator showed to POLYTEC the function and applicability of components and building blocks of silicon photonics. The material platform proves to be very mature and ready to be used for components in a commercial product. The demonstrator of a multichannel interferometer is able to show nearly the full potential of the measuring principle like an intended product would have. There is a big demand for solutions to enable the measurement of extended surfaces during non-repeatable events. Other applications of integrated photonics are also envisaged replacing classical free space optical systems. There are several scenarios imaginable where integrated optics can replace classical schemes for cost and space saving.

The multi-parameter sensing demonstrator developed by TNO showed the capability of the silicon photonics technology in the field of miniaturised multi-parameter gas- and/or bio-sensors. This demonstration capability is expected to lead to future projects for industry, in which TNO will be able to collaborate with other PLAT4M partners.

The demonstrators of coherent beam combining and FMCW LiDAR both showed excellent performances, which were widely diffused within the Thales Group Business Units. In that sense, the objective of assessing the maturity of the European Silicon Photonics technological ecosystem for industry application has been met beyond expectations. These demonstrators already triggered internal development actions, as well as the elaboration of new collaborative projects, in particular with PLAT4M partners.

The main dissemination activities of the PLAT4M were manifold:

Two press releases were issued: The first one announcing the project and the second one on the maturation of the platforms and first results on demonstrators. This last one on November 20th 2015 received a lot of attention.

Scientific activities resulted in 13 articles in Journals and 61 presentations in conferences.

Two Silicon Photonics Summer schools were organized. The first one took place on 29th June – 4th July 2014 at Gent University and was attended by 155 participants. The second Silicon Photonics Summer school was scheduled 29th August - 2nd September 2016, at Gent University and was attended by 81 participants. All lectures of the summer schools have been archived using multimedia technology with 2 synchronized video streams capturing the lecturer and the narrative and a screen capture of the electronic beamer. The complete archive is publicly available on the PLAT4M website.

There have been several Silicon Photonics design courses to introduce the design community to the different technologies, design kits and design flow, with hands-on exercises on tools for design, layout

and verification. These courses have been organized at different premises reaching about 120 photonics designers:

- Imec – 18th-22nd November 2013 – 25 attendants
- VTT – 31th March - 4th April 2014 – 16 attendants,
- Tyndall – 24th-28th November 2014 – 16 attendants,
- Imec – 16th-18th March 2015 – 25 attendants
- Imec – 16th-18th November 2015 – 18 attendants
- Imec – 2nd-4th May 2016 – 20 attendants
- Imec – 24th-26th October 2016 – 15 attendants

Additional sessions are scheduled after the end of the project.

- Imec – 8th-10th May 2017 – 15 attendants registered
- Imec – Q4 2017 – yet to be announced

5. The address of the project public website, if applicable as well as relevant contact details

A project public website http://PLAT4M-fp7.eu/ is available.
The project coordinator email is: jean-marc.fedeli@cea.fr