ADDAPT

Adaptive Data and Power Aware Transceivers for Optical Communications

Deliverable Report D 1.4

Final Report

Small or medium scale focused research project (STREP)
ICT-2013.3.2 Photonics

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Version Management

Table 1: List of Revisions

Version	Description	Author	Released
V1.0	Document creation, copy of publishable summary, Executive summary and conclusion	R. Henker (TUD)	November 20, 2017

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Executive Summary

This public deliverable report D1.4 is referred to the third Project Periodic Report which will be submitted via Participant Portal. It summarizes the progress and results of the third ADDAPT project phase covering project month M29 (March 2016) to M48 (October 2017). As the project report is confidential due to unpublished and unpatented content, this deliverable report D1.4 is public. It shows the publishable summary of the third project report which summarizes the project context and objectives as well as the project progress and results of the first, second and third project phases. Finally, the overall results of ADDAPT are concluded.

1 Publishable summary

1.1 *Project context and objectives*

The performance requirements of existing and future optical networks, especially of the optical links and interconnects, are not static and change over time. The individual needs of the users, applications and boundary conditions lead to a strong dynamic behaviour of data rate in today's data networks for instance. However, existing optical networks operate statically at their maximum performance to accommodate the peak traffic requirements and therefore, do not offer much adaptability. Thus, the links are not flexible and not energy-efficient. Therefore, one of the main innovations treated by ADDAPT is to adjust the performance and in turn the power consumption of the multiple optical links from system down to optical device, electrical circuit and transistor level to the actual required data load and link conditions. To achieve this, a high-speed electro-optical transceiver module will be developed whose parameters like bandwidth, modulation format, clock rate, amplitudes can be adapted as it is illustrated in Figure 1. This leads to a reconfiguration of the system according to the actual transmission requirement which in turn reduces the system power consumption. To realize this, a smart adaptivity control is implemented that decides how and when the system parameters need to or may change. The transceiver design includes novel high-speed directly modulated lasers and photodetectors equipped with low-loss low-cost efficient optical coupling, novel adaptive integrated circuits with equalization facilities like laserdiode driver (LDD), transimpedance/variable gain amplifier (TIA / VGA), clock data recoveries (CDR) in advanced 14 nm CMOS technology and high-speed low-loss packaging solutions using glass or ceramic substrates. A transceiver system with 4 link paths each with adaptive data rates from 7 Gb/s up to 56 Gb/s and maximum 10 m link distance is targeted. Further goals are low power consumption and high energy efficiency of the transceiver and its components as well as low latency data transmission. The development of such an adaptive optical interconnect paves the way to build flexible energy-efficient optical transmission links and networks coping with varying bitrate demands and pave the way for massive reductions of CO_2 emission and costs.

Key applications of ADDAPT are optical interconnects for short range data communication, e.g. in data-centers or high performance computing (HPC), for rack-to-rack, server-to-server and board-to-board connections. One possibility would be to replace standard fixed performance and power consumption active optical cables (AOC) with ADDAPTive transceiver.

To achieve the project goals, the ADDAPT consortium involves a full supply chain from semiconductor technologies, component and system design over packaging, assembling and characterization to user requirements, interconnect applications and commercial markets. Complementary competences of 3 large companies, 3 SMEs and 2 universities including device manufacturers, suppliers of communication equipment and network operators are combined. Involved EU and associated countries are the Netherlands, Czech Republic, Poland, United Kingdom, Cyprus, Switzerland and Germany.

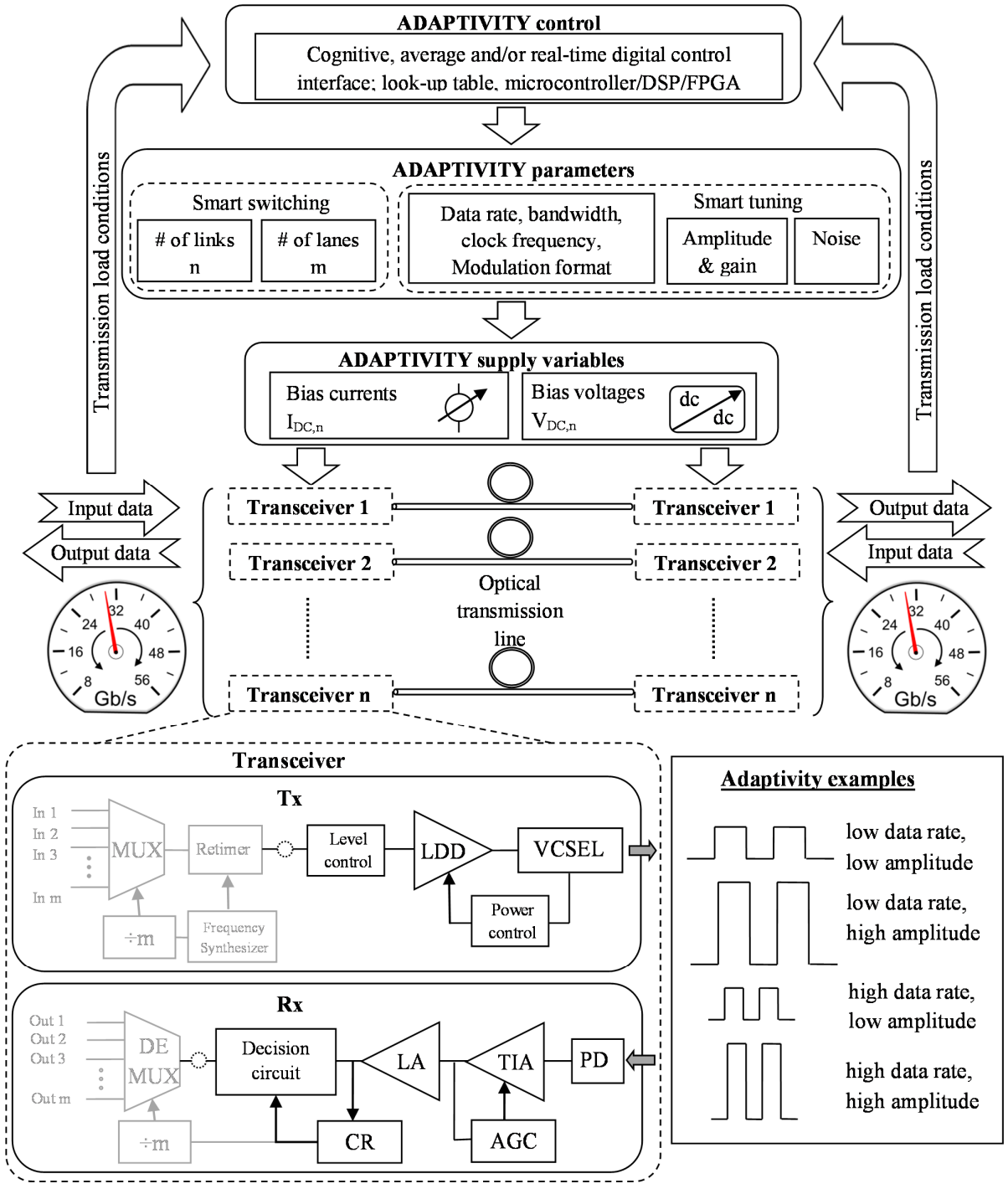

Figure 1: ADDAPT concept.

1.2 *Project progress and results*

Started in November 2013 the project has recently passed the third project period and was finalized by October 2017. In the first project period from November 2013 to December 2014 the project has successfully been launched and elaborated from management point of view. The main research focus was on system and component specifications. Concepts for the high-speed adaptive energy-efficient 4 lane system have been defined and the design of the first components has been started. During the first project period, 10 project deliverables with reports have been provided which state the progress and results.

An intensive market, application and standardization study shows the huge potential of the ADDAPT technology in HPC and data-center environments. Appropriate dissemination and exploitation activities have been defined. A long term network analysis over one year revealed that the link utilization in a data center is on average indeed below 50 % which makes the ADDAPTive techniques reasonable. A first system concept with 4 link lanes each running up to 56 Gb/s with less than 4 pJ/bit and equipped with adaptive rapid on/off switching (< 20 ns) and smart speed tuning functionality between different data rates (56-28-14-7 Gb/s) for additional power savings was developed. This is based on a master-slave concept with one master lane always running to keep the phase information for a fast wake-up of the slave lanes. For the optical components including vertical-cavity surface-emitting lasers (VCSEL) and photodiodes (PDs) improved designs and fabrication processes were investigated. However, it turned out that equalization has to be applied by the electrical circuitry to achieve the 56 Gb/s transmission rate. Therefore, big effort was spend in the generation of a reliable VCSEL model. A novel near-field coupling (NFC) concept was developed which enables easy alignment in packaging process. The initial concepts and specifications for the adaptive transceiver integrated circuits (IC) designed in 14 nm CMOS technology have been derived from the system concept. A high data rate of up to 56 Gb/s and a high overall energy efficiency of maximum <4 pJ/bit is targeted and subject to be optimized for the laserdiode driver (LDD), transimpedance/variable gain amplifier (TIA/VGA) and clock-data-recovery (CDR). Adaptivity in terms of on/off switching and bandwidth/power scaling is implemented into the circuits. To detect the very weak input currents, the receiver (Rx) has to have a high sensitivity and low noise. To provide this a new configuration of low bandwidth TIA, bandwidth compensating DFE and regulating VGA is implemented. To verify all the concepts and components a packaging concept for a single lane and a 4 lane demonstrator was developed and packaging techniques for 56 Gb/s operation evaluated. The first HF board design iteration including simulations was done. Results show the total insertion loss of demonstrator between ports of IC pad to coaxial connector interface of <3.0 dB. Thermal simulations of the transceiver components revealed that due to the low power consumption the maximum temperature change is just ~ 25 K and therefore thermal inter-component influence is marginal. The design and fabrication of first optical components and ICs as well as packaging test boards were started.

The second project period started in January 2015 and was finalized by February 2016. The main focus of this project phase was on the design, fabrication and verification of the first components. During the second project period, 5 project deliverables with reports have been provided.

The system concept was optimized. The master-slave concept was overcome and now all lanes can be switched off completely. The energy efficiency of the complete single lane link was confirmed to be 4 pJ/bit. The power consumption can be tuned by 80% to 220-97-58-43 mW at 56-28-14-7 Gb/s. Further system level simulations confirm an up to 80 % power saving at link latencies of 10 % by applying rapid on/off switching. First improved VCSEL design was finished and first components were successfully fabricated. They reach single mode emission at reasonable drive currents and an error-free operation up to 45 Gb/s. These are currently the fasted VCSELs worldwide. The laser model has been updated appropriately. The coupling efficiency of optical NFC approach is too low for the application in ADDAPT demonstrator. Therefore, novel coupling scheme to polymer waveguides was developed, but finally a refractive optical coupling was implemented. High-speed PDs have been designed and are in fabrication. Optical transmission experiments verified VCSEL operation at 50+ Gb/s which were published at renowned conferences and journals. First IC designs were finished and the 14 nm chips were measured. The LDD shows functional FFE and high performance electrical operation at 54 Gb/s. Several re-designs with rapid on/off functionality and performance adaptivity are in fabrication. Additionally, adaptive LDD and TIA circuits have been designed in 28 nm CMOS, fabricated and successfully measured regarding their ADDAPTive potential. By reducing the LDD and TIA performance, power consumption can be reduced by 25 % and 50 %, respectively. A second iteration of test boards have been designed and fabricated. Measurements have shown very low insertion loss of <2 dB up to 50 GHz for the complete electrical signal path. Large signal measurements confirmed error-free electrical data transmission up to leading edge 54 Gb/s. Test boards for the single lane demonstrator package have been realized. Besides the technical progress further management activities guaranteed the successful progress of ADDAPT. Further studies on market potentials and competitive solutions still confirm the high impact of the project in the field of data communication in data center and HPC environments. Finally, further dissemination actions in terms of publications for instance and exploitation plans were performed.

The third project period started in February 2016 and was finalized by October 2017 which is the end of ADDAPT. The main focus of this project phase was on the re-design of the components and the setup of the single- and 4-lane link demonstrators which have been measured and characterized. During the third project period, 11 project deliverables with reports have been provided.
Two new epitaxial structures were designed and fabricated to achieve high performance VCSEL operation at higher temperatures. VCSEL process technology was improved and results in well performing devices up to 50 Gb/s (see Figure 2). However, some processing and assembling weaknesses still occurred. High-speed photodetectors were fabricated and measured (see Figure 3). Also they showed some problems with the air bridge process. In summary, 9 VCSEL wafers and 3 photodetector wafers have been processed during ADDAPT runtime and VCSEL and PD samples have been provided for assembling of demonstrators. Optical coupling from polymer waveguide to the photodetector shows significant loss. Therefore, more efficient optical coupling with refractive optical element was implemented into the demonstrator boards.

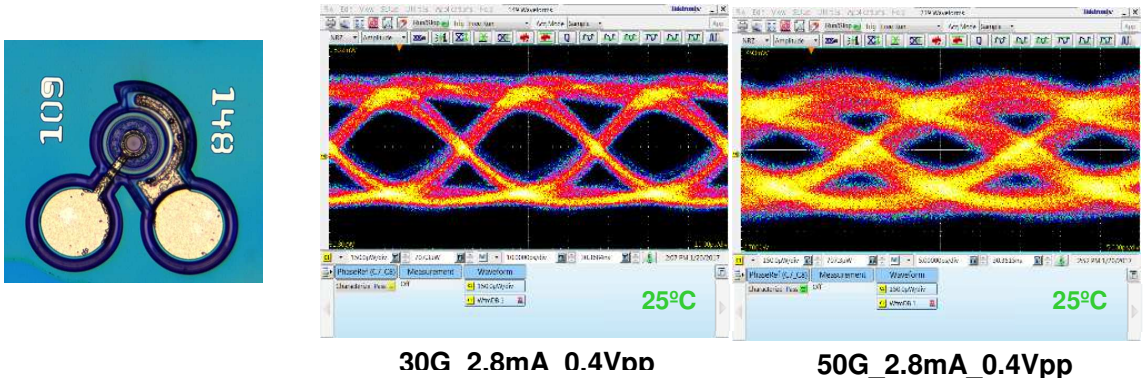

Figure 2: VCSEL chip micrograph and large signal performance at 30 Gb/s and 50 Gb/s.

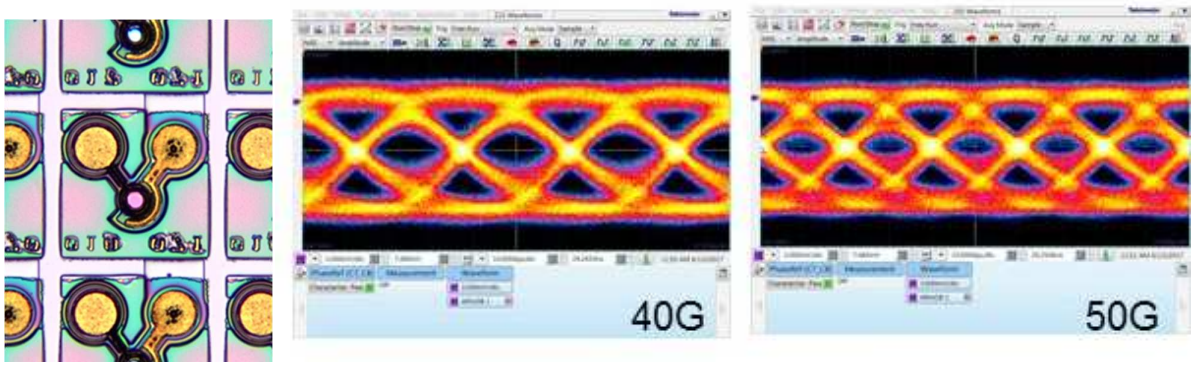

Figure 3: 20 µm photodetector chip micrograph and large signal performance at 40 Gb/s and 50 Gb/s.

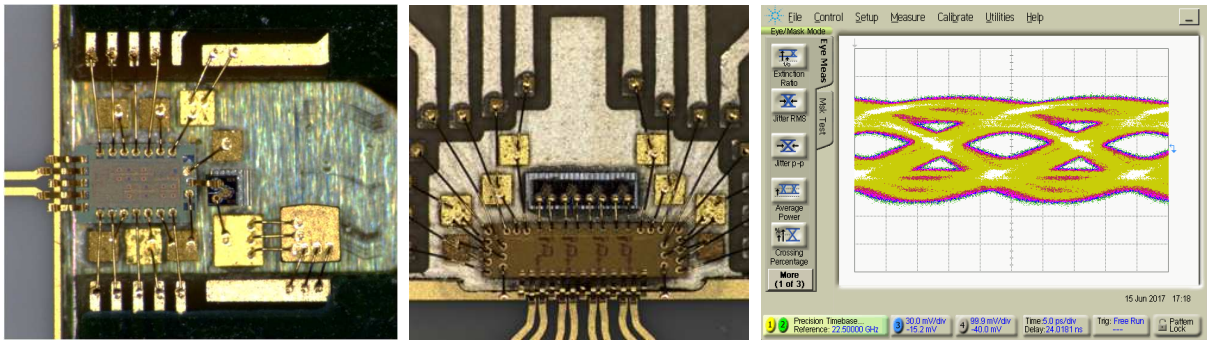

Figure 4: Assembled 1-ch and 4-ch Tx with performance up to 45 Gb/s.

The first 1-ch 4 nm CMOS IC designs were improved on basis of the measurement's outcome. Additional functionality like the rapid on/off switching, signal detection and adaptive tuning were added. Finally, complete 4-ch transmitter (Tx) and receiver (Rx) ICs were implemented and measured. The Tx (see Figure 4) achieves an error-free data transmission with up to 45 Gb/s and an energy efficiency below 2 pJ/bit/channel for all performance modes at different data rates. For the Rx a rapid on/off switching of approximately 8 ns at 56 Gb/s was measured with an energy efficiency of around 2 pJ/bit. Performance tuning scales down the power consumption linearly. Verification of the Rx analog frontend (AFE) consisting of TIA and VGA revealed error-free

operation up to 30 Gb/s. A final AFE chip was designed and fabricated with full additivity (adaptive tuning, rapid on/off switching with signal detect). This has to be measured.
The packaging for the ADDAPT demonstrators was further optimized. The final 5th iteration of the continuous improvement of the test board design, as shown in Figure 5, combines all insights from the previous designs. These were also applied to the multi-channel 4-lane test boards, as shown in Figure 6. The boards show very good performance. Error-free operation was measured at 50 Gb/s but s-parameter measurements show high frequency operation up to 70 GHz. The complete electrical path has very low insertion loss of < 2.5 dB insertion loss at 60 GHz. The cross talk among the channels was verified with approximately -30 dB at 56 Gb/s. Finally, the demonstrator packages were built with all optical and electrical components, as can be seen in Figure 7. In conclusion, 46 demonstrator packages have been built including 25 5th iteration boards and 17 4-ch boards in the third project period.

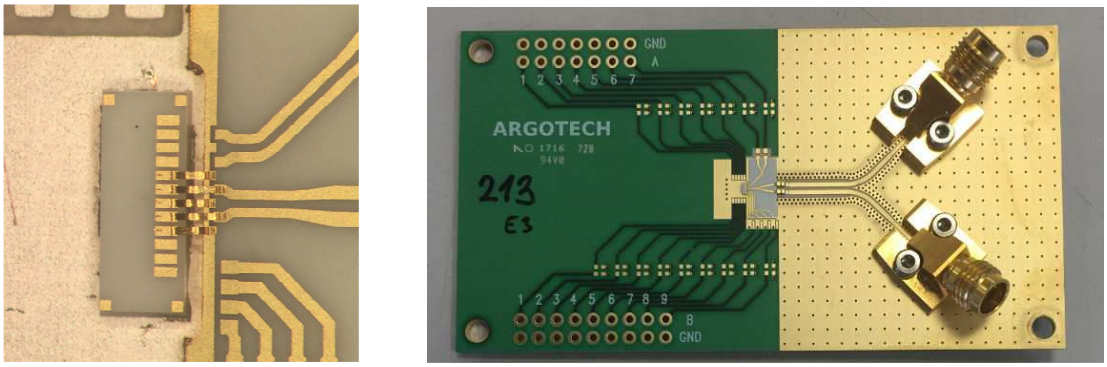

Figure 5: 5th iteration 1-ch design.

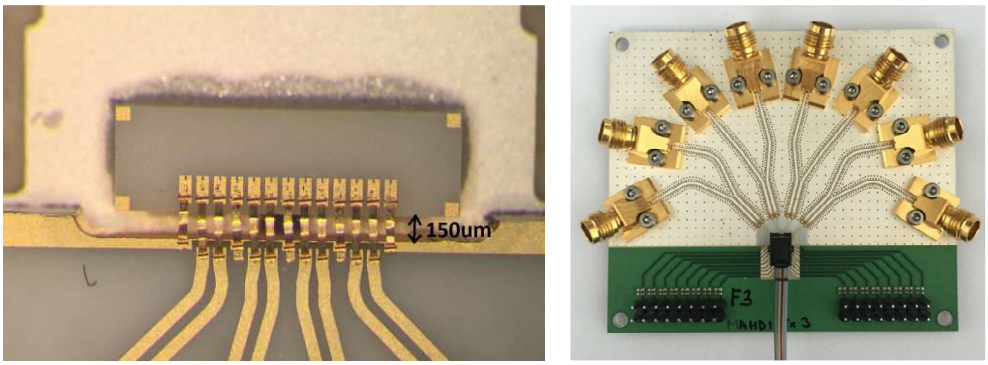

Figure 6: 5th iteration multichannel design.

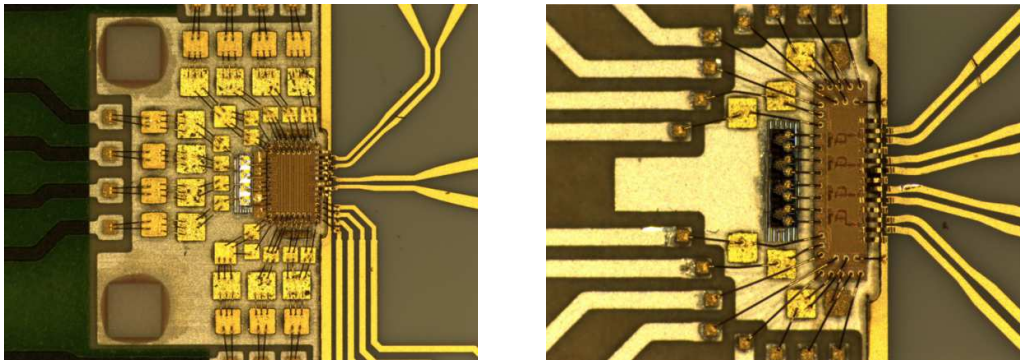

Figure 7: 4-ch Rx and Tx packages.

To measure the Tx and Rx boards in the loop they have been connected with optical multimode fiber, as shown in Figure 8. The verification platform enables the measurement of the performance, rapid on/off switching with protocol and power up/down detection, and the adaptive tuning. Single-channel and 4-ch channel links have been tested. The link is running up to 45 Gb/s with an energy efficiency of 4 pJ/bit, rapid on/off switching <10 ns at up to 40 Gb/s, as well as adaptive data rate and power tuning with energy efficiency below 4 pJ/bit. Currently, this is the fastest and most energy-efficient VCSEL-based link completely with CMOS circuitry.

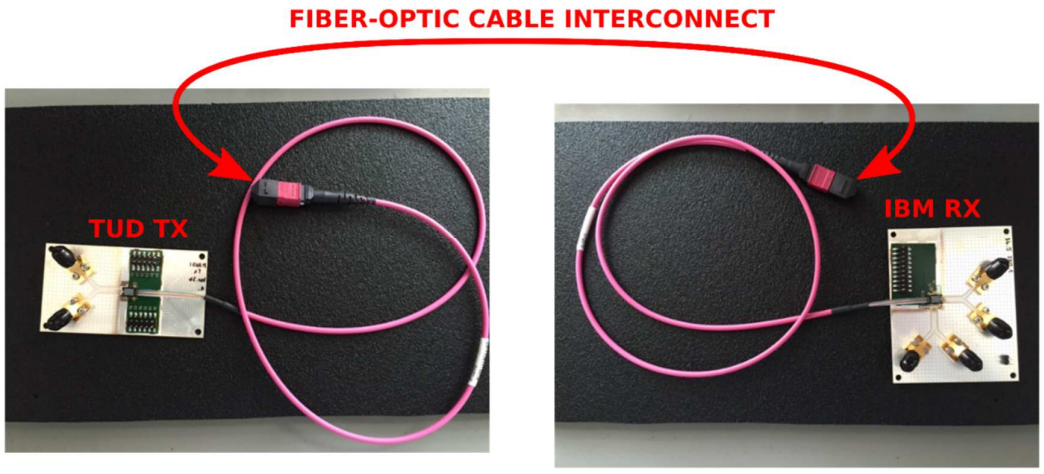

Figure 8: Details of TX/RX package showing 12 channels fiber and MTP connectors.

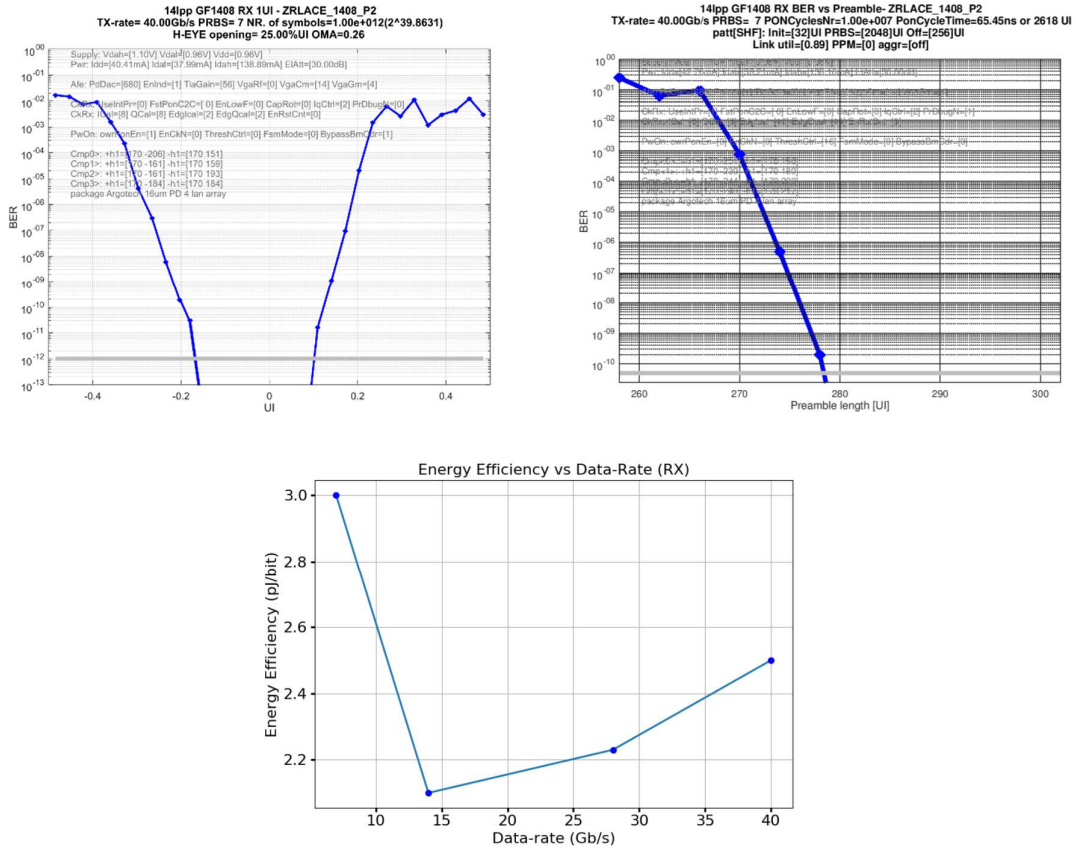

Figure 9: 40 Gb/s link operation with rapid on switching <10 ns and adaptive tuning.

The results of the third project period have been presented in more than 35 publication on renowned conferences and in journals. The project co-organized two workshops on optical interconnect technology at Optical Fibers and Their Applications conference and international Conference on Transparent Optical Networks 2017. Further market and competing solution review revealed that the ADDAPT approach is still unique and the performance advances the state of the art. Due to those good results a start-up company Cooloptics was founded to potentially further exploit the ADDAPT technology.

The ADDAPT coordination enabled the finalization of the project. Due to the step out of project partner TE and the ambitious project goals an amendment was arranged for the reorganization of consortium, resources and tasks including the timeline. The final reports and meeting were organized to conclude the project and its results.

2 Conclusions

In conclusion the fastest and most energy efficient VCSEL-based fully CMOS NRZ optical link was developed with world record switching time and unique adaptive tuning. Many dissemination activities, market and competitor analysis verify the uniqueness and that the impact of the ADDAPT still high. Therefore, the start-up company Cooloptics was founded for potential exploitation of the ADDAPT technology. In this regard parts of the approaches are IPR protected.
IC design was conducted in a leading edge 14 nm CMOS technology which is very challenging on the one hand, but will be used in future processor nodes. High-speed VCSEL and photodetectors were designed and corresponding process development was conducted. The fabrication technology was proven and improved in several iterations. Not all process steps work perfect yet and the yield have to be further improved. Packaging and assembling techniques for high bandwidths, data rates and low losses were developed. A bandwidth of up to 70 GHz (data rate of 54 Gb/s measured) and insertion loss of less than 2.5 dB was achieved for the complete electrical interface. In total 68 single- and multi-channel Tx and Rx demonstrator boards have been packaged. All components, which are developed in ADDAPT, show advances beyond the state of the art. The complete system link achieves error-free performance at 40 Gb/s with energy-efficient 4 pJ/bit and unique adaptive features like rapid on/off switching below 10 ns as well as dynamic bandwidth and power scaling which enable power savings up to 80 %. Although the target of 56 Gb/s link data rate was not achieved, the ADDAPT project results in several world records at the time of it finalization:

- Fastest CMOS optical receiver (64 Gb/s)
- Fastest CMOS optical receiver with CDR (60 Gb/s)
- Lowest power optical receiver above 32 Gb/s
- Fastest CMOS optical transmitter (45 Gb/s)
- Fastest rapid turn-on delay: 7 ns
- CMOS RX showing sensitivity on par with SiGe (around -9 dBm OMA)
- Lowest VCSEL link power consumption above 32 Gb/s (4 pJ/bit)
- Highest HF package bandwidth applied with wire bonding

Therefore, ADDAPT was finalized successfully.

For more details, please refer to:

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Acronyms

Acronym	Definition
AOC	Active optical cable
CDR	Clock data recovery
HPC	High performance computing
LA	Limiting amplifier
LDD	Laserdiode driver
MBO	Mid-Board-Optics
NFC	Near field coupling
OMA	Optical modulation amplitude
Rx	Receiver
TIA	Transimpedance amplifier
Tx	Transmitter
VGA	Variable gain amplifier