



# EURO SERVER

**Project N°: 610456**

## *D7.6 Final Report on Using and Disseminating the knowledge*

*April 5<sup>th</sup>, 2017*

### **Abstract:**

This document defines the dissemination objectives for the EUROSERVEN project, as well as the different targets for all its activities, the dissemination tools, the interaction with similar projects. It defines also how the actual activities support exploitation. First, the project impact is described from different perspectives: strategic, societal, industrial. Then it focuses on exploitation, at first in the global project perspective, and then systematically detailed by each partner.

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Table 1: Acronyms used in this document

Acronym	Meaning
APM	Applied Micro (a manufacturer of ARM based devices, now MACOM)
ASIC	Application-specific integrated circuit
AXI	Advanced eXtensible Interface (ARM)
CAPEX	Capital expenditure
COMPS	COMP Superscalar (technology from BSC for clusters)
CRAN / C-RAN	Cloud-Radio Access Networks
EPA	Environmental protection agency
FDSOI	Fully depleted silicon on insulator
FET	Future and emerging technology
FMC	FPGA Mezzanine Card
FPGA	Field programmable gate array
HMC	Hybrid memory cube (3D stacked memory unit)
HPC	High performance computing
IaaS	Infrastructure as a service
IO	Input / Output
IoT	Internet of Things (generally refers to small embedded, smart devices)
IP (block)	Intellectual Property (refers to code that runs on an FPGA that can be licensed)
MPSoC	Multiprocessor system-on-chip
NFV	Network Function Virtualisation
NRE	Non-recurring engineering (costs associated with R&D for a new technology)
NUMA	Non-uniform memory access (when describing multi-socket systems)
OFED	OpenFabrics Enterprise Division (Technology from Mellanox)
OPEX	Operational expenditure
OS	Operating system
PoC	Proof of concept
QPI	(Intel) Quick path interconnect technology for connecting high-speed system devices
RDMA	Remote Direct Memory Access
SDN	Software Defined Networks
SIMD	Single instruction multiple data
SiP	System-in-Package
SoS	System on Silicon
STB	Set top box
UEFI	Unified Extensible Firmware Interface
VM	Virtual machine

## Introduction

Effective dissemination of the EUROSERVER project outputs is of great importance to the project partners and will be closely linked to the project's success. This document details how the knowledge and expertise generated in the EUROSERVER project has been disseminated and used. Per previous iterations of this exercise, this report includes the general objectives that the dissemination activities were designed to achieve, the methods by which these have been carried out and the metrics on which they have been evaluated. This report also contains the partners' efforts towards exploiting the project results relevant to their domains of expertise, as documented in the project Description of Work.

The dissemination strategy falls under WP7, which is divided into three main strands:

- Communicating project progress to a wide audience
- Establishing the de-facto standard for specifications and models developed during the project through publications and knowledge transfer to industry partners
- Exploitation activities

The inclusion in the project of worldwide research centers and well known universities has provided a clear path to dissemination of EUROSERVER outcomes through conferences and publications, as well as through teaching new students who will be the architects of future systems.

The difficulty in finding and recruiting skilled engineers is a reality in Europe and western countries. This requires training and development of students and junior engineers who will be able to meet the forthcoming challenges as identified through EUROSERVER. Although EUROSERVER has been technically challenging there have been a number of opportunities for junior engineers and PhD students to participate in the project, not only having a direct contribution to the project, but also learning from a diverse set of companies in order to realise changes that will have an impact on society. This training has been invaluable and assists not only the consortium but also the next generation of scientists, engineers and designers.

Since the project requires the creation of a functional prototype a commercial deployment of such a prototype would be comparatively simple and as such the applicability to market is high. The EUROSERVER functional prototype has been designed to logically and physically support the chiplet concept. It encourages modularity and could be aimed at multiple target markets with limited non-recurring engineering (NRE) cost and effort. NRE costs are the one-time costs incurred when trying to deliver a new type of device, which is aside from the production costs. The partners in the project have selected key individuals that have a strong bearing on company policies. These individuals and the companies have been selected not only for their understanding of the technical challenges required and the ability to meet them but also such that they can help alter the direction of the company roadmaps.

This final document reports the use and the dissemination of EUROSERVER knowledge throughout the course of the project. This report as a final version covers all the exploitation activities that have been carried out through the 41 month duration of the project.

## General objectives

The main objectives of the dissemination activities that have been undertaken as part of WP7 are outlined in this document are as follows:

- To ensure visibility among key project stakeholders
- To raise awareness of the project, the issues it raises and project outcomes among a wider audience, especially potential end users
- To engage key groups such as PhD students, engineers and businesses and encourage their participation in the project
- To influence the IT industry in terms of the energy efficiency and total cost of ownership of their products
- To establish the de-facto standard for specifications and models developed over the course of the project
- To exploit EUROSERVER outcomes with industrial partners

## Target audience

This section lists the target groups of the EUROSERVER project. The project should be able to attract the attention of the following groups:

- EUROSERVER partners
  - Researchers, technical management, senior management, sales, marketing
- Scientific community involved in the topics related to the project, as well as end users of the possible technology to be developed
- European IT Industry vendors of servers and energy-efficient servers
- Cloud computing service providers
- Research organisations
- Stakeholders
- Policy makers
- Related EU and International Projects: HiPEAC, Mont-Blanc, DreamCloud, FIPS, POLCA, PRACE, SUPERFLUIDITY, ExaNoDe, ExaNeSt, ECOSCALE, and EuroEXA.
- General public

## Competitive analysis

EUROSERVER is not the only consortium and company working on low-power ARM-based micro-server designs. There are several competitors in this industry. For the purpose of keeping up to date with the changes in the ecosystem, EUROSERVER first performed an update to the competitive analysis in May 2015 that was then presented at the interim review. As this is an ongoing activity this was re-performed and forms the basis of the DATE'16 Paper that was prepared in October 2015 – *EUROSERVER: Share-Anything Scale-Out Micro-Server Design*. An analysis of different solutions and systems was performed.

The ARMv8, 64 bit ecosystem has enjoyed an increase in the number of companies and institutions that have been involved. HP has launched two specialised cartridges that use ARM technology in their converged, Moonshot platform. The M400 cartridge is based on the Applied Micro (APM) X-Gen1. In

addition there are other companies that have taken advantage of the 64 bit designs including MiTAC (APM X-Gene1), SoftIron (AMD Opteron 1100), miniNodes (Kirin 6220) and Dell Storage PoC (APM). There have also been alternative solutions that are in stages of testing and/or sampling, Qualcomm have a 64 bit solution and the 64bit ThunderX and ThunderX2 systems from Cavium.

The 48-core Cavium ThunderX is an interesting platform and although there is a product available with double sockets, there is the capability to use quad sockets. These cores though are small CPUs and will suffer the same issue that Intel has with QPI in getting a coherent platform so has limited scalability. EUROSERVER does not limit or define how big a coherent island can be. Many coherent islands can be connected together through UNIMEM using a memory architecture rather than the traditional share-nothing device based communications abstractions that are present in most current architectures. The ThunderX platforms therefore differ from EUROSERVER in that they offer the traditional multi-socket NUMA platform that has been present for the last few years that suffers from the inherent scaling problems that Intel have seen. The sockets then use traditional device based communication for extensibility, which EUROSERVER's architecture seeks to overcome.

Another big advantage of the EUROSERVER design, relative to the other systems available is that it paves the way towards manufacture by a European supplier rather than a U.S. or global supplier, which has positive security implications and provides a unique offering in the European market. It has been subsequently taken further extensions as ExaNeSt, ExaNoDe, ECOSCALE and EuroEXA.

This competitive analysis carried out in May 2015 has subsequently been updated in January 2017 and is included in Deliverable D7.9 – “Review of Industry trends – Competitive analysis.”

## Realised impacts

### *Strategic impact*

The EUROSERVER project had a broad, strategic impact at the European level in opening and fostering an ecosystem across both business and research.

The main realised impacts of the project are the following:

1. Reinforced European technological leadership and industrial competitiveness in the design, operations, and control of embedded systems with performance-density and low-power requirements, key for growth into Internet of Things (IoT) and System on Silicon (SoS) solutions. This has been demonstrated with the creation of multiple follow up projects from EUROSERVER including but not limited to ExaNoDe, ExaNeSt, ECOSCALE, and EuroEXA projects.
2. Growth of the competitiveness of European technology suppliers across the computing spectrum; in particular for data-centre servers with improvements of an order of magnitude in the total cost of ownership, performance-density and energy-efficiency.

This has been demonstrated through the creation of two, commercial spin-off companies; KALEAO Ltd. and ZeroPoint Technologies.

The MicroVisor technology is being used in new commercial offerings. ONAPP has also benefited in working and developing against the ARM ecosystem and working with leading researchers in topics related to potential market areas.



3. Improved system characteristics: energy/cost efficiency, performance-density, compute deployment, nanotech enabled software, security, safety, resource sharing architectures and platforms solutions. EUROSERVER's mechanisms to reach improved system characteristics are described in the deliverables associated with WP4 and evaluated in the deliverables associated with WP6.
4. Increased take-up of European computing technologies in industry, in particular from SMEs. EUROSERVER has achieved this through promoting ARM based servers as realistic server alternatives to American or International server manufacturers.  
The use of ARM based, energy-efficient servers has been investigated by ONAPP and commercial offerings are soon expected to utilise European technology within the Cloud market that ONAPP addresses.
5. Improvements in the efficiency of application software development by breaking the dependence on dual expertise for application development and customisation for advanced computing systems. EUROSERVER has achieved this through two technologies developed in the project; 1) UNIMEM technology for sharing memory resources between different boards and 2) improving the efficiency of the virtualisation platform to achieve near bare-metal performance through the MicroVisor technology.
6. Reinforced open source ecosystem in both the micro-server cloud computing application domain and embedded use through the required enablement and optimisation. EUROSERVER has achieved this through adding contributions to the Xen project and generally feeding back into the open source community for improvements to Linux technologies.

### *Societal impact*

A few of the industrial or societal domains where EUROSERVER has had an impact are listed below.

1. **Cloud Services.** With the massive move of society to mobile compute, whether through the smartphone, tablet or simply Internet connected devices; the requirements of the cloud are going to expand. Today the cost of building the cloud and the associated power requirements are already forcing companies to deploy their data-centre in the most inhospitable and remote locations. The required growth must be addressed by a step-change in approach to delivering these services. The EUROSERVER approach through energy-efficient servers addresses the cloud's compute requirements through increased performance-density, lower operational power requirement and subsequently will lower the total cost of ownership enabling the markets required growth. The improvement to workloads in the Cloud is described in D6.6.
2. **Embedded Servers.** To enable and deploy intelligent systems and services, it is also necessary to create the interfaces and compute of an embedded system. Becoming known as IoT or SoS, these compute networks and systems need the capabilities of embedded servers. Although Europe today is strong in embedded computing, especially across telecom, automotive and air, to secure those markets, and to ensure their growth as these solutions extend into these IoT/SoS solutions, it will be necessary to continue to increase their compute capabilities to increase their intelligence and connectivity while maintaining their strict power consumption requirements. The EUROSERVER approach through power-efficient servers will step-change the performance capability of these solutions while maintaining their embedded power requirements. The integration techniques of the energy-efficient server device will bring the

latest technology to the embedded markets with volumes too small to afford the development of such advanced solutions. This will not only enable the embedded use of such technology but also opens opportunities for innovation in the embedded market where Europe is strong with SME and end market customers. The design of the EUROSERVER prototype is described in D6.7, D6.8 and D6.9.

- 3. Medicine and life sciences.** Genomic therapy and personalised medicine are more and more envisaged as very powerful tools. The explosion of biomedical information, for instance European Bioinformatics Institute (EBI) saw its data volume jumped from 6,000 TBytes in 2009 to 11,000 TBytes in 2010 with more than 4.6 million requests per day, leads to a huge increase in storage and processing capability to go through all of these data. Drug discovery pipeline requires scanning of more than 100,000 molecules per day to check their potential effect. Identification of potential drug candidates for identified disease targets will be fuelled by next generation of energy efficient servers. In this trend EUROSERVER can really bring an innovative solution that will allow in the future such complex processing available for your own doctor and then provided a more efficient and targeted medicine locally and immediately. UNIMEM enables shared memory resources and allows larger in-memory workloads as described in D4.8.
- 4. Energy.** Needs in term of improved safety and efficiency of the facilities (especially for nuclear plants) and also for optimising the overall energy infrastructure in order to reduce waste require a lot of monitoring and data collection. The smart grid approach strongly relies on the monitoring in real time of the users' needs in order to match offer with demand. In this type of systems a lot of data are generated and have to be processed in real time. To that respect EUROSERVER micro-servers will allow very efficient solutions with the right form factor in an energy budget capable of keeping competitiveness for the energy supplier operators. The COMPS system that models the energy requirements is described in D4.5 and assessed in D6.6.
- 5. Enterprise.** The demand for more and more accurate and pertinent data in enterprise is everywhere. For example:

  - Just taking into account our mailboxes, it is now gigabytes of data, which are flowing through them per month. Adding on top of this all the ERP systems and the huge amount of information generated inside and outside of the company, there is a huge demand for a never-ending amount of data to be stored and processed. Most of the companies are now limiting email capacity, for instance, because of the level of CAPEX but more because of the level of OPEX it represents. The approaches to dealing with efficient IO in EUROSERVER are described in D4.4.
  - The new business and technological scenarios created by the "Internet-of-Things" or "Smart-Environments" paradigms are creating an increasing demand of both distributed and centralised light-weight servers to manage the huge amount of data generated by sensors, devices and appliances. Since enterprise customers must be enabled to manage their portfolio of wired or wirelessly connected devices either through preconfigured web portals or existing back office systems, such new generation embedded servers with a suitable software stack can be considered as a crucial component of the modern concept of Enterprise infrastructure.

6. **Population aging.** There is a clear trend in trying to keep aging people at home in order to decrease health cost. This is strongly linked to the capacity of the various health systems to manage huge volume of data. Assuming 10Kbyte/day per person for the population above 65 this represents more than 200GBytes per day in 2020 that has to be stored and investigated every day. This estimation clearly excludes video, which if it has to be taken onto account, could lead to 100 to 1000 more data and then reach 200Tbytes per day. To that respect EUROSERVER can bring a real competitiveness in providing a solution allowing exploitation of all these data at a reasonable cost. This type of approach is absolutely mandatory for such ecosystem which is very fragmented and which needs very efficient solution in order to get a large adoption.

### *Industrial Impact*

EUROSERVER paves the way for making performance computing available to the applications, either remotely by increasing the data-centre capabilities, or even locally with embedded servers. In this respect, numerous industries can benefit from EUROSERVER innovations.

1. **Fundamental and applied research.** For instance the ATLAS detector, at CERN, with its millions of sensors generates more than a PBytes per second which needs to be stored and analyzed to allow progress in science in order to fuel industry innovation 10 to 15 years away from now. For sure regarding the energy need, for such a large instrument like Large Hadron Collider (LHC), storage is not the first line in term of electricity consumption. But this need of recording, monitoring and storing a lot of data is ubiquitous in a large number of research labs in Europe. For a large majority of them the computer infrastructure is becoming a very important level of OPEX which has to be taken into account very carefully in order to avoid a limitation in research activity in the future. EUROSERVER with its aggressive objectives of performance, energy consumption, and form factor can help to overcome such limitations and thus to keep Europe at the leading edge of research in a lot of domains.
2. **Automotive** for which for instance crash test needs to be improved with more accurate body and tissue modeling therefore leading once again to an explosion of the amount of data manipulated. Even inside cars there are now more and more devices which are connected that manage a large volume of data. To that respect and thanks to its aggressive objectives, EUROSERVER can bring innovative approaches allowing micro-server embedded solutions in cars.
3. **Smart Environments.** Physically a smart environment is a smart space populated by interconnected sensors, devices, and appliances with the capability to self-organise itself, and to provide services and complex data to the people/entities who physically traverse this space. Such smart space is usually fed by services provided by a hierarchical infrastructure of interconnected servers operating on-the-field and in data-centres. This scenario is changing the way new public and private infrastructures are built in many application domains from transportation to healthcare, from safety to utilities, etc. and, thanks to its holistic approach, EUROSERVER can significantly contribute with a cost-effective solution that can be used in all the layers of such application domains.

4. **Aeronautic.** The more and more accurate modeling of an aircraft in its environment and the addition of lot sensors on a plane generate once again a huge increase in volume of data. The management of most of these data has to be made on board and in real time. EUROSERVER with its aggressive low energy and dense processing performance can bring solution to this new challenge.

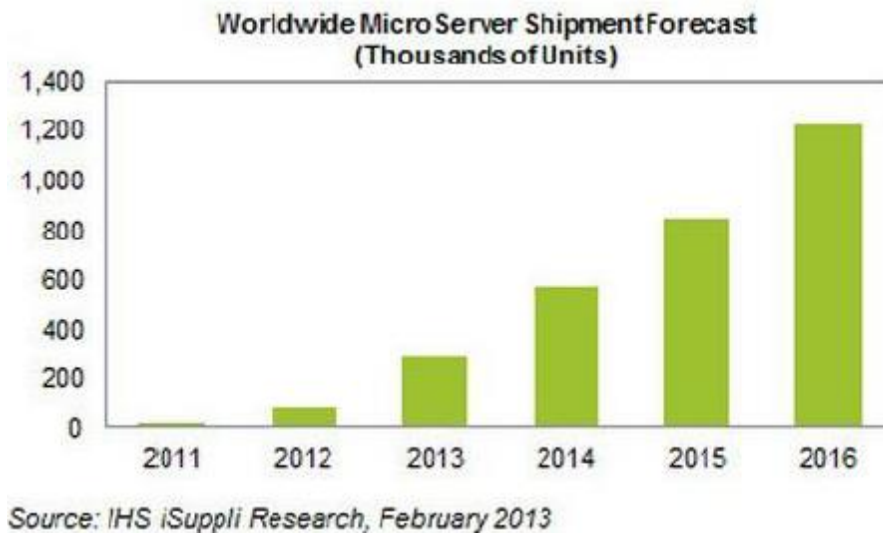
ST reports that EUROSERVER and the development linked to EUROSERVER (chiplet) have allowed discussion with major actors in the aeronautic domain (Thales, Safran, Airbus). The chiplet approach has been proposed in another project with embedded FPGA (DEMETER/ECSEL JU). Even if the Chiplet development has been stopped, embedded/large FPGA development in 28FDSOI for spatial and aeronautic application is continuing. New customer projects have been initiated with some key aeronautic actors, thanks to the EUROSERVER initiative

5. **Finance.** Algorithmic trading and deep financial technical analysis generate large amounts of data. For instance financial operators in London during the Olympic Games in 2012 had to find solution for data back-up in order to deal with potential electricity shortage.
6. **Telecom.** Cloud-Radio Access Networks (C-RAN), Software Defined Networks (SDN) and Network Function Virtualisation (NFV) are key enablers to address the demand for broadband connectivity with low cost and flexible implementations. Many crucial shortcomings affect today's networks, and must be addressed for successful 5G network deployments. These include: overly long provisioning times; reliance on proprietary, hard-to-modify and cost-ineffective hardware devices and components to meet capacity and performance targets; and the daunting complexity emerging from the need to converge a wide range of heterogeneous access technologies and multi-vendor network components. In order to tackle these challenges, flexibility and cloudification of the network components is inevitable. NFV proposes to implement network services as virtualised software applications running on commodity hardware. EUROSEVER micro-server architecture can significantly contribute to the deployment of virtual network functions within the cloud infrastructure.

## *Pathway to exploitation*

### **Opportunities for commercial exploitation**

EUROSERVER is tailored for a current window of opportunity: The \$50B USD server market is growing, as shown by the projection in Figure 1. Cloud segments are expected to grow dramatically.



**Figure 1: Worldwide micro-server shipment forecast**

Still, the enterprise server market dominates but has saturated, though the upcoming opportunities – Internet of things and “big data” – will likely sustain the growth. Within this market, micro-server (<45W and less complex server boards) shipments are expected to grow by a factor of 50 between 2011 and 2016 (HIS iSuppli).

The EUROSERVER strategy fits into the market trends:

- Technically, it is following research indications to match massive core-level parallelism.
- It aligns with the technology inflection point by offering highly optimised, low cost compute units.
- It leverages key innovations offered by tier-1 experts in server technology.

### Primary technological results to be reused by the partners

#### 1. Next Generation Compute System Architecture

The scale-out and scalable heterogeneous compute is a key outcome for ARM and ST. The memory model utilising a virtual-capable shared global address space completes the solution. This Architecture is also being used and further evolved by research partners in the follow-up projects ExaNoDe, ExaNeSt, EcoScale, and EuroEXA, with outstanding exploitation prospects there as well.

#### 2. Nanoscale Integration

The project leverages the integrated “chiplet” concept. EUROSERVER developed a new chiplet based architecture with integration into System-in-Package. This concept is currently improved for higher performance and smaller form factor with 3D integration of chiplets on active interposer in the follow-up H2020 project ExaNoDe.

#### 3. Software Architecture and Frameworks

This project was the first to prototype to demonstrate the “UNIMEM” memory hierarchy - a cornerstone for the follow-up projects and for upcoming exploitations. Resource sharing aspects of UNIMEM principles are already being commercialised by KALEAO Ltd. in its first product offering.

### **Kaleao Limited**

Kaleao is a privately funded startup company, incorporated with headquarters in the UK, and the USA, with research and development in Crete and Grenoble targeting hardware system solutions through their operations in Italy to the international enterprise server markets. This European structure has a close alignment with the founders joint associations within the EUROSERVER FP7 funded project. Although not a participant partner of the project, Kaleao is working with many of the EUROSERVER partners in realising a commercial exploitation of the key technologies and implementation prototypes that have been defined and created within the EUROSERVER project. Kaleao plans to have first products available to the market by the summer of 2016, of which will show an explicit exploitation of both the system architecture, contained technologies, and other industrial exploitation initiatives, as a result of the innovations of EUROSERVER and previous FP7 funded projects. Finally the target customer for the standalone PCB did not materialize in 2016, and since then Kaleao have been working on the full integrated product, which first customer orders will be fulfilled on or before the 28<sup>th</sup> April. Below are a few press releases about some of these first customers:

<http://www.channelbuzz.ca/2017/03/arm-based-hyper-converged-vendor-kaleao-enlists-vancouvers-tuangru-as-key-channel-partner-20791/>

<http://finance.yahoo.com/news/kaleao-axxonsoft-bring-solution-isc-130000652.html>

<http://www.realwire.com/releases/KALEAO-Partners-With-ILA-microservers-to-Bring-True-Convergence-to-Europe>

<http://finance.yahoo.com/news/kaleao-partners-network-allies-bring-130000210.html>

The Kaleao micro-server is a HW/SW integrated product using a compact cartridge based blade and chassis approach and a web scale system architecture that was co-designed with a unique new-generation of scale-out software platform while also maintaining compatibility and fully leveraging the broader application and services ecosystems for ARM-based servers such as Open-Stack and Juju Charms.

By using Kaleao’s innovative System-In-Package chiplet integration technology and the web-scale software-managed Kaleao-UNIMEM<sup>®</sup> machine architecture, it is possible to build solutions that fulfill all the requirements of a standard server through micro-server technology with the following additional features:

- **Low cost:** Web-scale, high-performance, multi-cores subsystems that can be aggregated in application-transparent, large and complex configurations.
- **Solution Configurability:** Thanks to the integration approach and to the use of reconfigurable hardware in all key IO interfaces
- **Extreme energy efficiency:** enabled by the dense and everything-close, hyper-converged design.

This approach makes the Kaleao value proposition unique to the enterprise and cloud server markets and enables key values to the customer through reduced cost, product flexibility and subsequent

competitiveness. Together this gives a commanding opportunity for Kaleao based solutions to be successful, even in presence of the traditional and other ARM micro-server players in this market.

Finally, the KMAX platform is available as an Appliance Edition through a commercial agreement with ONAPP makes their software solution available, pre-integrated on the KMAX server. This includes the key work from EUROSERVER by ONAPP through their Microvisor solution.

### **ZeroPoint Technologies AB**

ZeroPoint Technologies is a technology start-up company incorporated in 2015 and headquartered in Göteborg, Sweden with the mission of commercialising IP blocks for enhancing the performance of memory systems. Based on the innovative memory compression technology developed at Chalmers University of Technology, in the context of the EUROSERVER project, it is marketing MaxiMem™, a product family that can triple the memory capacity and the effective memory bandwidth. ZeroPoint Technologies AB has today a staff of about ten people and recently raised 1 M€ in funding.

The MaxiMem™ product family is based on an IP-block that implements highly-efficient memory compression algorithms. The IP-block interfaces to the processing unit, on the one side, and to the memory controller, on the other side.

It enables fast and lossless compression and decompression of data in main memory at the speed of the memory controller offering a tripling of effective memory capacity and bandwidth.

A first market targeted by ZeroPoint Technologies is FPGA acceleration in a number of areas including deep learning, financial prediction and in-memory databases to mention a few. By including a small IP-block next to the memory controller, the efficiency of FPGA acceleration can be improved substantially. For example, if the memory bandwidth is exhausted, MaxiMem™ can triple the performance by allowing three times more computational kernels to access memory.

The long-term goal is to offer ASIC versions of MaxiMem™ to be included in System-on-Chip solutions for the server and mobile computer market.

## **Exploitable results**

### ***Enablers***

#### **Hardware Prototypes**

The EUROSERVER project builds a compute reference board (Figure 2, Figure 3) that contains the required compute capabilities with the UltraScale+ FPGA, test and integrity test capabilities for possible Hybrid Memory Cube (HMC) and System-In-Package (SiP) integration. A fully assembled pair of EUROSERVER boards mounted in an assembly can be seen in Figure 4.

Both embedded and data centre designs can be quickly and efficiently turned around from the reference test board.

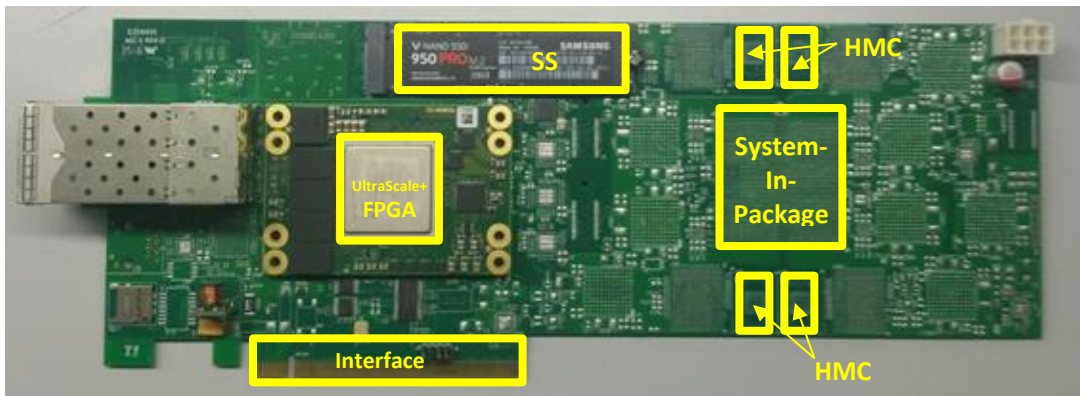


Figure 2 : EUROSERVER compute reference board



Figure 3: EUROSERVER - fully assembled board

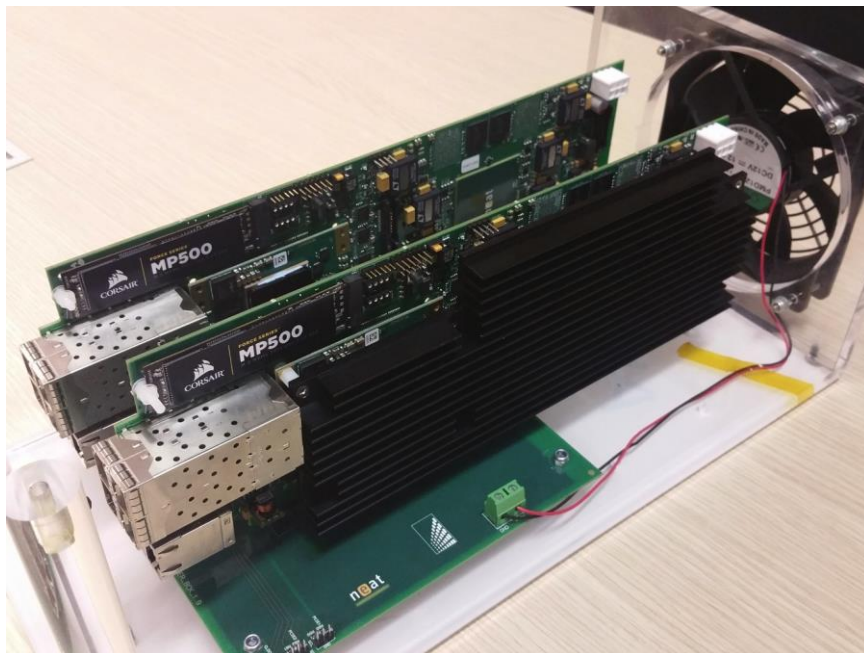


Figure 4: Fully assembled pair of EUROSERVER boards mounted in an assembly



The reference board has been designed as close as possible as a real product and thus enables the following exploitations:

- It may be used for customer trials by ST and NEAT.
- It can be used for alpha evaluation by the partners, and as demonstrators in industrial fairs and congresses.
- It can be used for prototyping HMC-based memory subsystem.
- It can be used for multi-board prototype design to scale-out UNIMEM concept.
- It can be used for development and evaluation of FPGA-based HW accelerators
- It can be used for the development of system and application software

### Software Studies and prototypes

The systems software stack of EUROSERVER introduces new technology at four layers:

- The native Linux OS
- The hypervisor  
ONAPP reports that new product offerings are being explored based on the MicroVisor and there are already some commercial agreements in-place related to the use of the MicroVisor.
- The runtime system and associated libraries
- The applications themselves with new applications in the domain of data center and CRAN

Earlier in the project, both the 32-bit Discrete Prototype and the 64-bit Juno-based Discrete Prototype had offered precious experience and testbeds to the partners of the project, to the ExaNeSt and ExaNoDe projects, and had served as initial guidance for Kaleao.

### Licensing

Each of these layers has its own innovations, as discussed in the corresponding deliverables. For exploitation purposes certain layers exhibit also certain limitations. The main limitation is that the native Linux kernel and the hypervisor have a GPL license. Therefore, code modifications in these systems are bound by the same license. The overall framework for releasing code and the different components of the systems software is:

- The native Linux OS, hypervisor:  
Patches and kernel modifications will become by necessity GPL. Loadable modules can use partner-specific licensing schemes.
- The runtime system and associated libraries:  
Here also, Partner specific schemes may be used as there is no limitation in the licensing scheme.
- The applications themselves with new applications:  
Here also, Partner specific schemes may be used as there is no limitation in the licensing scheme.

## Open source

Certain stack components will become open source, based on current partner discussions. For instance OnApp is planning to release as open source the extensions to Xen and FORTH the patches to the Linux kernel memory allocator.

## Software Prototype, results of WP4

The partners involved in WP4 have delivered a system software stack that is adapted for the EUROSERVER architecture. As such, the main use of the stack will be to demonstrate the validity of the research ideas and to be used for subsequent research. Individual partners are planning to feed results in their own infrastructure and plans. In some cases, device-driver-level software accompanies firmware IP blocks that are being licensed to spinoffs.

## *Program collaborations*

EUROSERVER provides a European foundation and ecosystem for scalable, low-power and low-cost approach for computing. Several subsequent H2020 projects in the area of “HPC Core Technologies” are aligned with EUROSERVER concept and further develop EUROSERVER technology:

- ExaNoDe (H2020-FETHPC-2014 - 671578): focuses on the delivery of the initial compute element for HPC application system deployment. Partners involved in ExaNoDe from EUROSERVER; CEA (lead), ARM, FORTH, BSC, Researchers from EUROSERVER/ARM at University of Manchester.
- ExaNeSt (H2020-FETHPC-2014 – 671553): focuses on the physical deployment (housing & cooling) supporting the required compute density along with its storage and interconnect services. Partners involved in ExaNeSt from EUROSERVER; FORTH (lead), Researchers from EUROSERVER/ARM at University of Manchester.
- EcoSCALE (H2020-FETHPC-2014 – 671632): focuses specifically on integrating and exposing the acceleration capabilities of FPGA's. Partners involved in EcoSCALE from EUROSERVER; Researchers from EUROSERVER/FORTH present at TSI (lead), STM, Chalmers, Researchers from EUROSERVER/ARM at University of Manchester.
- ACTiCLOUD (H2020 ICT-16-Cloud Computing - 732366): supports a collaboration between Kaleao and OnApp and others to further develop the capabilities of the KMAX product to address the challenges specific to cloud computing through development of federation and rack-scale management. This uses the KMAX, EUROSERVER based server as a development testbed.
- EuroEXA (H2020-FETHPC-01-2016 – 754337): this will be the continuation of the previous three projects, hence a “grand-child” of EUROSERVER (2017-2020). Forming the third in the sequence of projects in which UNIMEM forms the foundation of the memory model of this system. This selected project will deploy a large testbed in the push towards exascale level servers.

The EUROSERVER project has common participants across these various consortiums. Moreover, these H2020 projects are coordinated by EUROSERVER partners: CEA for ExaNoDE, FORTH for ExaNeSt. A researcher from FORTH who works on EUROSERVER with dual affiliations is leading EcoSCALE via TSI.

The consortium has organised a first workshop within the HiPEAC conference in January 2015 and a second workshop at the HiPEAC Conference in January 2017, and invited potential partners (more details in § Dissemination).

The consortium shared booths with these “associated” H2020 projects at DATE2016 (more details in § Dissemination).

EUROSERVER complements the portfolio of IT platforms in 5GPPP related projects such as SUPERFLUIDITY (H2020-ICT-2014-2-671566). SUPERFLUIDITY is focusing on enabling technologies and platforms for flexible virtualised 5G networks. SUPERFLUIDITY started in July, 2015. Partners from EUROSERVER involved in SUPERFLUIDITY include ONAPP and TUD.

### *Exploitation plans per partner*

This section describes the exploitation action plans for the partners that have identified potential exploitation activities. To systematically focus the exploitation efforts, a classification of different exploitation types has been devised, see Table 1.

**Table 2: Exploitation Types**

Number	Type	Description
1	New Business Product	Based on the work the project, partner develops IP in the form of software algorithms, components or software services, including hardware devices. Partner might reuse any EUROSERVER output as agreed in the CA and introduce a product as a commercial offering in the market place. This could be as existing partner or as a spin up/out.
2	New Business Service	Partner develops and provides a service to the relevant industry.
3	Additional Consultancy or Training Services	Partner develops their knowledge and offers consultancy or training services to industry therefore wins new business as a direct result of developing this capability.
4	Internal Exploitation	Partner develops internal capability and exploits the knowledge and methods developed within EUROSERVER.
5	Internal or External Influence	Partners are able to influence key stakeholders based on EUROSERVER results either internal to their organisations or external
6	Influence Standards	The EUROSERVER Consortium influences relevant industry standards.
7	Open Source	EUROSERVER develops and releases some of its results as software
8	Additional Research Funding	Winning additional research funding to pursue further research based on EUROSERVER results.
9	Achievement of Academic Qualifications	Leveraging EUROSERVER research to complete a MSc or PHD

## CEA

CEA-LETI has been designing hardware/software IPs and 3D integrated circuits for highly demanding applications, mainly in the embedded systems area. Within the EUROSERVER project, CEA-LETI will enlarge its scope to servers, enrich its technology portfolio.

Specifically, CEA-LETI will refine its expertise for on-chip system interconnect and inter node communication in the context of System-In-Package integration. CEA will gain new experience in server memory subsystems: the new memory technologies offer huge possibilities for building the future computing systems, and CEA will exploit its in-house technological expertise and work with the other partners to design the optimal memory IPs for on-chip caches, memories and memory controllers.

CEA is active in prototyping complex embedded systems, and this activity requires to maintain a portfolio of infrastructure IPs to be used for these systems. More precisely, EUROSERVER was an opportunity to cover the interconnection of ARM computing nodes with CEAs 3D NoC, preparing the way to 3D stacking of compute chiplet on Silicon interposer, as promoted by the ExaNoDe H2020 project where CEA is involved as coordinator and 3D-Integrated-Circuit design.

The project also offers the opportunity to work on a new communication IP to support Remote DMA. This innovative solution aims at providing a flexible way to establish efficient communication between user-space processes running different CPU of the System-on-Chip without the involvement of their respective OS kernel.

After the 3<sup>rd</sup> amendment, which implied many changes in hardware architecture as well as the postponed chiplet design, the CEA RDMA patented block integration was suspended, as well as the related tasks to inter-node communication and software OFED stack integration.

<b>Action ID</b>	CEA-01
<b>Action Type</b>	New business product
<b>Description</b>	License under-patent technology (sw/hw) for inter node communication (RDMA) to firms willing to use our scale-out node architecture.
<b>Goal/Opportunity</b>	Transfer research results to industry
<b>Priority</b>	High
<b>Likelihood</b>	High
<b>Parties Involved</b>	CEA, third parties
<b>Status</b>	On-going investigation, suspended with amendment#3.
<b>IP Issues</b>	None

<b>Action ID</b>	CEA-02
<b>Action Type</b>	Internal Exploitation
<b>Description</b>	Use systems software prototype of modified OFED RDMA stack for subsequent research activities.
<b>Goal/Opportunity</b>	Advance further the state of the art in research

<b>Priority</b>	High
<b>Likelihood</b>	High
<b>Parties Involved</b>	Different groups at CEA
<b>Status</b>	On-going investigation, suspended with amendment#3.
<b>IP Issues</b>	Deal with GPL restrictions of the OFED Open Fabric Alliance stack

<b>Action ID</b>	CEA-03
<b>Action Type</b>	Additional Research Funding
<b>Description</b>	Use IP and prototypes of EUROSERVER to address problems related to inter-node communication or I/O virtualisation.
<b>Goal/Opportunity</b>	Advance further the state of the art in research
<b>Priority</b>	Medium
<b>Likelihood</b>	High
<b>Parties Involved</b>	Different groups at CEA
<b>Status</b>	Investigation completed, no implementation yet
<b>IP Issues</b>	None

<b>Action ID</b>	CEA-04
<b>Action Type</b>	Achievement of Academic Qualifications
<b>Description</b>	PhD thesis : Hardware support for inter-process communication within a multi-core System on Chip
<b>Goal/Opportunity</b>	Research and training of highly qualified personnel
<b>Priority</b>	Medium
<b>Likelihood</b>	High
<b>Parties Involved</b>	CEA
<b>Status</b>	On-going (one thesis completed and one thesis on-going)
<b>IP Issues</b>	None

### STMicroelectronics

The initial exploitation foreseen by STMicroelectronics was mainly in the set-top box and micro server business. The major change in strategy, which happened in January 2016 change a lot the exploitation path. Nevertheless all the knowledge developed during EUROSERVER is now benefiting other internal project in other business domains.

- **Evolution of STB (Set-Top Box) Business.** A major change happened in STMicroelectronics strategy in January 2016 as the decision was made to stop the set-top box business. As such it became impossible to exploit some of the work made in EUROSERVER in this type of business. Nevertheless the experience acquired with EUROSERVER is reused in other business units such

as consumer, space-mission and defense. Unfortunately the confidentiality agreement signed with these customers does not allow STM to discuss the targeted applications.

<b>Action ID</b>	ST-01
<b>Action Type</b>	New Business Product
<b>Description</b>	Evolution of STB (Set-Top Box)
<b>Goal/Opportunity</b>	Exploitation of advanced FDSOI silicon technology.
<b>Priority</b>	Not applicable
<b>Likelihood</b>	Not applicable
<b>Parties Involved</b>	Different groups at ST
<b>Status</b>	Cancelled as Set-top Box business has been stopped
<b>IP Issues</b>	None

- **Validation of new technologies.** Even if there are no specific developments of very advanced new silicon technology in EUROSERVER, the design, manufacturing, testing and validation of multiple heterogeneous chiplets is a real challenge. To that respect EUROSERVER is intended at providing the right framework to allow validation of this new technology approach in order to allow later on an industrial deployment when needed. Even if it was not possible to develop a demonstrator, a lot has been learnt by ST within the scope of EUROSERVER and has been partially re-used in other application domains (space-technology and defense applications).

<b>Action ID</b>	ST-02
<b>Action Type</b>	New Business Service
<b>Description</b>	Maturation of new silicon technologies
<b>Goal/Opportunity</b>	Industrial demonstration vehicle
<b>Priority</b>	medium
<b>Likelihood</b>	medium
<b>Parties Involved</b>	Different groups at ST
<b>Status</b>	Stopped. Knowledge transfer ongoing
<b>IP Issues</b>	None

- **Definition of new architecture.** The initial objective of moving to multiple chiplet solution was strongly driven by set-top box application. The closure of this business line drastically reduced the need for this type of approach. Nevertheless it is still an approach which is being discussed internally in ST for other business applications but as of yet, there has been no decision of whether to proceed or not.

<b>Action ID</b>	ST-03
<b>Action Type</b>	Internal or External Influence

<b>Description</b>	New micro-server architecture
<b>Goal/Opportunity</b>	Complete development of an innovative solution
<b>Priority</b>	High
<b>Likelihood</b>	High
<b>Parties Involved</b>	Different groups at ST, ARM, EUROSERVER Academic partners
<b>Status</b>	Pending
<b>IP Issues</b>	None

• **Valorisation in networking domain.** A certain number of technological innovations are key for the networking domain. Among the most important ones we can underline:

- Integration of an HMC controller
- Prototyping of a scalable AXI extension
- SiP prototyping in view of cost reduction

These key features allow the definition of very performant systems providing differentiation for ST solutions.

<b>Action ID</b>	ST-04
<b>Action Type</b>	Internal or External Influence
<b>Description</b>	Key features for networking applications
<b>Goal/Opportunity</b>	This objective was linked to the set-top box business and is no longer relevant as the associated business operation has been closed.
<b>Priority</b>	Not applicable
<b>Likelihood</b>	Not applicable
<b>Parties Involved</b>	Business units interfacing with key players in networking solutions.
<b>Status</b>	Stopped
<b>IP Issues</b>	None

## ARM

ARM anticipated that the project will steer in a direction to deliver the design requirements and techniques required to enable ARM based platforms to be commercialized around the compute chiplet solution. Specifically, the logical and physical design requirements for the chiplet to interposer to I/O interconnect, the logical design structure and the associated standard software stack. Commercial priorities led to re-scope in the project to better align behind a silicon-modular approach, rather than pure 2.5D chiplet. The chiplet investigational work in furthering the roadmap for 2.5D chiplet is continuing, and is still anticipated in the future to be the technology of choice in the integration of heterogeneous silicon die within a single package.

<b>Action ID</b>	ARM-01
<b>Action Type</b>	Internal or External Influence

<b>Description</b>	New architecture for ARM-based devices
<b>Goal/Opportunity</b>	Integration Technology maturity, availability of new interconnect and IO solutions
<b>Priority</b>	High
<b>Likelihood</b>	High
<b>Parties Involved</b>	ARM, ST, LETI
<b>Status</b>	Pending technology and commercial alignment
<b>IP Issues</b>	None

A primary goal of the ARM compute unit is to provide a standard unit of compute for software. Standardisation of such compute units will accelerate and reduce the risk in the adaptation of compute into new markets while reducing the cost of entry and associated non-recurring design costs. Although, ARM has not announced any product in this area, however there are numerous activities across the ecosystem in which related technology approaches are being adopted. The foreseen general availability of such compute modules has not been forthcoming, and instead ARM external influence has led to the approach within other companies for the delivery of their product range. Currently public examples include the Marvell MoChi<sup>1</sup> and the Altera Stratix-10 Hyperflex<sup>2</sup>

<b>Action ID</b>	ARM-02
<b>Action Type</b>	New Business Product
<b>Description</b>	Development of a standard compute component
<b>Goal/Opportunity</b>	Improve market penetration for ARM64 product
<b>Priority</b>	High
<b>Likelihood</b>	High
<b>Parties Involved</b>	ARM, ST, NEAT
<b>Status</b>	Ongoing
<b>IP Issues</b>	None

With the holistic goals of the project to address the full software stack, as well as the fabrication techniques, the project will also enhance the ARM ecosystem to better address multiple markets. ARM will directly exploit the software efforts of the project to further enable the Open Source software ecosystem onto ARM based designs such as the ARM Generic Firmware and associated standardisation efforts around UEFI.

<sup>1</sup> <https://www.marvell.com/architecture/mochi/>

<sup>2</sup> <https://www.altera.com/products/soc/portfolio/stratix-10-soc/features.html>



Aligned with the project’s investigation into the requirement for RAS for servers, ARM subsequently released an update to the architecture specification<sup>3</sup> ARMv8.1, which has now been implemented in several server chips. This work also has direct external influence in the creation of the associated software stack through the work of Linaro<sup>4</sup>.

<b>Action ID</b>	ARM-03
<b>Action Type</b>	Internal or External Influence
<b>Description</b>	Development of a SW stack for ARM 64b compute
<b>Goal/Opportunity</b>	Develop ARM software ecosystem
<b>Priority</b>	High
<b>Likelihood</b>	High
<b>Parties Involved</b>	ARM, OpenSource community
<b>Status</b>	Ongoing
<b>IP Issues</b>	None

## NEAT

The expected main outcomes from the EUROSERVER project for NEAT are the identification of the key design rules and elements (technologies, components, architectures, processes) both required to design form-factor board level components that will enable the new class of micro-servers enabling new convergences between embedded computing and ICT.

NEAT consider the participation to the EUROSERVER initiative an important activity for many reasons:

- It helps to increase the company portfolio of technological skills and know-hows in high-end electronics that is crucial to increase the company competitiveness in the markets where NEAT is already present;
- It provides the company with the insight of new IPs that can be reused in current and future NEAT developments;
- It puts NEAT in touch with an important network of research organisations and industrial players that are currently defining the state-of-the-art of the electronics market in the computing domain.

Besides the indirect effects in terms of both increase of competitiveness and presence in the market resulting by the exploitation of the benefits described in the point above, the EUROSERVER\_project has a strategic value for NEAT, which, in fact, is currently defining a new business strategy that is explicitly addressing the use of micro server farm for execution of automatic massive testing of railway plants (millions of automatically generated and executed on thousands of processors).

<sup>3</sup> <https://community.arm.com/processors/b/blog/posts/armv8-a-architecture-evolution>

<sup>4</sup> <https://wiki.linaro.org/LEG/Engineering/Kernel/RAS>

<b>Action ID</b>	NEAT-01
<b>Action Type</b>	Internal or External Influence
<b>Description</b>	Identification of re-usable key components for micro-servers suitable for market seeding activities and customer presentations.
<b>Goal/Opportunity</b>	Leverage development effort, rationalise architectures
<b>Priority</b>	High
<b>Likelihood</b>	High
<b>Parties Involved</b>	NEAT and its customers
<b>Status</b>	NEAT is currently proposing architectures like the one designed and developed for the EUROSERVER projects and/or high-end components like the ones used on the EUROSERVER board to its customers in the mission & safety critical markets, where the demand for high performance computing platforms is raising.
<b>IP Issues</b>	None

Moreover such strategy is linked to a newly established company, Kaleao Ltd., addressing the world-wide micro-server market. Within this project NEAT will be the best candidate to support the product design and manufacturing activities thus re-using the know-hows and skills developed in the EUROSERVER project and transforming the EUROSERVER hardware and software platforms into product candidates after having negotiated the licensing of needed IPs with the consortium partners.

<b>Action ID</b>	NEAT-02
<b>Action Type</b>	New Product
<b>Description</b>	Optimisation of the EUROSERVER hardware and software platform and transformation in a product suitable for the micro server market.
<b>Goal/Opportunity</b>	Leverage development effort, exploit business opportunities
<b>Priority</b>	High
<b>Likelihood</b>	High
<b>Parties Involved</b>	NEAT and its partners
<b>Status</b>	NEAT has been one of the key-partners of Kaleao Ltd. in developing its new microserver products, leveraging the EUROSERVER project experiences.
<b>IP Issues</b>	None

## TUD

TUD has evaluated the EUROSERVER micro-server technology by running a Cloud RAN (CRAN) telecom applications. Results will be used to specify and further improve Cloud RAN software stack as well as hardware technology. Especially, energy efficiency and performance are regarded. It will strengthen the already available expertise at TUD in the developing leading edge baseband algorithms and suitable hardware. We plan to apply the expertise to improve base station design by using the energy efficient micro-server and provide prototypes to industrial partners. Furthermore, we plan to educate and

prepare students to develop telecommunication applications and their adaptations towards an efficient hardware implementation. The CRAN framework developed within EUROSERVER project will be exploited for further research within 5G Lab Germany. Moreover, TUD will look for the opportunity to startup company using the results of EUROSERVER project (Note that Vodafone Chair TUD successfully started 14 companies within 15 years in the wireless domain some of them acquired by Philips, NXP, Intel, National Instruments, Actix).

<b>Action ID</b>	TUD-01
<b>Action Type</b>	Achievement of Academic Qualifications
<b>Description</b>	PhD theses on novel radio access computing architectures and system management exploiting EUROSERVER general purpose nodes.
<b>Goal/Opportunity</b>	Research and training of highly qualified personnel
<b>Priority</b>	High
<b>Likelihood</b>	High
<b>Parties Involved</b>	TUD
<b>Status</b>	Completed (one thesis completed Oct-2015: Investigation of communications mechanisms in heterogeneous multi-processor systems) On-going (three theses on-going, defenses planned Sep-2017 and Dec-2017; one thesis interrupted for one year 2016-2017 due to maternity leave and the continuation and defense planned in 2018)
<b>IP Issues</b>	None

<b>Action ID</b>	TUD-02
<b>Action Type</b>	Achievement of Academic Qualifications
<b>Description</b>	Master thesis on scheduling dataflow applications on micro-server architectures
<b>Goal/Opportunity</b>	Research and training of highly qualified personnel
<b>Priority</b>	High
<b>Likelihood</b>	High
<b>Parties Involved</b>	TUD
<b>Status</b>	On-going (thesis defense on April-2017)
<b>IP Issues</b>	None

<b>Action ID</b>	TUD-03
<b>Action Type</b>	Internal or External Influence

<b>Action ID</b>	TUD-03
<b>Description</b>	Promotion of EUROSERVER results regarding CRAN protocol processing to network providers (NGMN) and base station manufacturers.
<b>Goal/Opportunity</b>	Contribution to the evolution of radio access architecture
<b>Priority</b>	Medium
<b>Likelihood</b>	Medium
<b>Parties Involved</b>	TUD
<b>Status</b>	Completed but continued activity presentations and demos at: Vodafone Innovation Days, NGMN Industry Conference & Exhibition, Vodafone ACDC Workshop Dresden, 5G Lab Germany, IEEE 5G Summit Planned demonstrations: DATE 3/2017, DAC 6/2017, IEEE 5G Summit 9/2017
<b>IP Issues</b>	None

<b>Action ID</b>	TUD-04
<b>Action Type</b>	Additional Research Funding
<b>Description</b>	Use CRAN framework of EUROSERVER to address tactile and industrial internet research area.
<b>Goal/Opportunity</b>	Advance further the state of the art in research
<b>Priority</b>	Medium
<b>Likelihood</b>	High
<b>Parties Involved</b>	TUD
<b>Status</b>	In Progress, Dataflow framework research and development continued in EU project Superfluidity (H2020-ICT-2014-2 – 671566). Started industrial research project (2016-2019) with National Instruments on the extension of EUROSERVER CRAN dataflow framework to heterogeneous computing platforms
<b>IP Issues</b>	None

<b>Action ID</b>	TUD-05
<b>Action Type</b>	Internal Exploitation
<b>Description</b>	Use EUROSERVER dataflow runtime system and CRAN applications for subsequent research activities and projects. Use of EUROSERVER guaranteed service interconnect and path allocation approaches to design scalable many-core architectures for wireless communications.

<b>Action ID</b>	TUD-05
	Development and integration of CRAN acceleration subsystem based on EUROSERVER specification and its integration with EUROSERVER dataflow framework. (Designed Tomahawk-4 MPSoC accelerator subsystem for CRAN applications - publication at DAC'2017)
<b>Goal/Opportunity</b>	Advance further the state of the art in research
<b>Priority</b>	High
<b>Likelihood</b>	High
<b>Parties Involved</b>	Different groups at TUD and 5G Lab Germany
<b>Status</b>	On-going
<b>IP Issues</b>	None

### BSC

Due to significant overlap between the data centre server and HPC architecture markets, it is in the strategic interest of BSC to participate in collaborative projects for data centre. HPC research has traditionally been at the forefront of computing, and techniques first invented for HPC have later appeared in servers; e.g. vector/SIMD, cache hierarchy, distributed memory and NUMA.

<b>Action ID</b>	BSC-01
<b>Action Type</b>	Achievement of Academic Qualifications
<b>Description</b>	PhD thesis on common secure virtualisation layer to support programming model and OS use cases enabled by UNIMEM
<b>Goal/Opportunity</b>	Research and training of highly qualified personnel
<b>Priority</b>	High
<b>Likelihood</b>	High
<b>Parties Involved</b>	BSC
<b>Status</b>	In Progress
<b>IP Issues</b>	None

<b>Action ID</b>	BSC-04
<b>Action Type</b>	Achievement of Academic Qualifications
<b>Description</b>	PhD thesis on interconnect energy proportionality and topology
<b>Goal/Opportunity</b>	Research and training of highly qualified personnel
<b>Priority</b>	High
<b>Likelihood</b>	High

<b>Action ID</b>	BSC-04
<b>Parties Involved</b>	BSC
<b>Status</b>	In Progress
<b>IP Issues</b>	None

The COMPSs framework allows portable, maintainable development of applications for grid and cloud computing, and we are keen to promote its wider adoption. It is therefore important to apply COMPSs to a wide range of application domains. In addition, the COMPSs framework is in use in production runs at the BSC, in the BSC private cloud (IaaS) and in our TOP500 cluster (MareNostrum).

<b>Action ID</b>	BSC-02
<b>Action Type</b>	Open source
<b>Description</b>	COMPSs framework developed for EUROSERVER will be released with Apache open source license. Supporting web applications and integration with VM manager are in the COMPSs 2.0 (November 2016) release. The energy scheduler will be included in the next release.
<b>Goal/Opportunity</b>	Contribution to open source software stack
<b>Priority</b>	Medium
<b>Likelihood</b>	High
<b>Parties Involved</b>	BSC
<b>Status</b>	In Progress
<b>IP Issues</b>	None

Early in the implementation of the project, we decided to cease development of and support for EMOTIVE Cloud (BSC's IaaS solution). We therefore focussed our efforts in the EUROSERVER project on enhancing OpenStack, a free open-source cloud computing software platform, to better support ARM-based platforms. We have developed the VM Manager, an open source component equipped with scheduling policies to optimise the placement of VMs and services in the provider's resources with regards to the energy efficiency metric. The VM Manager has been integrated with the OpenStack ecosystem. The VM Manager exploits the complexity and diversity of software applications with these policies.

<b>Action ID</b>	BSC-03
<b>Action Type</b>	Open source
<b>Description</b>	Energy-aware virtual machine scheduler will be released with open source licence
<b>Goal/Opportunity</b>	Contribution to open source software stack
<b>Priority</b>	Medium
<b>Likelihood</b>	High
<b>Parties Involved</b>	BSC

<b>Action ID</b>	BSC-03
<b>Status</b>	Completed
<b>IP Issues</b>	None

A power model based on the offline collection and processing of user-space available metrics with Machine Learning techniques has been developed by BSC. It is internally used by the VM Manager mentioned above to perform power forecasts when deciding the placement of VMs, although it can be used also standalone. The methodology and tools to generate it have been released with open source license.

<b>Action ID</b>	BSC-05
<b>Action Type</b>	Open source
<b>Description</b>	Methodology and tools to generate a power model will be released with open source license
<b>Goal/Opportunity</b>	Contribution to open source software stack
<b>Priority</b>	Medium
<b>Likelihood</b>	High
<b>Parties Involved</b>	BSC
<b>Status</b>	Complete
<b>IP Issues</b>	None

By means of the results from this project, BSC intends to position itself as a referent in the research topic of energy-aware management of data centers, thus allowing us to increase our collaborations with other research institutions, or to establish consultancy contracts with companies interested in deploying our management solutions in their infrastructures.

## **FORTH**

As a matter of general policy since its founding, FORTH-ICS promotes the commercial exploitation of R&D results by providing services, licensing products to industrial partners, contracting with industrial partners to jointly develop new products, and participating in spin-off companies and joint ventures. FORTHnet S.A., a spin-off company that FORTH-ICS created in the 90's, is today one of the major Internet Service Providers in Greece, and is quoted in the Athens Stock Exchange. In the last 10 years, the CARV Laboratory of FORTH-ICS, which carried out the EUROSERVER work at FORTH, had been involved in three spin-off / commercialisation efforts - among these, a subsystem in the storage software developed in FORTH, dealing with Solid-State-Disk (SSD) Caching, had been successfully commercialised, through a large international company.

In the case of EUROSERVER, FORTH-ICS/CARV has been strongly involved in the commercialisation activities via Kaleao Ltd. (UK):

- The first key contribution of EUROSERVER and FORTH to the Kaleao commercialisation was through the *training* of engineers and researchers: the main development lab of Kaleao is

currently in the Science and Technology Park of Crete (STEP-C), inside the Campus of FORTH, and its executive director as well as the majority of its staff were working at FORTH and in EUROSERVER before joining Kaleao; the training that they received in this project was centrally useful to the tasks that they now have to carry out at Kaleao.

- The second contribution is through FPGA firmware IP's and associated systems software that FORTH developed within EUROSERVER to be licensed to Kaleao, especially in the area of I/O and SSD sharing, now, as well as in other areas in the future.

More generally, and looking into the future, FORTH promotes the commercialisation of the IP that it has generated within EUROSERVER in the hardware and systems software architecture and implementation domain, with an emphasis around the UNIMEM concept and its powerful and very promising applications, via follow-up projects, Kaleao, and other opportunities. FORTH targets to commercially exploit several results that it has generated within EUROSERVER, as listed below. FORTH has also applied for a patent on this IP, as also listed below:

<b>Action ID</b>	FORTH-01
<b>Action Type</b>	Additional Research Funding
<b>Description</b>	Use IP and prototypes of EUROSERVER to further develop hardware and systems software solutions for micro-servers to be applied in multiple domains
<b>Goal/Opportunity</b>	Advance further the state of the art in research
<b>Priority</b>	High
<b>Likelihood</b>	100% (already in progress)
<b>Parties Involved</b>	CARV Laboratory of FORTH-ICS
<b>Status</b>	In progress, in the ExaNeSt and ExaNoDe FET-HPC projects, and forthcoming in the EuroEXA project.
<b>IP Issues</b>	None



<b>Action ID</b>	FORTH-02-HW
<b>Action Type</b>	New business product
<b>Description</b>	License Hardware IP blocks to firms like e.g. Kaleao Ltd.
<b>Goal/Opportunity</b>	Transfer research results to industry
<b>Priority</b>	High
<b>Likelihood</b>	100%
<b>Parties Involved</b>	FORTH, Kaleao, possibly others
<b>Status</b>	<p>Currently available IP blocks:</p> <ul style="list-style-type: none"> <li>• <i>Shared Ethernet NIC (and SSD)</i>: FORTH has designed and implemented a virtualised Ethernet NIC, which can be shared transparently in hardware by multiple OS or VMs running on the same or different coherence islands. While the current hardware design depends on Xilinx IPs, FORTH is planning to use only FORTH's IPs in future designs. Similar to the shared Ethernet NIC, FORTH is planning to provide an IP core for shared IO storage.</li> <li>• <i>Local-to-Global Address Translation</i>: FORTH has designed and implemented the first version of a local-to-global address translation and routing mechanism, which is used in order to provide Global Address Space in the system by routing remote memory accesses initiated by a coherence island to the appropriate destination (other coherence island) in the system. Next versions of the IP core will provide finer-grained translation schemes.</li> <li>• <i>Hierarchical Interconnect</i>: The current EUROSERVER routing infrastructure interconnects multiple instances of the Xilinx AXI interconnect. However FORTH is planning to design and implement its own energy-efficient hierarchical interconnect that will supersede the existing one. The new interconnect will support quality of service and multiple virtual channels.</li> <li>• <i>AXI-based Chip2Chip IP block</i>: FORTH has designed and implemented an AXI chip-to-chip IP core, which can bridge two devices over a 64-bit AXI4 interface and/or a 64-bit AXI Stream interface. The bridging function allows all AXI and AXI Stream channels to operate independently by forwarding per-channel data and control information in compliance with AXI per-channel Valid-Ready handshake. The current IP core supports two modes: one with 40 LVDS pairs physical interface and another with 20 LVDS pairs physical interface. Future designs will also support multi-lane high-speed serial physical interfaces.</li> <li>• <i>FMC Fan-Out daughter card</i>: FORTH has designed a daughter card that can be used to connect up to four Microzed boards<sup>5</sup>, four 10Gbit/s serial SFP+, and one 4-lane PCIe to a VITA-57 HPC FMC connector. This daughter card can be employed in order to build an A9 multi-core</li> </ul>

<sup>5</sup> <http://zedboard.org/product/microzed>

<b>Action ID</b>	FORTH-02-HW
	system consisting of multiple interconnected Microzed boards. There is no other similar daughter card available in the market today.
<b>IP Issues</b>	Some of the IP blocks are derivatives of IP blocks by Xilinx.

<b>Action ID</b>	FORTH-02-SW
<b>Action Type</b>	New business product
<b>Description</b>	License systems software layers to firms in the micro-server market
<b>Goal/Opportunity</b>	Transfer research results to industry
<b>Priority</b>	High
<b>Likelihood</b>	High
<b>Parties Involved</b>	FORTH, third parties
<b>Status</b>	<p>Currently available and under development items:</p> <ul style="list-style-type: none"> <li>• <i>IO Virtualisation Support</i>: FORTH has developed an Ethernet device driver for the aforementioned shared Ethernet NIC, which takes full advantage of the hardware assisted virtualisation support. Moreover FORTH will develop a device driver for the shared IO storage.</li> <li>• <i>Sockets over RDMA</i>: FORTH plans to provide a custom Sockets-over-RDMA library, which takes full advantage of the energy-efficient UNIMEM architecture, instead of the existing power-hungry Linux TCP/IP stack which consists both of a user-space component (part of the standard C library) and a substantial in-kernel subsystem. FORTH has already started working on the implementation of the Socket-over-RDMA library using the HW primitives provided by the EUROSERVER architecture.</li> <li>• <i>NUMA-aware linux on ARMv8</i>: While NUMA is supported by Intel-based servers, NUMA is not supported in ARM-based environments yet. FORTH is planning (in EUROSERVER and in subsequent projects) to be the first to port the NUMA Linux library onto ARMv8 taking advantage of the NUMA-like UNIMEM architecture.</li> </ul>
<b>IP Issues</b>	Deal with GPL restrictions of the Linux kernel

<b>Action ID</b>	FORTH-03
<b>Action Type</b>	Internal further Exploitation until ready for new business product
<b>Description</b>	Patent application in Congestion Management for Interconnection Networks
<b>Goal/Opportunity</b>	Advance further the state of the art in research with the goal of solving an important problem in real systems
<b>Priority</b>	High
<b>Likelihood</b>	Good

<b>Action ID</b>	FORTH-03
<b>Parties Involved</b>	CARV Laboratory of FORTH-ICS
<b>Status</b>	<p>Within WP3, FORTH has defined and simulated a novel method for dynamic (source) rate regulation that is appropriate for low-cost implementation in hardware and for low-latency reaction to changing traffic characteristics. It only requires <i>per-flow</i> hardware in the sources (e.g. DMA engines for EUROSERVER), while inside the network the hardware used does <i>not</i> need any per-flow state. Rates are regulated according to the well-known and highly desirable max-min fairness (MMF) criterion, which is highly efficient in its use of available network bandwidth, highly dynamic in nature, and fully fair. FORTH has filed a provisional (24 Sep. 2014) and then a full (24 Sep. 2015) patent application on this novel method:</p> <ul style="list-style-type: none"> <li>• "<i>Dynamic Max-Min Fair Rate Regulation Apparatuses, Methods and Systems</i>": USPTO Provisional Patent Application Number 14/864,355; filed on 24 September 2015 – priority date 24 Sep. 2014; publication number US 2016/0087899 A1. International application, to the PCT (via the EPO): application number PCT/EP2015/072048.</li> </ul> <p>See: <a href="https://patents.google.com/patent/US20160087899A1/en">https://patents.google.com/patent/US20160087899A1/en</a></p>
<b>IP Issues</b>	Pending patent application; no examination results received yet

<b>Action ID</b>	FORTH-04
<b>Action Type</b>	Achievement of Academic Qualifications
<b>Description</b>	Bachelor, Master and PhD theses in efficient and transparent user-space inter-process communication and other EUROSERVER topics
<b>Goal/Opportunity</b>	Research and training of highly qualified personnel, so that they become available for further R&D projects as well as for industrial work in the area (including at the Kaleao Crete Development Lab).
<b>Priority</b>	High
<b>Likelihood</b>	One (1) PhD, two (2) Master's, and five (5) Bachelor's Theses completed
<b>Parties Involved</b>	FORTH, University of Crete
<b>Status</b>	See list in section "Education and training"
<b>IP Issues</b>	None

## CHALMERS

<b>Action ID</b>	CHAL-01
<b>Action Type</b>	New business product
<b>Description</b>	<p>Licensing of memory compression technology to firms that will enter the micro-server market.</p> <p>Specifically,</p>

	<ul style="list-style-type: none"> <li>• Chalmers is developing a memory compression technology within the EUROSERVER project that promises to use memory resources 3X more efficiently which can yield substantial increase in cost-performance and energy efficiency for micro-servers. This memory compression technology, developed within the EUROSERVER project, has been disseminated to a number of key companies engaged in EUROSERVER technologies at international scale.</li> <li>• Chalmers is collaborating with FORTH to align this technology to the virtualisation technology that will be offered in the EUROSERVER project.</li> <li>• Chalmers contribution of HyComp has been disseminated in the IEEE/ACM International Symposium on Microarchitecture (MICRO 2016).</li> <li>• Chalmers contribution of HyComp has led to an article submitted for consideration to the IEEE Top Picks in Computer Architecture, 2015.</li> <li>• Two project members have participated in a custom discovery workshop based on the business canvas model to verify assumptions regarding value proposition, potential markets, and business models to commercialise the technology.</li> <li>• Chalmers has been granted a national project (from VINNOVA) to explore commercialisation opportunities of its memory compression technology.</li> <li>• A spinout company with the purpose of commercialising the IP, ZeroPoint Technologies AB, has been incorporated in Sweden with an exclusive license agreement to the inventors at Chalmers.</li> <li>• Based on the potential of the memory compression technology, ZeroPoint Technologies AB has attracted more than 1MEuro in investments for its commercialisation.</li> <li>• Eight patents have been filed to secure a unique position.</li> <li>• ZeroPoint Technologies have made many visits with potential customers including Google, Facebook, Intel, nVIDIA, Samsung and Qualcomm with keen interest in the technology.</li> </ul>
<b>Goal/Opportunity</b>	Transfer research results to industry
<b>Priority</b>	High
<b>Likelihood</b>	High
<b>Parties Involved</b>	CHAL, ZeroPoint Technologies AB
<b>Status</b>	In progress
<b>IP Issues</b>	Exploration of license and protection policy

## ONAPP

OnApp is a public cloud infrastructure provider that builds and provides a cloud software platform solutions based on multiple layers of cloud services. OnApp solutions enable providers to stay profitable and competitive by launching their own unique Cloud, Storage or CDN services, quickly, easily and cost-effectively. The main product is a platform that allows users to control and manage their own cloud services in a simple way.

“OnApp Cloud Product is understood to have the most paid deployments in production, with a claimed 900, followed by CloudStack, CA AppLogic and VMware” - 451 Research.

OnApp CDN Product - 172 Points of Presence in 113 cities across 43 countries.

The OnApp Federated Market was released as an alpha version as part of OnApp version 3.2 in Q1 2014. In Q3 2014, OnApp acquired SolusVM to add 2000 providers to the Federation Marketplace.

As part of the exploitation plans described below, OnApp intends to make the technologies developed as part of EUROSERVER available to its customers.

OnApp will strongly promote the micro-server vision proposed in EUROSERVER through the development of the Microvisor architecture. By developing software that will work with existing software products and also new products, OnApp will promote micro-servers in general by offering new technologies to its large, global, public hosting customers, offering an alternative to standard x86 servers on offer currently.

OnApp will work with ARM and the other partners in EUROSERVER to promote the adoption of low-power, energy efficient hardware designs that use multiple distributed cores to provide improved system-level efficiency and lower power usage for typical workloads.

<b>Action ID</b>	OnApp-01
<b>Action Type</b>	New Business Products / New services
<b>Description</b>	New product(s) and/or upgrades to existing products for public cloud service providers, based on micro-server architecture support.
<b>Goal/Opportunity</b>	Improved performance for micro-server type systems (e.g. low power, low resource cores) by reducing Dom0 overhead.
<b>Priority</b>	High
<b>Likelihood</b>	High by the end of project
<b>Parties Involved</b>	OnApp – Core and Emerging Product Teams.
<b>Status</b>	Prototype / proof of concept Update 2015-05-27; No Change Update 2015-11-16; Probability changed to high for end of project, due to increase in length of project by 5 months and also increased commercial interest. Update 2017-02-16; Commercial agreement to use the software on one version of the Kaleao integrated KMAX solution. (Commercial ready)
<b>IP Issues</b>	Developed by OnApp so none foreseen

<b>Action ID</b>	OnApp-02
<b>Action Type</b>	New and updated Business Products / New services
<b>Description</b>	Enabling virtualisation platforms to use energy metrics that are provided from hardware and improving UI features, will allow dynamic workload migration to hardware in order to improve the overall power efficiency of the data centre (e.g. to enable automatic power down of certain parts of the data centre when idle).
<b>Goal/Opportunity</b>	Power-aware workload distribution in public cloud hosting DCs
<b>Priority</b>	Medium/High Low/Medium
<b>Likelihood</b>	Medium/High
<b>Parties Involved</b>	OnApp – Core and Emerging Product Teams. FORTH, BSC.
<b>Status</b>	Research / Discussion stage Update 2015-05-27; Lowered priority Update 2015-11-15; Have spoken with a number of power vendors (EATON, Server Tech, Emerson) for rack scale APIs. It now looks like more vendors are going the API approach, but likelihood remains the same. Update 2017-02-16; The RAPL scripts that are used for Intel power analysis have been used for prototype work. Incomplete.
<b>IP Issues</b>	UI features will be limited to OnApp product but the algorithms and heuristics will be platform independent and open such that other platforms can develop based on the ideas.

In a report in 2007, EPA estimated that data-centre consumed about 61B kWh of electricity in 2006-equivalent to 1.5% of total US electricity consumption. In a report by Maki Consulting of the Data Center Alliance presented at the DG Connect workshop (Environmentally sound Data Centres: Policy measures, metrics, and methodologies) this figure in 2014 has reached 2% globally. Reducing idle servers and increasing the effectiveness of idle servers is seen as one way of increasing data centre efficiency. Exploitation activity - OnApp-02 – looks to improve on the state of the art.

<b>Action ID</b>	OnApp-03
<b>Action Type</b>	New and updated Business Products / New services
<b>Description</b>	Data centre infrastructure management as described in OnApp-02 will be assisted with improved distribution and management of VM resources at large scale within the data centre. Through better management tools, CIOs and data centre managers will have improved visibility of the whole system and be able to manage resources more efficiently.
<b>Goal/Opportunity</b>	Large scale VM distribution and management using lightweight Microvisor clustering
<b>Priority</b>	Medium/High

<b>Likelihood</b>	Medium/High
<b>Parties Involved</b>	OnApp, FORTH, BSC.
<b>Status</b>	<p>Early</p> <p>Update 2015-05-27; No Change</p> <p>Update 2015-11-16; There are more commercial requests for DCIM type integrations and as such the priority is increased to medium/high.</p> <p>Update 2017-02-16; Initial work carried out in scope of EUROSERVER is now being continued in SUPERFLUIDITY and is in a mature state but not commercially released.</p>
<b>IP Issues</b>	UI features will be limited to OnApp product but the algorithms and heuristics will be platform independent and open such that other platforms can develop based on the ideas.

<b>Action ID</b>	OnApp-04
<b>Action Type</b>	Internal Exploitation
<b>Description</b>	Expertise and knowledge in the micro-server space will be fed into other parts of OnApp, allowing for promotion of the ideas company wide. Power awareness and energy efficiency will then start to be added to the relevant roadmaps. With new products this will then lead eventually to marketing and sales around the micro-server vision as proposed by EUROSERVER.
<b>Goal/Opportunity</b>	Promote low energy, high-efficiency micro-servers internally to OnApp
<b>Priority</b>	High
<b>Likelihood</b>	High
<b>Parties Involved</b>	OnApp – Emerging Technology, Management, Sales, Marketing Teams
<b>Status</b>	<p>Early stage – ideas proposed. Some knowledge of the systems is being disseminated internally.</p> <p>Update 2015-05-27; Members of Emerging Technology team are being involved in Microvisor development. Discussion of Microvisor at company strategy and policy level.</p> <p>Update 2015-11-16; One extra team member working on OpenStack integration to allow Microvisor to be exposed.</p> <p>Update 2017-02-16; Extra team members working on OpenStack integration and UI (also for OnApp-03). Intel joint marketing solution that has four nodes in a more power-efficient layout is available via <a href="https://onapp.com/intel">https://onapp.com/intel</a></p>
<b>IP Issues</b>	N/A

<b>Action ID</b>	OnApp-04b
<b>Action Type</b>	Internal Exploitation

<b>Action ID</b>	OnApp-04b
<b>Description</b>	Related to OnApp-04. Caching has been worked on in the context of EUROSERVER to improve performance access to thinly provisioned resources via the Microvisor platform.
<b>Goal/Opportunity</b>	Promote technology re-use in existing technologies/products
<b>Priority</b>	High
<b>Likelihood</b>	High
<b>Parties Involved</b>	OnApp – Emerging Technology, Management, Sales, Marketing Teams
<b>Status</b>	Update 2015-05-27; New exploitation activity. Work on caching is ongoing and being merged into Integrated Storage Product and Microvisor Platform. Update 2015-11-16; Dev work related to caching has been completed and is now being prepared for QA Update 2017-02-16; Fully released into mainline storage product as of June 2016.
<b>IP Issues</b>	N/A

<b>Action ID</b>	OnApp-04c
<b>Action Type</b>	Internal Exploitation
<b>Description</b>	Related to OnApp-04. Storage I/O performance has been worked on in the context of EUROSERVER through the research and development of ATAOE technology. Removing performance overhead of networking stack for small packet forwarding that limits current storage platforms. This will be integrated into Integrated Storage product.
<b>Goal/Opportunity</b>	Promote technology re-use in existing technologies/products
<b>Priority</b>	High
<b>Likelihood</b>	High
<b>Parties Involved</b>	OnApp – Emerging Technology, Management, Sales, Marketing Teams
<b>Status</b>	Update 2015-05-27; New exploitation activity. Work on ATAOE is ongoing and being merged into Integrated Storage Product and Microvisor Platform. Update 2015-11-16; ATAOE is now integrated into the backend storage controllers. Currently we can only address individual end-points so more work is required here to get a fully-featured platform. Update 2017-02-16; Integrated into Microvisor work that has a commercial solution ready, see OnApp-01.
<b>IP Issues</b>	N/A

<b>Action ID</b>	OnApp-05
<b>Action Type</b>	Open Source



<b>Action ID</b>	OnApp-05
<b>Description</b>	<p>Data centre infrastructure management as described in OnApp-02 will be assisted with improved liquidity of VM resources within a coherent system and also throughout the data centre. Through better management tools, CIOs and data centre managers will have improved visibility of the system and be able to manage resources more efficiently.</p> <p>OnApp have been in communication with the Xen community via mailing lists and also attendance of Xen Hackathons and are working to provide the source code changes for the Zedboard / MicroZed ARM A9 platforms to the Xen community.</p>
<b>Goal/Opportunity</b>	Releasing extensions to Xen community for Discrete Prototype hardware. Promotion of ideas of EUROSERVER to the Open Source community
<b>Priority</b>	High
<b>Likelihood</b>	High
<b>Parties Involved</b>	OnApp, FORTH
<b>Status</b>	<p>Establishing links with community and providing source code</p> <p>Update 2015-05-27; Xen-PV port originally from Samsung modified by OnApp and uploaded to xenbits as part of open source plan.  <a href="http://xenbits.xen.org/gitweb/?p=people/julianchesterfield/xen.git;a=summary">http://xenbits.xen.org/gitweb/?p=people/julianchesterfield/xen.git;a=summary</a></p> <p>OnApp attended/participated at Xen Hackathon (May 29<sup>th</sup>-30<sup>th</sup> 2014, Rackspace, London)</p> <p>Update 2015-11-16; For UI integration, work has been performed on integration with OpenStack that is OpenSource.</p> <p>Update 2017-02-16; OnApp attended/participated at Xen Hackathon (18-19 April 2016 at ARM in Cambridge). Further work promoted via OnApp opensource – accessible via OnApp webpage.</p>
<b>IP Issues</b>	Features developed by OnApp have been provided as agreed with WP leads, FORTH. Further technology developments provided in collaboration with other partners may pose IP challenges.

<b>Action ID</b>	OnApp-06
<b>Action Type</b>	Additional research funding
<b>Description</b>	<p>A large amount of experience and training has resulted already from working on EUROSERVER. It is envisaged that this will lead to new and updated products as described in other exploitation activities.</p> <p>By working on the products, new ideas and possible collaborative efforts may be planned.</p>
<b>Goal/Opportunity</b>	Using the knowledge and experience gained through EUROSERVER, work on extensions of the ideas proposed through secondary projects or new proposed projects in the area.
<b>Priority</b>	Low/Medium

<b>Action ID</b>	OnApp-06
<b>Likelihood</b>	Low/Medium
<b>Parties Involved</b>	OnApp + Other interested partners
<b>Status</b>	<p>Ongoing</p> <p>Update 2015-05-27; Microvisor development will likely continue and be used in Superfluidity Project (H2020-ICT-2014-2 – 671566). Two proposals that are under consideration by EC also propose to leverage Microvisor technology - ' CANTO ICT-04-2015, Customised and low power computing (Research and Innovation Action)' and 'SERFER ICT-30-2015, Internet of Things and Platforms for Connected Smart Object'.</p> <p>Update 2015-11-16; Project CANTO was rejected (14<sup>th</sup> August, 2015) Project SERFER was rejected (14<sup>th</sup> August, 2015)</p> <p>New project proposal is starting that will be prepared for April 2016 (currently un-named)</p> <p>Update 2017-02-16; Project ACTiCLOUD that involves some participants of EUROSERFER consortium was accepted and started in January 2017</p>
<b>IP Issues</b>	None – Future work

### Patents & IP issues

Partner	Title	Patent application number	Date	Comment
FORTH	<p>"Dynamic Max-Min Fair Rate Regulation Apparatuses, Methods and Systems"</p> <p><a href="https://patents.google.com/patent/US20160087899A1/en">https://patents.google.com/patent/US20160087899A1/en</a></p>	<p>USPTO Provisional Patent Application Number 62,054,866 Regular (non-provisional) Application Number 14864355 and to the PCT (via the EPO) (application number PCT/EP2015/072048)</p>	<p>September 24<sup>th</sup>, 2014</p> <p>September 24<sup>th</sup>, 2015</p>	<p>MMF-Rate Congestion Management</p> <p>Status: pending</p>
CEA	<p>"Procédé d'exécution d'une requête d'échange de données entre des premier et deuxième espaces d'adressage physiques disjoints de circuits sur carte ou puce" / "Methods and apparatus for data exchange between two systems without any common physical address space"</p>	<p>N° E.N. : 15 51012</p> <p>Publication n :WO2016128649</p> <p>N° FR3032537</p>	<p>February 2<sup>nd</sup>, 2015</p> <p>February 2<sup>nd</sup>, 2016</p> <p>FR priority demand on</p>	<p>Analysed by INPI (French National Institute of Industrial Property)</p> <p>Demand of international extension of the patent</p>

Partner	Title	Patent application number	Date	Comment
			February 9 <sup>th</sup> , 2016	
CHALMERS	<i>"Methods, Devices and Systems for Data Compression and Decompression"</i>	Swedish Patent with the application number 1550644-7	May 21 <sup>st</sup> , 2015	Pending, National
CHALMERS	<i>"Methods, devices and systems for data compression and decompression"</i>	PCT/SE2016/050462	May 21 <sup>st</sup> , 2015	Pending, International
CHALMERS	<i>"Methods, devices and systems for data compression and decompression"</i>	PCT/SE2016/050463	May 21 <sup>st</sup> , 2015	Pending, International
CHALMERS	<i>"Methods, devices and systems for data compression and decompression"</i>	1650767-5	June 1 <sup>st</sup> , 2016	Pending, Swedish
CHALMERS	<i>"Variable-sized symbol entropy-based data compression"</i>	1650426-8	April 2016	Pending, Swedish
CHALMERS	<i>"Methods, devices and systems for decompressing data"</i>	1650119-9	January 29 <sup>th</sup> , 2016	Pending, Swedish
CHALMERS	<i>"Methods, devices and systems for compressing and decompressing data"</i>	PCT/SE2017/050074	January 27 <sup>th</sup> , 2017	Pending, International
CHALMERS	<i>"Methods, devices and systems for compressing and decompressing data"</i>	PCT/SE2017/050078	January 30 <sup>th</sup> , 2017	Pending, International

## Dissemination strategy

A summary of the dissemination activities is listed in Table 3.

**Table 3: Overview of the dissemination and exploitation activities**

Objectives	Activities
To disseminate generally understandable information about the project idea, approach and results	<ul style="list-style-type: none"> <li>- Public website, including press release and project abstract</li> <li>- Brochure, various presentations</li> <li>- Electronic newsletters</li> <li>- Attending events related to the outcomes of EUROSERVER</li> </ul>
To interact with stakeholders, other researchers in the field and the general public	<ul style="list-style-type: none"> <li>- Wide dissemination on the website of the public deliverables, jobs offers, potential collaborations, news, etc.</li> <li>- Submitting collaborative, peer-reviewed publications and depositing them into an online repository, making efforts to ensure open access within 6 months after publication</li> <li>- Careful and strategic revision of the plan for the use and dissemination of foreground</li> <li>- Electronic newsletters</li> <li>- Participate and publish articles at relevant, top-tier conferences, such as Usenix ATC, ASPLOS, EuroSys, MICRO, OSDI, SOSP</li> <li>- Presentation and demonstration of prototypes in supercomputer events, i.e., ISC – June, Europe, and Supercomputing – November, US. in partner booths.</li> </ul>
To push scientific and technological innovations for uptake by market actors, increase the acceptability of understanding for uptake by market actors, increase the acceptability of understanding of the field	<ul style="list-style-type: none"> <li>- Dissemination of confidential and restricted deliverables having a direct potential use for end-users and other stakeholders (following protection of results and signature of non-disclosure agreements)</li> <li>- Business-to-business communication in dedicated end-user magazines.</li> <li>- Disseminating project results at working groups and strategic committees beyond the consortium.</li> </ul>

The first step of the dissemination plan has been to design and build the project website ([www.euroserver-project.eu](http://www.euroserver-project.eu)) which plays a major role in informing public awareness and opinion. It details the project objectives, its partners and its results. The website also displays the required brochure and poster and the updates on the results of publicly shared deliverables. Regular editions of the project brochure and flyers are provided to partners for distribution at trade fairs, conferences and other meetings.

The partners disseminate the findings of EUROSERVER to the scientific and industrial communities through traditional channels including follow-on press releases, peer-reviewed publications, and specialised websites and participating in well-known scientific conferences.

Through the WP7 activities associated with the creation of specification documentation, the commercial participant associated with the IP and design of associated devices will be able to build on the ARM ecosystem to further broaden the attractiveness of EUROSERVER technology based design. This market pull will in turn extend the market opportunity for the initial participants of the project through their time to market advantage and experience in developing such solutions.

To monitor and evaluate the effectiveness of communication and dissemination activities within EUROSERVER, a set of data will be collected and analyzed. All project partners will contribute. The table below is a synthesis of the definition of data to collect together with the target figures.

**Table 4 : Dissemination metrics and target**

Description	Measure	Target
International events (fairs)	Name, date and location of events What was presented (prototype, presentation, poster...)	Embedded World Conference (Nuremberg - DE) International Supercomputing Conference (Leipzig - DE) Cloud Computing Expo (Santa Clara - US)  Supercomputing (USA) NGMN Industry Conference & Exhibition (Frankfurt) IEEE 5G Summit (Dresden) MPSoC Forum (Ventura) HiPEAC
Scientific conferences	Number of papers produced that were submitted to a scientific conferences Number of papers accepted	<u>Application</u> : ICDCS, IEDM <u>Circuit design</u> : DAC, DATE, GLVLSI, ISSCC, CCECE, ESSIRC/ESSDERC, 3DIC, Coolchips,  <u>Embedded</u> : DATE, ESWEEK, HiPEAC, SOC  <u>HPC</u> : ACM TACO / HiPEAC, ACM ICS, UCC, ACACES, HPCA, ISC, ISCA, LCN, Euromicro, ICPADS  <u>Storage</u> : MSST, FAST, ISSCC <u>System Architecture</u> : ACM TACO, HiPEAC, DSN, ISCA, MICRO, HPCA, ICS, ASPLOS, Usenix ATC, MSST, ANCS, ASAP  <u>OS</u> : EuroSys, ASPLOS, OSDI, SOSP
Dedicated workshop	Number of people actively participating	A specific EUROSERVER workshop will be organised during the last year of the project to present the project achievements and to discuss the beyond state of the art topics.

Description	Measure	Target
Journal Publications	Number of papers produced and submitted Number of papers accepted	ACM Tran. on Architecture & Code Optimisation (TACO), IEEE Tran. on Computers (TC)
Project web site	Number of visits Number of requests for further information	The website will display the required poster and also updates on the results of publicly shared deliverables
Press releases	Number of press releases issued Number of media inserts Number of individual press impacts	

## Project Image

### Logo

The main image of the project is the design of the logo presented below.



Figure 5: project logo

The logo image was designed to suggest a stylised version of a manycore server, while the colour green was chosen to reflect the sustainability and energy-saving objectives of the project. The font was chosen to give the text a clean, modern feel. This branding will be applied across the dissemination channels of the project, including the website, press releases and any material produced to publicise events. This logo has been approved by all EUROSERVER partners.

### Project Templates

Project templates for deliverables and PowerPoint presentations are available under the project repository.

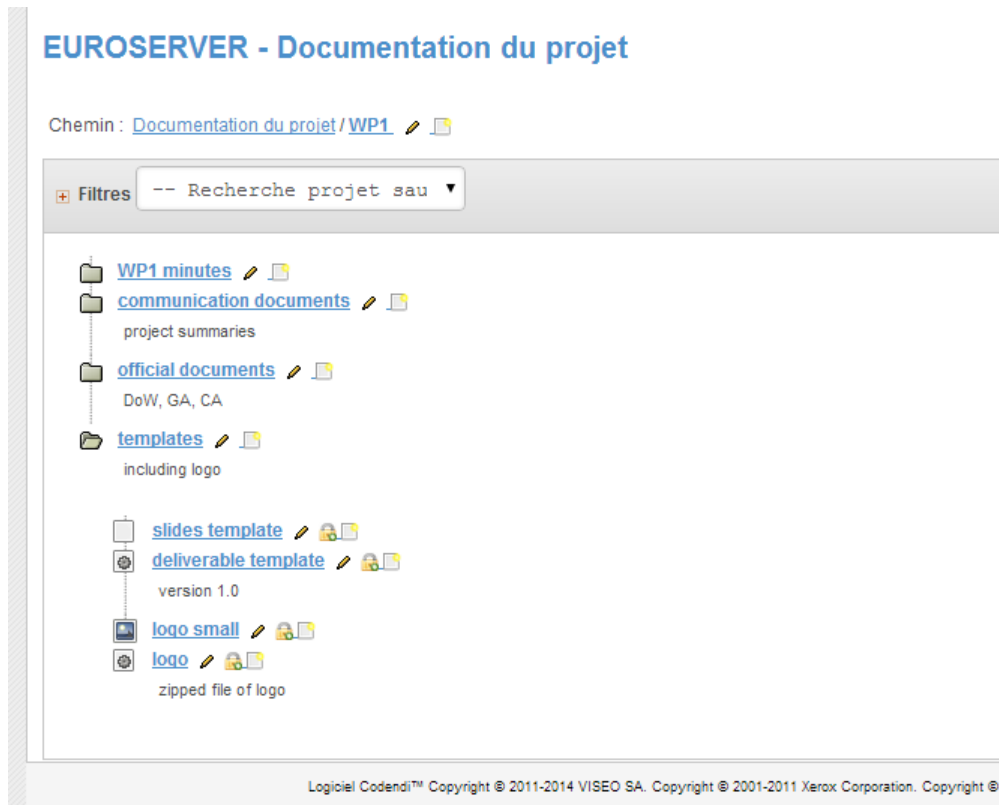


Figure 6: project templates available in the WP1 folder

### Publication acknowledgement sentence

When appropriate, following acknowledgment paragraph should appear in the text of journal papers or conference proceedings:

This research project is supported by the European Commission under the 7th Framework programme under the “Information and Communication Technologies” theme, with grant number 610456.

### *Management of Intellectual Property Rights (IPR) for dissemination*

The detailed terms, rights and responsibilities of the partners concerning intellectual property are detailed in the Consortium Agreement.

However, dissemination of the foreground will be carried out as swiftly as possible. Nevertheless, special efforts will be made so that dissemination doesn’t endanger the protection and use of the foreground (IP) by partners in line with the confidentiality clauses of the Consortium Agreement, all project results will be considered confidential at first. Partners who would like to disseminate research results will transmit a summary to all partners prior to the expected dissemination date as *defined in the Consortium Agreement*. *Any partner can raise an IPR issue concerning the summary of research results.*

## External website

The project website plays and will play a major role in informing public awareness and opinion. It details the project objectives, its partners and its results. The website will displays the required poster and also updates on the results of publicly shared deliverables.

- ▶ The website <http://www.EUROSERVER-project.eu/> has been active since Feb. 2014. Its first version contained basic information, and as yet no deliverable or foreground information. It has been updated and revisited in terms of design and contents since June 2015. It presents the project (Figure 7), details the main characteristics (Figure 8), the partners, etc.
- ▶ All public deliverables are now available on the website, as well as posters, videos and pictures. The website is regularly updated with new information, bringing into relief the current event (Figure 9).
- ▶ The *Results* section on the front page highlights on the one hand the creation of the two start-ups related to EUROSERVER results, Kaleao and ZeroPoint Technologies. Links to H2020 associated projects such as ExaNoDe, ExaNeSt, ECOSCALE and EuroEXA are pointed out (see Figure 7).

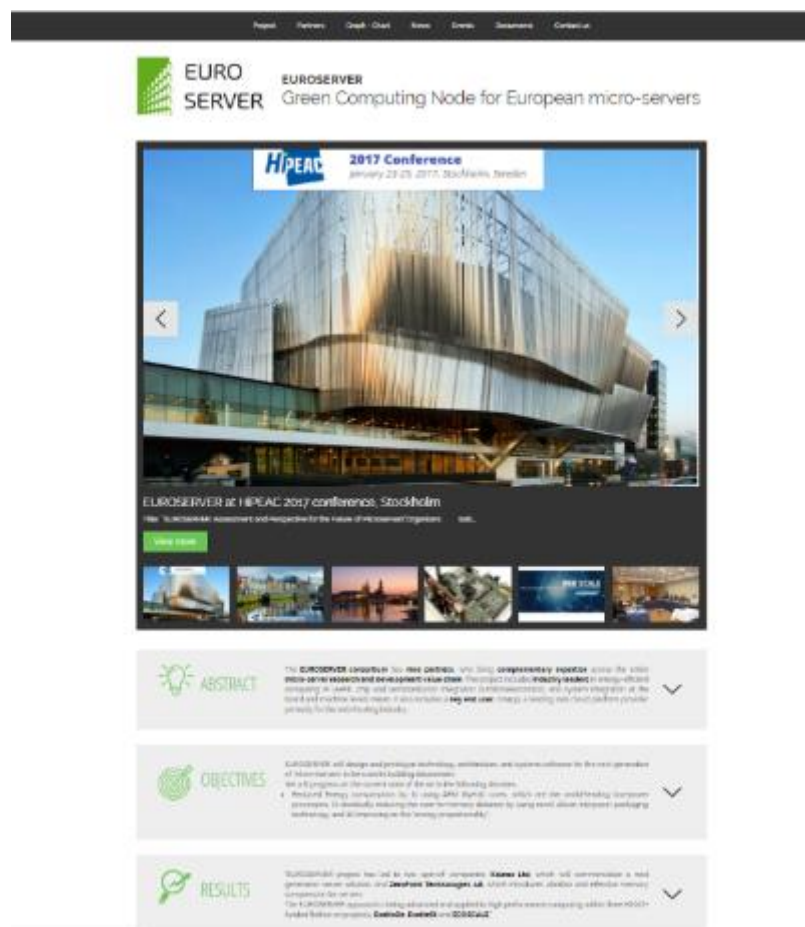


Figure 7 : EUROSERVER website - Front page



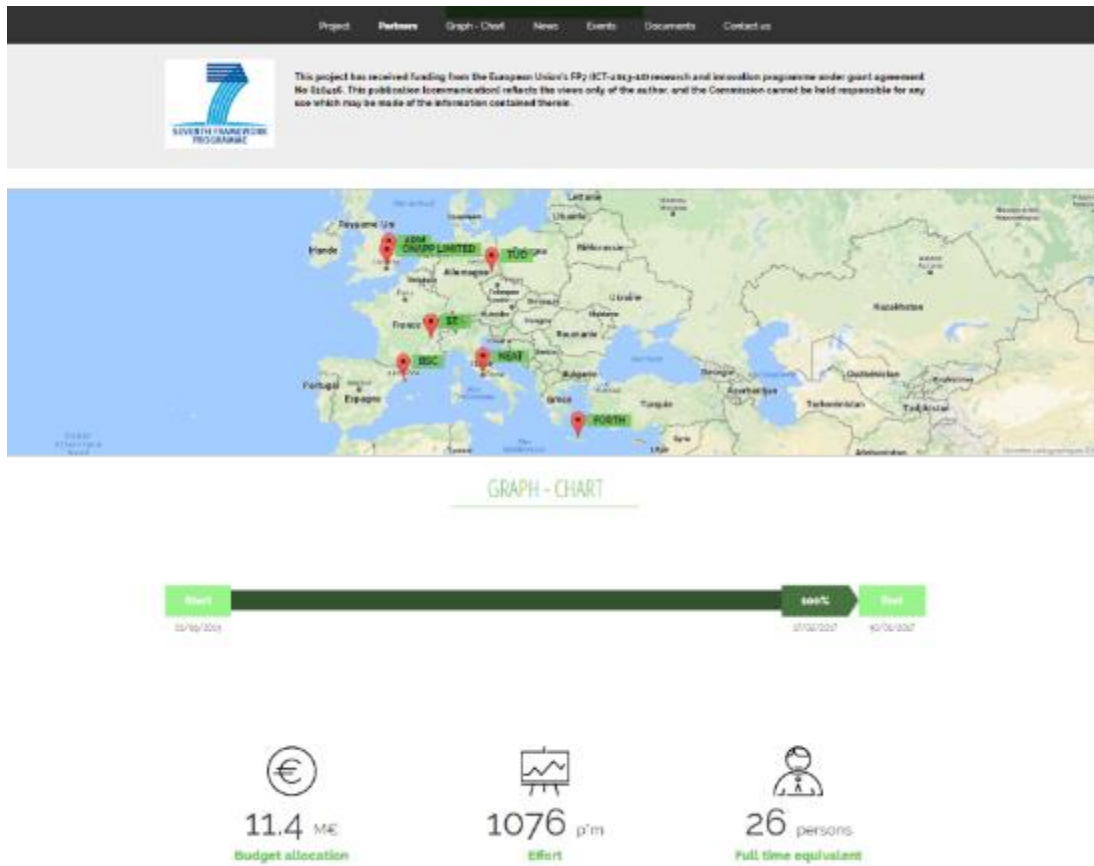


Figure 8 : EUROSERVER website - Consortium and project presentation

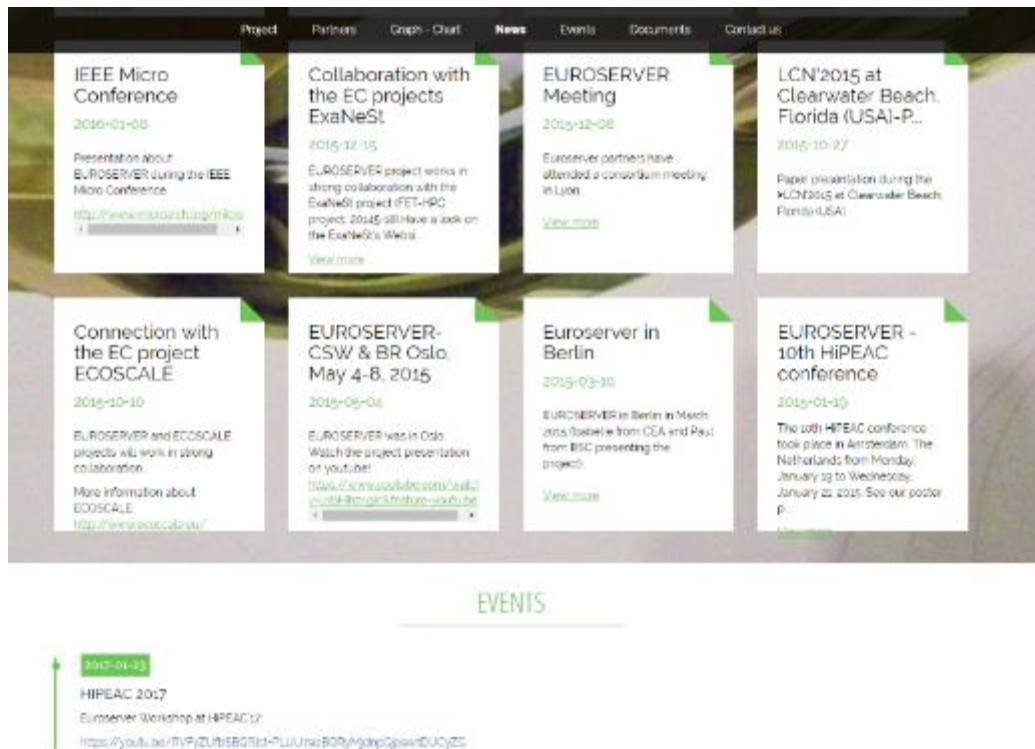


Figure 9: EUROSERVER website - News/events/videos/documents to be uploaded

### *Industrial Advisory Board*

The Industrial Advisory Board (IAB) was formed early 2016 with the two start-up companies Kaleao and ZeroPoint technologies. IAB Invitations letters were signed and announcement was made public on EUROSERVER website. The two start-ups provided keen insight of the market trends, validated EUROSERVER network activities through business collaboration on EUROSERVER technical research outcomes (ZeroPoint Technologies with Chalmers, Kaleao with FORTH and ONAPP through KALEAO-Crete Development Centre, Kaleao with CEA through a signed collaboration contract on advanced 3D packaging design for micro-servers). The two start-ups participated actively to the HiPEAC 2017 workshop focusing on EUROSERVER outcomes.

### *Events and Conferences*

The partners disseminate the findings of EUROSERVER to the scientific and industrial communities through traditional channels including peer-reviewed publications, specialist websites and participating in scientific conferences in the field of computer architecture, information technology, embedded computing, etc. Presenting the latest updates of the project at such events, meetings or workshops will be an effective means of involving industry leaders in standards discussions early on. The list of targeted academic/industrial events includes conference and networks of excellence is listed in Table 4 above.

The list of events and conferences actively attended by EUROSEVER partners is summarised in Table 4 for the period M1-M19 and in Table 6 and Table 7 for M23-M41. The conference/event/workshop distribution is illustrated for the second period and the overall project, with activity focusing on conference and workshop participation.

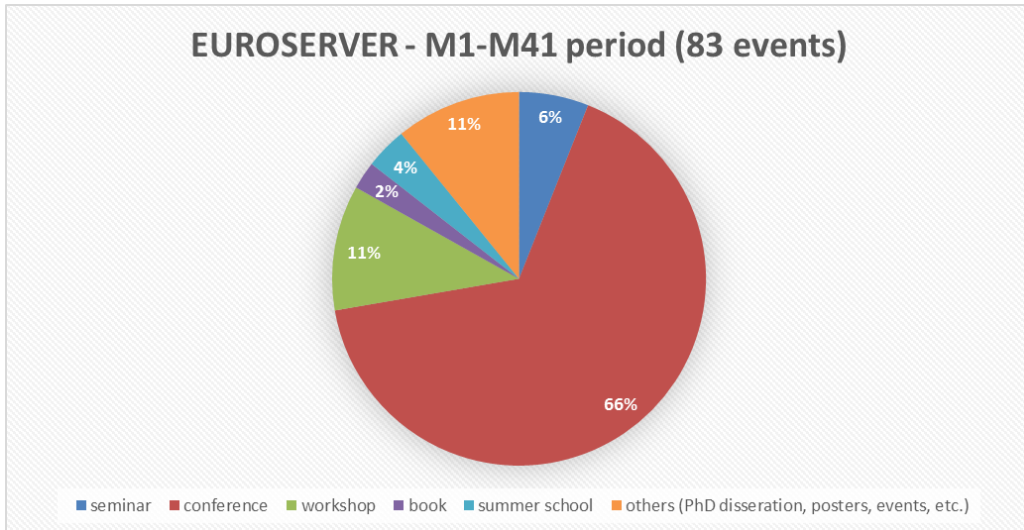


Figure 10: EUROSERVER – Conference/event distribution over the 2<sup>nd</sup> period (M19-M41)

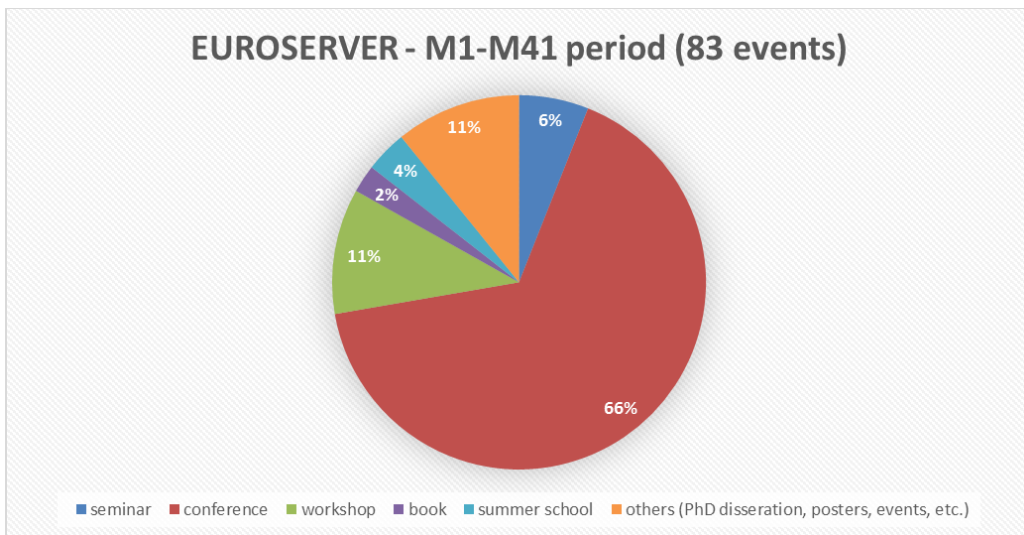


Figure 11: EUROSERVER – Conference/event distribution over the whole project duration (M1-M41)

IN 2016, during Date 2016, a project presentation booth was shared with ExANODE, ExANEST, Eurolab-4-HPC and Ecoscale. The consortium took also the opportunity of the European Project session to present a EUROSERVER paper “EUROSERVER: Share-Anything Scale-Out Micro-server Design”, presentation made by Manolis Marazakis from FORTH. The paper can be found in Annex 5.



Figure 12: Date 2016 – shared project booth

Table 5: EUROSERVER - Attended events/conferences for the period M1-M19 (1st period)

dissemination : past events						
date	event	where	type	partner	who	what
Nov 22, 2013	10th workshop on virtualization in high performance cloud computing (VHPC SC13)	Denver (USA)	workshop	ARM	JG	Invited talk
Dec 10, 2013	Next Generation Computing Systems: components and architectures for a scalable market	Brussels (BE)	workshop	CEA, ST	DD	Project overview+ 3D technology
Jan 20, 2014	HiPEAC 2014	Vienna (AT)	conference	EuTECH, CHA, CEA, FORTH, BSC	6+	Project presentation poster
Jan 28, 2014	Final workshop of the Next Generation Computing Roadmap Study	Brussels (BE)	workshop	CEA	YD	Technology overview
Feb 9-13, 2014	ISSCC	San Francisco (USA)	conference	ARM	JG	Invited talk
Apr 14, 2014	Semba	Pont-en-Royans (FR)	workshop	CEA	YD	Invited pres. Technology overview
May 15, 2014	HiPEAC Computer system week	Barcelona (ES)	thematic session	FORTH	IM	Organization of "Microserver and Virtualization" thematic session
May 19, 2014	Xen project Hackathon	London (UK)	conference	OnApp	JT	Promoted EuroSERVER, Microserver concepts
May 31 - June 8, 2014	MSST 14	Santa Clara (USA)	conference	FORTH	MM	Paper presentation "Jericho Achieving Scalability Through Optimal Data Placement on Multicore System"
Jun 14-18, 2014	ACM/IEEE ISCA'14	Minneapolis (USA)	conference	CHALMER S	AA & PS	Paper presentation "SC2: a statistical compression cache scheme"
Jun 18-21, 2014	Workshop on Parallel I/O Optimization	Hamburg (DE)	workshop	FORTH	MM	Invited talk "Jericho Achieving Scalability Through Optimal Data Placement on Multicore System"
Jul 7-11, 2014	MPSoc 14	Margaux (FR)	conference	TUD	E. Matus	Invited talk "Dataflow models and runtime environment for CRAN applications"
Jul 7-11, 2014	MPSoc 14	Margaux FR)	conference	FORTH	IM	Invited talk "NUMA-like Architecture for Microservers"
Jul 7-11, 2014	MPSoc 14	Margaux FR)	conference	ARM	JG	Invited keynote
July 13-19, 2014	ACACES 2014	Fiuggy (IT)	Summer School	FORTH	KH & JB	Poster presentation "Towards Operating System Support for Remote Memory Usage on ARM Microprocessors"
Aug 17, 2014	DSD 2014 : Special Session on European Projects (EPDSD)	Verona IT)	conference	BSC/CEA/ ...	YD	Project technical presentation
Oct 1, 2014	CFAED Research festival	Dresden (DE)	event	TUD	E. Matus	Demonstration of TUD's "Dataflow multi-core platform for telecom"
Oct 9, 2014	HiPEAC computer system week	Athens (GR)	conference	ARM	JG	Talk
Oct 9, 2014	HiPEAC computer system week	Athens (GR)	conference	FORTH	IM	Presentation "Euroserver: Fast, Energy-efficient Microserver communication in the EuroSERVER project"
Oct 9-10, 2014	Vodafone Innovation Days	Dusseldorf (DE)	event	TUD	E. Matus	Demonstration of TUD's "Dataflow multi-core platform for telecom"
Oct 22, 2014	26th International symposium on computer architecture and high performance computing (SBAD-PAD)	Paris (FR)	symposium	ARM	JG	Invited talk
Oct 27-29, 2014	SOC'14	Tampere (FI)	conference	TUD	O. Arnold, G. Fettweis	Presentation "Adaptative Runtime Management of heterogeneous MPSoC: Analysis, acceleration and silicon prototype"
Nov 3-5, 2014	ACM SoCC'14	Seattle (USA)	conference	FORTH	MM	Poster + paper presentation "Vanguard Increasing Server efficiency via Workload isolation in the storage IO Path"
Dec 2014	Electronic Times interview	international	interview	ARM	JG	interview
Dec 2, 2014	IEEE 3DIC Conference	Dublin (IR)	conference	ARM	JG	Keynote
Jan 20, 2015	HiPEAC 2015	Amsterdam (NL)	conference	all	BSC, FORTH, Chalmers, OnAPP + 2 invited speakers (B. Grot, A. Motakis)	Workshop organization "Greencomputing Node for European Micro-Servers"
Jan 20, 2015	HiPEAC / EuroSERVER workshop	Amsterdam (NL)	conference	FORTH	DP	Paper presentation "Software mechanisms for ARM microserver internal/external communication using memory and RDMA"
Jan 20, 2015	HiPEAC / EuroSERVER workshop	Amsterdam (NL)	conference	OnApp	JC	Paper presentation "A Hypervisor architecture for microservers"
Jan 21, 2015	HiPEAC 2015	Amsterdam NL)	conference	all		Poster presentation
Feb 13, 2014	UC Berkeley award ceremony 'IEEE' milestone for the RISC project	Berkeley USA)	Invited Seminar	FORTH	Manolis Katevenis	Invited talk "Interprocessor communication and its interface to the memory hierarchy"
Mar 9-11, 2015	ARTEMIS/ITEAC co-summit 2015	Berlin (DE)	conference	BSC/CEA/ FORTH	YD, ID, PC	Project presentation poster
Mar 19, 2015	UKDF	Manchester (UK)	conference	ARM	JG	Invited talk
Mar 23, 2015	ARM Internal strategy workshop	Cambridge (UK)	workshop	ARM	JG	Workshop participation
Mar 25-25, 2015	NGMN Industry Conference & Exhibition 2015	Frankfurt (DE)	conference	TUD	E. Matus	Paper presentation "Dataflow for CRAN applications"
Apr 10, 2015	Innovate UK EEC SIG AGM	Manchester UK)	conference	ARM	JG	Invited talk
Apr 15, 2015	Coolchips	Yokohama (JP)	conference	ARM	JG	Keynotes
May 7-8, 2015	IEEE/ACM ANCS'15	Oakland, CA (USA)	conference	FORTH	A. Psathakis, V. Papaefstathiou, N. Chrysos, F. Chaix, E. Vasilakis, D. N. Pnevmatikatos, M. Katevenis	Paper Presentation "A Systematic Evaluation of Emerging Mesh-like (CMP) NoCs"

Table 6: EUROSERVER - Attended events/conferences since M20 up to M35

date	event	where	type	partner	who	what
July 5 – 10, 2015,	Dagstuhl Seminar 15281 – Algorithms and Scheduling Techniques to Manage Resilience and Power Consumption in Distributed Systems	Schloss Dagstuhl – Leibniz Center for Informatics, Germany.	Seminar	BSC	Fredy Juarez, Jorge Ejarque, Rosa M. Badia	Energy-aware Scheduling for Task-based Applications
July, 13-17, 2015	MPSoc'15	Ventura (USA)	conference	ARM	J. Goodacre	Keynote presentation "Starting a push towards European Exascale: exaNODE/exaNEST/ecoSCALE and mores"
July 16, 2015	MPSoc Forum 2015	Ventura (USA)	conference	TUD	E.Matus	Presentation: Data Plane Framework for Software Defined Radio Access Networks ( <a href="https://www.mpsoc-forum.org/previous/2015/program.html">https://www.mpsoc-forum.org/previous/2015/program.html</a> )
Sept 3-4, 2015	UK eFutures workshop	Leeds (UK)	workshop	ARM	J. Goodacre	Presentation about shared and positioned EUROSERVER activities and applicability in a workshop ( <a href="http://efutures.ac.uk/sensors-systems-event-34th-september-2015">http://efutures.ac.uk/sensors-systems-event-34th-september-2015</a> )
Sept 15, 2015	ICTenergy, Workshop on the Future Energy in ICT Research Agenda	Bristols (UK)	workshop	ARM	J. Goodacre	Presentation about position of EUROSERVER for energy usage in ICT ( <a href="https://www.eventbrite.co.uk/e/workshop-on-the-future-energy-in-ict-research-agenda-tickets-16972659682">https://www.eventbrite.co.uk/e/workshop-on-the-future-energy-in-ict-research-agenda-tickets-16972659682</a> )
Sept 21, 2015	HiPEAC Systems Computing Week	Milano(IT)	thematic session	FORTH	N. Chrysos, F. Chaix	organization of a thematic session on "System-level interconnects for exascale-class Datacenters and HPC"
Oct 21, 2015	PhD Dissertation	Chalmers, Goteborg, Sweden	PhD	Chalmers	Angelos Arelakis and Per Stenstrom	PhD dissertation of Angelos Arelakis: Statistical Compression Cache Design
Oct 26-29, 2015	LCN'2015	Clearwater Beach, Florida (USA)	IEEE conference	BSC	Renan Fischer e Silva, Paul Carpenter	Exploring Interconnect Energy Savings Under East-West Traffic Pattern of MapReduce Clusters
Oct, 2015	PhD Dissertation	Dresden (DE)	PhD	TUD	B.Noethen	Investigation of communications mechanisms in heterogenous multi-processor systems
Nov 24, 2015	BigStorage ETN Project meeting		technical session	FORTH	Maniolis Marezakis	technical presentation about 'Storage Solutions' (the EuroServer features shared I/O devices); <a href="http://bigstorage-project.eu/">http://bigstorage-project.eu/</a>
Dec 8, 2015	IEEE Micro Conference	Honolulu, Hawaii	conference	Chalmers	Angelos Arelakis and Per Stenstrom	Paper presentation "a hybrid Cache compression Method for Selection of Data-Type-specific compression methods"
Dec, 2015	Morgan Claypool Synthesis Lectures	N/A	Book	Chalmers	A. Arelakis and P. Stenström w/ S. Sardashti and D. Wood (Univ of Wisconsin, USA)	Tutorial textbook on compression in the memory hierarchy "A primer on Compression in the Mmemory Hierarchy", Morgan-Claypool, 2015
Dec, 2015	Morgan Claypool Synthesis Lectures	N/A	Book	Chalmers	A. Arelakis and P. Stenström w/ S. Sardashti and D. Wood (Univ of Wisconsin, USA)	Tutorial textbook on compression in the memory hierarchy
Dec 5-9, 2015	IEEE Micro Conference	Honolulu, Hawaii	conference	Chalmers	Angelos Arelakis and Per Stenstrom	Two Papers - "HyCOMP: A Hybrid Cache Compression Method for Selection of Data-Type-Specific Compression Methods" - "A scalable Address Extension of DDR4 for Large Capacity Memories"

date	event	where	type	partner	who	what
Jan 18-20, 2016	HiPEAC 2016	Praga (CZ republic)	conference	All partners		Project Poster presentation+ Invited talk "Survey about power management in the microserver context" in the workshop "Microserver: energy efficient servers"
17-19 Feb. 2016	24th Euromicro International Conference on Parallel, Distributed, and Network-Based Processing (PDP 2016)	Heraklion, Crete	Conference	FORTH	Fabien Chaix	"Suitability of the Random Topology for HPC Applications" - DOI: 10.1109/PDP.2016.10
Mar-2016	DATE	Dresden	Conference	TUD	M.Hassler et al.	Demo: Dataflow framework for wireless communications
Mar 14-18, 2016	Date 2016	Dresden (DE)	conference	All partners		Paper "Euroserver: Share-Anything Scale-Out Micro-Server Design" submitted + Project presentation booth shared with ExANODE, ExANEST, Eurolab-4-HPC and Ecoscale
May 2016	IEEE CCECE	Vancouver	Conference	TUD	Y. Chen at al.	Paper: Centralized parallel multi-path multi-slot allocation approach for TDM NoCs
May 2016	IEEE GLSVLSI	Boston	Conference	TUD	Y. Chen at al.	Paper: Trellis-search based dynamic multi-path connection allocation for TDM-NoCs
May 15-18, 2016	The 29th annual IEEE Canadian conference on electrical and computer engineering (CCECE'16)	Vancouver (CA)	IEEE conference	TUD	Yong Chen, Emil Matus, Gerhard Fettweis	Paper "Centralized parallel multi-path multi-slot allocation approach for TDM NoCs"
May 18-20, 2015	IEEE/ACM Great Lakes Symposium on VLSI (GLSVLSI'16)	Boston, Massachusetts, USA	IEEE conference	TUD	Yong Chen, Emil Matus, Gerhard Fettweis	Paper "Trellis-search based Dynamic multi-path connection allocation or TDM-NoCs"
Jun 2016	ACM/EDAC/IEEE DAC	Austin	Conference	TUD	S.Haas, E.Matus et al.	Paper: An MPSoC for Energy-Efficient Database Query Processing
Jun 18-22, 2016	ISCA 2016, Internatinal Symposium on Computer Architecture		conference	Chalmers	D. Knyagin and al.	paper "A probabilistic Hybrid Main Memory Management Framework for High performance and Fairness"
Jun 28 - Jul 1, 2016	IEEE conference on dependable systems and networks (DSN 2016)	Toulouse (FR)	conference	TUD	Sadia Moriam, Gerhad Fettweis	Paper "Fault Tolerant Routing Algorithms for the Hexagonal Network-on-Chip based on the Turn Model"
Jul 2016	IEEE ASAP	London	Conference	TUD	S.Haas, G.Fettweis et al.	Paper: HW/SW-Database-CoDesign for Compressed Bitmap Index Processing
Jul 2016	ACACES 2016	Fiuggy (IT)	Summer School	FORTH	Dimitrios Poullos, Manolis Marazakis, Manolis Katevevis	Poster presentation: "Accelerating TCP Sockets using RDMA in a Microserver Environment"
Jul 2016	ACACES 2016	Fiuggy (IT)	Summer School	FORTH	Dimitris Giannopoulos, Nikolaos Chrysos, Manolis Katevenis	Poster presentation: "Max-Min Fair Rate Allocation Congestion Control for Network QoS"

Table 7: EUROSERVER – Attended events/conferences since M36 up to M41

date	event	where	type	partner	who	what
29 Aug - 2 Sep 2016	Proceedings of the 13th International Conference on Principles and Practices of Programming on the Java Platform: Virtual Machines, Languages, and Tools (PPPJ '16)	Lugano, Switzerland	Conference	FORTH	Foivos S. Zakkak and Polyvios Pratikakis	"DisQuawk: 512 cores, 512 memories, 1 JVM" - DOI: <a href="http://dx.doi.org/10.1145/2972206.2972212">http://dx.doi.org/10.1145/2972206.2972212</a>
Sep 29 2016	IEEE 5G Summit	Dresden (DE)	conference	TUD	Emil Matus	Flexible Signal and Data Processing Platforms for Wireless Communications
Sep 29 2016	IEEE 5G Summit	Dresden (DE)	conference	TUD	Sadia Moriam	Resilient Network-on-Chip for MPSoC
Sep 29 2016	IEEE 5G Summit	Dresden (DE)	conference	TUD	Yong Chen	Guaranteed Service in Network-on-Chip
Oct 01 2016	IEEE Conference on Local Computer Networks (LCN)	Dubai	conference	BSC	Renan Fischer e Silva, Paul Carpenter	Controlling Network Latency in Mixed Hadoop Clusters: Do We Need Active Queue Management?
Oct 3-6, 2016	MEMSYS 2016, 2016 International Symposium on Memory Systems		conference	Chalmers	S. Sardahti and al.	paper "Adaptative Row Addressing for cost-efficient parallel memory protocols in large-capacity memories"
Nov 2016	IEEE NorCAS	Copenhagen	Conference	TUD	S.Haas at al.	Paper: A Database Accelerator for Energy-Efficient Query Processing and Optimization. Best paper award
Nov 7--10, 2016	LCN'2016	Dubai	IEEE conference	BSC	Renan Fischer e Silva, Paul Carpenter	Controlling Network Latency in Mixed Hadoop Clusters: Do We Need Active Queue Management?
Dec 6-9, 2016	9th IEEE/ACM International Conference on Utility and Cloud Computing (UCC 2016)	Shanghai, China	IEEE/ACM conference	BSC	Mauro Canuto, Raimon Bosch, Mario Macias, and Jordi Guitart	Paper "A Methodology for Full-System Power Modeling in Heterogeneous Data Centers"
11-18 Dec 2016	Proceedings of the 22nd IEEE International Conference on Parallel and Distributed Systems (ICPADS'16)	Wuhan, China	Conference	FORTH	Panagiota Fatourou, Nikolaos D. Kallimanis, Eleni Kanellou, Odysseas Makridakis, and Christi Symeonidou	"Towards Implementing Efficient Distributed Data Structures for Future Many-core Architectures"
14-17 December 2015	Proceedings of the 19th International Conference on Principles of Distributed Systems (OPDIS '15)	Rennes, France	Conference	FORTH	Nikolaos D. Kallimanis and Eleni Kanellou	"Wait-free Concurrent Graph Objects with Dynamic Traversals"
Jan 2017	HiPEAC Conference 2017	Sweden (SE)	conference	all		Organized EUROSERVER Workshop
Jan 23-25, 2017	HiPEAC 2017	Stockholm (SE)	workshop	CEA, Chalmers, FORTH, TUD, BSC, ONAPP + invited speakers (Kaleao, ZeroPoint)		<i>EUROSERVER: Assessment and Perspective for the Future of Energy-Efficient Servers</i>
Feb 01 2017	8th International Supercomputing Conference in Mexico	Guadalajara, Mexico	conference	BSC	Fredy Juárez, Jorge Ejarque, Rosa M. Badia, Sergio Natan and Luis A. Rivas	Energy-Aware Scheduler for HPC Parallel Task Base Applications in Cloud Computing
Mar 2017	Euromicro PDP	St.Petersburg	Conference	TUD	Y. Chen at al.	<i>Paper: Register-Exchange based Connection Allocator for Circuit Switching NoCs</i>
Mar 2017	DATE	Lausane	Conference	TUD	M.Hassler et al.	Demo: Dataflow runtime system for wireless signal processing



## *Education and Training*

Participation or organisation of activities specifically connected to education and training such as research exchanges, seminars or training courses are planned within the project duration.

As reported in D1.2, a first EUROSERVER Workshop was organised during HiPEAC 2015 (Amsterdam, 22/01/2015) entitled “EUROSERVER : Green Computing Node for European Micro-Servers”. Two speakers were invited: Boris Grot (University of Edinburgh / School of Informatics) and Antonios Motakis (Virtual Open Systems) and four papers were presented by EUROSERVER partners. The complete agenda of the workshop is detailed in annex 6.

A second workshop was organised during HiPEAC 2017 (Stockholm, 25/01/2017), entitled “EUROSERVER: Assessment and Perspective for the Future of Energy-Efficient Servers”. This workshop, through invited talks and discussion, aimed at highlighting the project’s technical results and impact. Representatives of Kaleao and ZeroPoint were invited to participate, in order to offer their practical perspective on the commercialisation of project results. The complete agenda of the workshop is detailed in Annex 7. Around forty researchers and industry experts were in attendance at the meeting.



**Figure 13: HiPEAC 2017 – EUROSERVER workshop**

Theses or masters are conducted among the partners with topics directed connected to EUROSERVER project. The list below, see Table 8, displays details of them.

Table 8: EUROSERVER - List of theses

dissemination : thesis					
date1	date	Partner	Phd/Master	student	topic
J-14	End 2017 (expected)	BSC	PhD	Renan Fischer e Silva	Heterogeneous architecture Interconnect Energy Saving on Microserver workloads
F-14	Feb 2014	CHALMERS	MSc	Li Kang	Memory compression
M-14	Mar 2014	TUD	PhD	Yue Zhen Wen	MPSoC runtime system
J-14	End 2018 (expected)	BSC	PhD	Luis Garrido	Heterogeneous architecture Virtualization techniques for the exploitation of resources across coherence islands
J-14	Jun 2014	CHALMERS	Lic Eng	Dmitry Knyagin	Hybrid (DRAM/NVM) memory systems
J-15	Jan 2015	TUD	PhD	Friedrich Paulus	Data management, optimization for telecom MPSoC
J-15	Jan 2015	TUD	PhD	Sebastian Haas	Multiprocessor, achitecture for data intensive applications
A-15	Apr 2015	FORTH	MSc	Yannis Velegrakis	OS support for using remote memory and network interface on a system with an RDMA-capable interconnect
A-15	Apr 2015	FORTH	MSc	Dimitris Poullos	Sockets-based communication over an RDMA-capable interconnect
M-15	May 2015 (expected)	CHALMERS	MSc	Jonas Andersson	Memory compression
M-15	May 2015 (expected)	CHALMERS	MSc	Niklas Doverbo	Memory compression
S-15	Sept 2015 (expected)	CHALMERS	PhD Eng	Angelos Arelakis	Memory compression
S-15	Sep 2015	TUD	PhD	Nairuhi Grigorian	Software Defined RAN Architecture
S-15	Sep 2015	FORTH	BSc	Charalampos Aronis	Mechanisms to use remote memory on an ARM-based microserver
N-15	Nov 2015	FORTH	BSc	Georgios Constantinidis	DMA controller design factors and system architecture ramifications
F-16	Feb 2016	FORTH	BSc	Ioannis Vardas	Memory testing through an FPGA with an embedded processor
O-16	Oct 2016	FORTH	PhD	Foivos Zakkak	Java™ on Scalable Memory Architectures
N-16	Nov 2016	FORTH	BSc	Konstantinos Chalas	Introducing NUMA support for ARM64 based platforms
F-17	Feb 2017	FORTH	BSc	Michail Gianioudis	AXI Virtualized UART (Universal Asynchronous Receiver Transmitter)

## Journals

Partners have been very active in publishing, more than 20 papers in since May 2015, including at IEEE LCN 2015 (BSC), MICRO 2016 (Chalmers), DATE 2016 (all), IEEE LCN 2016 (BSC), IEEE/ACM ANCS 2015 (FORTH), MPSoC Forum 2015 (TUD), NGMN Industry Conference 2015 (TUD), and ISCA 2016 (Chalmers), etc.

The DATE 2016 publication, titled “EUROSERVER: Share-Anything Scale-Out Micro-Server Design”, to which all partners contributed, was a summary of the differentiation and uniqueness of the approach being adopted by the EUROSERVER project, more details in annex 5.

Additional publications submitted to journals, still under review, include IEEE Top Picks in Computer Architecture (Chalmers) and IEEE/ACM Transactions on Networking (BSC). The list below displays some of them (see Table 9).

## Press releases

Press releases (Table 9) are one of the most effective ways of communicating the existence of the project to a specific target audience (general public and related institutions) by attracting attention to the project's progress and its achievements. The initial press release is the most important one, because it defines the EUROSERVER project objectives as well as its working plan. There may be further press releases during the project. In the middle of the project there could be a press release to explain the project's progress, and at the end of the project, a press release for the scientific results. All press releases and press impacts will be uploaded on the project website. For more details, please read D 7.2 where the complete press strategy has been defined.

The first press release was released on March 27<sup>th</sup> 2014 with the content given in Annex 1: Text of press release, at the end of this document. It was sent to HPC Wire, Scientific Computing World, Technology Review, Wired, ComputerWorld, eWeek, The Register, GreenComputing Report, ISGTW.

Further details are given in D7.2 (Press Release Along with Project Web Site Address).

A second press release was released on November 3, 2017 through every partner communication department and through HiPEAC communication office. The press release text can be found in Annex 2. It can be mentioned that the press release was been picked up by the media and websites, listing for instance the following websites:

<http://irishtechnews.net/ITN3/more-computations-for-less-energy-new-approach-to-halve-the-cost-of-powering-data-centers/>

<http://www.electronicsspecifier.com/around-the-industry/more-computations-for-less-energy>

<http://www.sensorsmag.com/news/tech-product/news/more-computations-less-energy-european-way-23900>

<https://alltheinternetofthings.com/entries/82440>

<http://irishhub.biz/more-computations-for-less-energy-new-approach-to-halve-the-cost-of-powering-data-centers/>

EUROSERVER was also closely associated to the inauguration event of the Kaleao-Crete development center and many members took actively part as it can be seen in the agenda of the inauguration in Annex 3, the associated press release written by FORTH and Kaleao is available at <https://www.hipeac.net/press/6786/crete-becomes-the-silicon-island-of-high-technology-research-and-development/>.

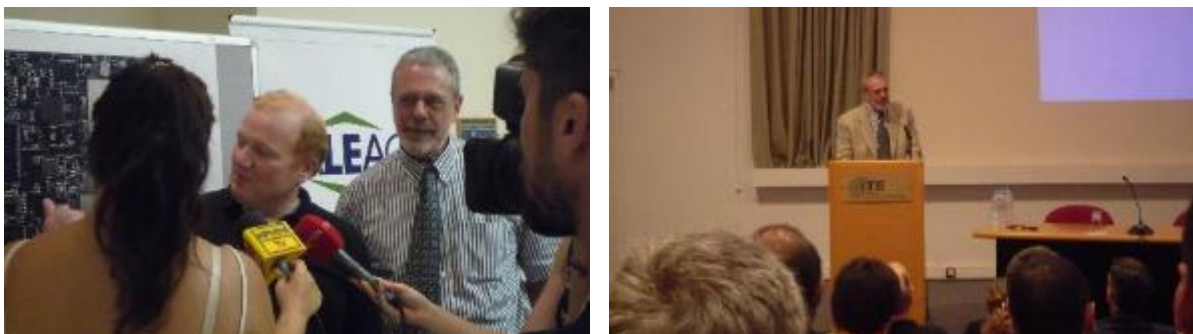


Figure 14: Kaleao-Crete development center, Inauguration

EUROSERVER outcomes are shortly discussed in HiPEAC newsletter January issue under the Tech Transfer section (p35 – HipeacInfo49.pdf, <https://www.hipeac.net/publications/newsletter/>). HiPEAC newsletter article is available in Annex 4. It is planned to contribute to HiPEAC magazine spring release with an extended article discussing EUROSERVER latest outcomes.

EUROSERVER is also mentioned in some technical articles, like the article “UK-based hyper-convergence startup bets on ARM processors » which was posted on SiliconAngle website at the following link <http://siliconangle.com/blog/2016/10/03/u-k-based-hyper-convergence-startup-bets-on-arm-processors/>.

**Table 9: EUROSERVER – List of publications and press releases**

date	Publication	content	reference
March 2014	PanEuropean Networks "Science and technology" issue 10	paragraph "green computing node" about EUROSERVER	<a href="http://www.paneuropeannetworks.com/ST10/">http://www.paneuropeannetworks.com/ST10/</a>
28 March 2014	Press release	Europe invests realising next-generation green computing for micro-servers and scalable compute	<a href="https://www.bsc.es/news/bsc-news/europe-invests-realising-next-generation-green-computing-micro-servers-and-scalable-compute">https://www.bsc.es/news/bsc-news/europe-invests-realising-next-generation-green-computing-micro-servers-and-scalable-compute</a>
3rd Jun 2014	BSC press release	<b>COMPSs enabling main programming languages: Java, C/C++ and Python</b>	<a href="https://www.bsc.es/news/bsc-in-the-media/comps-s-enabling-main-programming-languages-java-cc-and-python">https://www.bsc.es/news/bsc-in-the-media/comps-s-enabling-main-programming-languages-java-cc-and-python</a>
October 2014	EETimes	article on the HiPEAC microservers session and thus EuroSERVER project	<a href="http://www.eetimes.com/author.asp?section_id=36&amp;doc_id=1324294">http://www.eetimes.com/author.asp?section_id=36&amp;doc_id=1324294</a>
17th Oct 2014	BSC press release	<b>Microservers Brew in Europe's Labs</b>	<a href="https://www.bsc.es/news/bsc-in-the-media/microservers-brew-europes-labs">https://www.bsc.es/news/bsc-in-the-media/microservers-brew-europes-labs</a>
19th Nov 2014	BSC press release	<b>BSC releases COMPSs version 1.2 at SC14</b>	<a href="https://www.bsc.es/news/bsc-news/bsc-releases-compss-version-12-sc14">https://www.bsc.es/news/bsc-news/bsc-releases-compss-version-12-sc14</a>
December 2014	Elsevier-Microprocessing&Microsystems-Special Issues	EuroSERVER: Energy Efficient Node for European Micro-Servers	submitted - Dec 15, 2014 / Refused (March 2015) - <b>Refused</b>
January 2015	EETimes	European server project promotes ARM on FDSOI	<a href="http://www.electronics-eetimes.com/en/european-server-project-promotes-arm-on-fdsoi.html?cmp_id=7&amp;news_id=222923411&amp;page=0">http://www.electronics-eetimes.com/en/european-server-project-promotes-arm-on-fdsoi.html?cmp_id=7&amp;news_id=222923411&amp;page=0</a>
summer 2015	HiPEAC newsletter	Socket over RDMA and shared peripherals for ARM microservers	<a href="http://www.hipeac.net/assets/public/publications/newsletter/hipeacinfo43.pdf">http://www.hipeac.net/assets/public/publications/newsletter/hipeacinfo43.pdf</a>
11th Nov 2015	BSC press release	<b>BSC releases COMPSs version 1.3 at SC15</b>	<a href="https://www.bsc.es/news/bsc-news/bsc-releases-compss-version-13-sc15">https://www.bsc.es/news/bsc-news/bsc-releases-compss-version-13-sc15</a>
15th Mar 2016	BSC press release	<b>BSC at DATE 2016</b>	<a href="https://www.bsc.es/news/bsc-news/bsc-date-2016">https://www.bsc.es/news/bsc-news/bsc-date-2016</a>
2nd May 2016	BSC press release	<b>BSC releases COMPSs version 1.4</b>	<a href="https://www.bsc.es/news/bsc-news/bsc-releases-compss-version-14">https://www.bsc.es/news/bsc-news/bsc-releases-compss-version-14</a>

date	Publication	content	reference
14th Jun 2016	BSC press release	BSC at the collaboration workshop Advanced Computing and Cyber-Physical Systems 2016	<a href="https://www.bsc.es/news/bsc-news/bsc-the-collaboration-workshop-advanced-computing-and-cyber-physical-systems-2016">https://www.bsc.es/news/bsc-news/bsc-the-collaboration-workshop-advanced-computing-and-cyber-physical-systems-2016</a>
November 2016	Press release	MORE COMPUTATIONS FOR LESS ENERGY. NEW APPROACH TO HALVE THE COST OF POWERING DATA CENTERS	<a href="http://irishtechnews.net/ITN3/more-computations-for-less-energy-new-approach-to-halve-the-cost-of-powering-data-centers/">http://irishtechnews.net/ITN3/more-computations-for-less-energy-new-approach-to-halve-the-cost-of-powering-data-centers/</a> <a href="http://www.electronicsspecifier.com/around-the-industry/more-computations-for-less-energy">http://www.electronicsspecifier.com/around-the-industry/more-computations-for-less-energy</a> <a href="http://www.sensorsmag.com/news/tech-product/news/more-computations-less-energy-european-way-23900">http://www.sensorsmag.com/news/tech-product/news/more-computations-less-energy-european-way-23900</a> <a href="https://alltheinternetofthings.com/entries/82440">https://alltheinternetofthings.com/entries/82440</a> <a href="http://irishhub.biz/more-computations-for-less-energy-new-approach-to-halve-the-cost-of-powering-data-centers/">http://irishhub.biz/more-computations-for-less-energy-new-approach-to-halve-the-cost-of-powering-data-centers/</a>
11th Nov 2016	BSC press release	BSC releases COMPSs version 2.0 at SC16	<a href="https://www.bsc.es/news/bsc-news/bsc-releases-compss-version-20-sc16">https://www.bsc.es/news/bsc-news/bsc-releases-compss-version-20-sc16</a>
January 2017	HiPEAC newsletter - n°49		<a href="https://www.hipeac.net/publications/newsletter/">https://www.hipeac.net/publications/newsletter/</a>
18th Jan 2017	BSC press release	BSC in action at HiPEAC17	<a href="https://www.bsc.es/news/bsc-news/bsc-action-hipeac17">https://www.bsc.es/news/bsc-news/bsc-action-hipeac17</a>
20th Jan 2017	BSC press release	BSC releases PyCOMPSS version 2.0 as a PIP installable package	<a href="https://www.bsc.es/news/bsc-news/bsc-releases-pycompss-version-20-pip-installable-package">https://www.bsc.es/news/bsc-news/bsc-releases-pycompss-version-20-pip-installable-package</a>
Feb 2017	LinkedIN – BSC posting	Video link and Euroserver update	<a href="https://www.linkedin.com/company/barcelona-supercomputing-center/comments?topic=6237219113765216256&amp;type=U&amp;scope=226216&amp;stype=C&amp;a=VAoT 1424 impressions 13 clicks 4 likes (22/02/2017)">https://www.linkedin.com/company/barcelona-supercomputing-center/comments?topic=6237219113765216256&amp;type=U&amp;scope=226216&amp;stype=C&amp;a=VAoT 1424 impressions 13 clicks 4 likes (22/02/2017)</a>
Feb 2017	Twitter – BSC tweet	Video link and Euroserver update	<a href="https://twitter.com/BSC_CNS/status/831452201780465664 561 impressions. 3 clicks in details. 1 retweet (22/02/2017)">https://twitter.com/BSC_CNS/status/831452201780465664 561 impressions. 3 clicks in details. 1 retweet (22/02/2017)</a>
Feb 2017	Facebook – BSC posting	Video link and Euroserver update	<a href="https://www.facebook.com/BSCCNS/photos/a.132168396860367.32287.131332720277268/1216319678445228/?type=3&amp;theater 860 people reach. 2likes (22/02/2017)">https://www.facebook.com/BSCCNS/photos/a.132168396860367.32287.131332720277268/1216319678445228/?type=3&amp;theater 860 people reach. 2likes (22/02/2017)</a>
February 2017	BSC – website	The EUROSERVER project presents the video “Scale-out architecture for energy efficient servers & micro-servers”	<a href="https://www.bsc.es/news/bsc-news/the-euroserver-project-presents-the-video-%E2%80%9Cscale-out-architecture-energy-efficient-servers-micro">https://www.bsc.es/news/bsc-news/the-euroserver-project-presents-the-video-%E2%80%9Cscale-out-architecture-energy-efficient-servers-micro</a>

### ***Contributions to standards and policy developments***

The EUROSERVER consortium already has significant expertise in participating and leading standardisation activities at an individual partner level. This knowledge and experience will be harnessed for the benefit of the standardisation activities of the project.

There are many standardisation bodies that are related to energy efficiency of datacenters. In the US the certification standard is LEED from the US Green Building Council. In Europe and in particular the UK, the BREEAM Standard has had the largest following. BREEAM and LEED have been used for datacenters but the standards are not so useful after the initial building design has been completed. Ongoing energy use and the real operating costs are large in proportion to the initial costs and as such these standards have limitations that the industry has reacted to by developing other, more targeted standards.

The EC have a code of conduct for datacenters but as it is a self-certification system the British Computer Society created the Certified Energy Efficiency Datacenter Award (CEEDA) that was launched at the end of 2010.

There is also an emerging pan-European standard that is being developed by Building Research Establishment (BRE), Centre Scientifique et Technique du Bâtiment (CSTB) and other leading groups for efficient building design and construction, the Sustainable Building Alliance.

EUROSERVER would look at further investigating the standardisation bodies that are currently used and would look to promote further standards from the perspective of the operating efficiency of hardware. EUROSERVER is well placed to participate in standards bodies and also promote modifications to existing standards. In the course of the project, recommendations are discussed regarding the logical interface, physical interface and requirement of a chiplet for use within other integrated interposed System-in-Package based design with a focus on the memory and the chip-to-chip interfaces.

### ***Dissemination Pack***

The acknowledgement of the EC funding sources will be included in all dissemination materials with the following sentence:

This research project is supported by the European Commission under the 7th Framework programme under the “Information and Communication Technologies” theme, with grant number 610456.

### **General Brochure**

A one-page general presentation is available on the project repository. The general brochure provides information about the project, its objectives and future achievements and its. The format of the brochure is a single-sided A4 sheet, so that interested Project Partners can easily download and print for their own dissemination purposes. It can be distributed in all events or local actions to scientific and industrial contacts defined by each partner.

### Generic poster

A generic poster was initially designed for the HiPEAC 2014 conference. It is represented below in Figure 15:

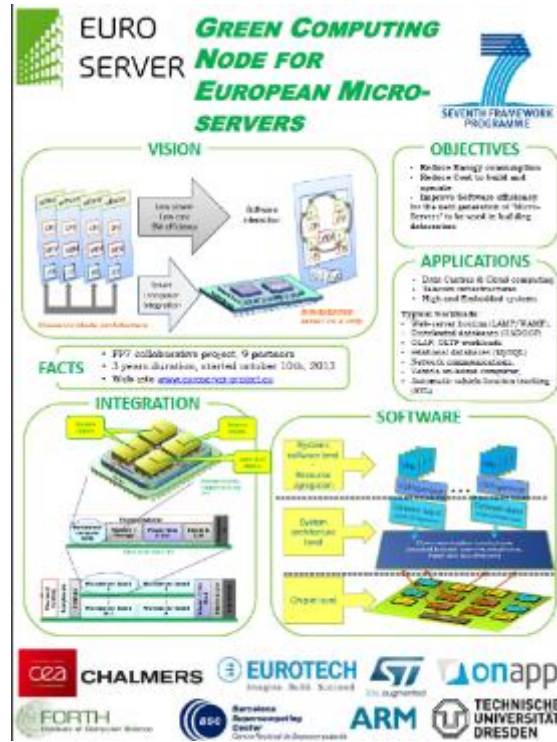


Figure 15: HiPEAC 2014 – EUROSERVER poster

It has been updated for HiPEAC 2015 (Figure 16) and HiPEAC 2016 and Date 2016, (Figure 17: HiPEAC 2016 / Date 2016 – EUROSERVER poster). Altogether a poster was specifically designed for the booth at Date 2016 presenting the 5 associated projects EUROSERVER, ExaNoDe, ExaNeSt, Eurolab-4-HPC and ECOSCALE, see Figure 18. All the posters are available on the project repository.

Figure 16: HiPEAC 2015 – EUROSERVER poster

Figure 17: HiPEAC 2016 / Date 2016 – EUROSERVER poster



**Building a European Ecosystem for Scalable, Low-Power, Low-Cost, High-Performance Computing**

**EURO SERVER** [www.euroserver-project.eu](http://www.euroserver-project.eu)  
 redesigns the enterprise server:  
 Lower cost through system integration  
 Energy efficiency : low-power 64 bit ARM processor and more efficient software  
 Mutualization (sharing) of I/O resources

**ExaNode** [www.exanode.eu](http://www.exanode.eu)  
 ExaNode:  
 highly modular scale-out architecture and building blocks for:  
 • highly efficient,  
 • highly integrated,  
 • high-performance,  
 • heterogeneous  
 compute element aimed towards exascale computing.

**Energy-Efficient Heterogeneous Computing at exaSCALE** - [www.ecoscale.eu](http://www.ecoscale.eu)  
 Many-core PGAS (OpenCL)  
 Reconfigurable Acceleration: Distributed shared reconfigurable logic, Remote coherent accesses, Transparent to user  
 High-Level Synthesis: OpenCL kernels  
 Realtime System: Reconfiguration at runtime, Locality Management, Task Scheduling

**European Exascale System Interconnect and Storage - www.exanest.eu**  
 Storage: fast, distributed in-node non-volatile memory  
 Interconnect: low-latency, unified compute & storage traffic  
 Packaging: advanced, liquid-cooled  
 App's: real, scientific and datacenter  
 Prototype: 1000+ ARM cores from EuroServer ARM nodes with UNIMEM address space & shared I/O from ExaNode, OpenCL, SI Interposer with exaSCALE Heterogeneous ARM + FPGA's  
 Isootope Ltd: Fully immersed Cooling Technology

**EuroLab-4-HPC: Foundation for a Centre of Excellence in HPC Systems** [www.eurolab4hpc.eu](http://www.eurolab4hpc.eu)  
 Objectives  
 • joining HPC system research around a long-term research agenda  
 • defining a curriculum to foster future European HPC technology leaders  
 • accelerating commercial uptake of new HPC technologies  
 • building an HPC ecosystem with researchers and other stakeholders, e.g. HPC system providers and venture capital  
 • forming the foundation and vision for a self-sustainable CoE

Figure 18: Date 2016 – Poster presenting the 5 associated projects

### Dissemination video

A dissemination video was produced to draw attention to the successful use of public money, leading to two start-ups. The video is targeting at a general audience. It is available at <https://youtu.be/2EnEKoZ2Tp0> and on EUROSERVER website.

## Annex 1: Text of press release

### INTRODUCING: THE EUROSERVER PROJECT

#### **Europe invests realising next-generation green computing for micro-servers and scalable compute:**

27 March 2014

The EUROSERVER project brings together under the support of the European FP7 ICT funding program world-class industrial and academic expertise to design and prototype technology, architecture and systems software for the future generations of energy-efficient reduced-cost micro-servers and scalable compute platforms

Data centres, and computing in general, are driving the Information Society worldwide and are one of the key resources for innovation and leadership of European industry. As data centre traffic and workloads continue to grow, data centre scaling is increasingly constrained by existing server technology due to insufficient server density, high power consumption and high total cost of ownership (TCO). This is why EUROSERVER has taken to reconsider the basic components and fundamental system architecture of future technology and the resulting server platforms, by architecting and proving their suitability through delivering into a full prototype system.

There are three key axes to the EUROSERVER approach. Firstly, the project will use the low-power 64-bit ARM Cortex™ processors fabricated using the FDSOI fabrication technology, an ideal silicon platform for data centre workloads. Secondly, the project will advance the state-of-the-art in 3D silicon-on-silicon and multichip module package integration, placing multiple silicon “compute chiplets” on an active silicon interposer, while also integrating multiple gigabytes of memory within package together improving fabrication yields, compute density, reduced energy consumption and significantly reducing the cost of acquisition and ownership. Thirdly, EUROSERVER proposes a new backwards compatible system software architecture that allows resource virtualisation and sharing of global memory and I/O between multiple compute nodes while delivering new memory models that will enable the future generation of more efficient and high-performance software paradigms.

EUROSERVER is a three-year project coordinated by Commissariat à l'énergie atomique et aux énergies alternatives (CEA) with a managed budget of 12.9 million euros, including 8.6 million euros funded by the European Commission's FP7 Programme plus significant indirect support from the industrial partners.

The three main project objectives are:

- To reduce energy consumption by: (a) using low-power 64-bit ARM cores, (b) reducing the core-to-memory distance through silicon interposer and packaging technology, and (c) while improving energy proportionality.
- To reduce the cost to manufacture, build and operate, by: (a) improved manufacturing yield through 3D integration of multiple chiplets on an active silicon interposer, and (b) small size of the packaged interposer module, and (c) and energy-efficient semiconductor process (FDSOI).
- To improve software efficiency through next-generation system software that (a) manages the resources in a server with a common global address space and (b) isolates and protects multiple

workloads from each other when they share resources such as I/O, storage, memory, and interconnects.

“The EUROSERVER prototype will demonstrate how the proposed approach can improve energy efficiency by a factor of ten, by 2020” says Yves Durand, EUROSERVER project coordinator. The prototype will be evaluated using workloads for (a) data centres and cloud computing (LAMP, WAMP, HADOOP, MySQL), (b) telecom infrastructures (network communications), and (c) high-end embedded systems (vehicle onboard computer, automatic vehicle location tracking [AVL], advanced security and surveillance).

EUROSERVER brings together a European consortium, joining industrial technology providers, universities and research centres: Eurotech (Italy) as the system integrator, ARM (UK) as the world leader in embedded high-performance processor IP, and STMicroelectronics (France), Europe’s leading semiconductor company, as well as OnApp (Gibraltar), which provides a complete IaaS platform for hosts, telcos and MSPs. In addition to the technology providers and users, EUROSERVER brings application and computer and memory architecture expertise from Barcelona Supercomputing Center (Spain), TU Dresden (Germany), FORTH (Greece) and Chalmers (Sweden).

EUROSERVER was launched in September 2013. More information is available at the project’s website at [www.EuroSERVER-project.eu](http://www.EuroSERVER-project.eu).

## Annex 2: Text of the 2<sup>nd</sup> press release



### More computations for less energy – the European way

#### *New approach for ARM-based technology to halve the cost of powering data centers*

Grenoble, 3 November 2016 – Press Release

EUROSERVER, a leading EU-funded research project, is paving the way toward lower energy consumption in data centers. Based on the concept of chiplets, where multiple silicon subsystems are mounted in an integrated device, along with an associated new groundbreaking system architecture, the project has enabled more energy-efficient servers and has even inspired startups motivated by the new technology.

Delivering the potential to reduce energy consumption in data centers by at least half, the breakthrough leads to substantial reduction in the total cost of acquisition and operation (total cost of ownership (TCO)).

EUROSERVER created system architecture and runtime software innovations: the sharing of peripheral devices, access to system wide memory, compression of data to better utilise memory and lightweight hypervisor capabilities. These are being demonstrated with applications across the data center and telecommunications domain. All reduce energy consumption and have been developed for systems built around energy-efficient 64-bit ARM<sup>®</sup> v8-based architecture.

Two startups have already been launched, inspired by the technology created during the project:

*Kaleao Ltd.*, with headquarters in the UK and labs in Crete and Italy, has introduced a unique new generation of web-scale, true-converged server appliance that features physicalised resource sharing, OpenStack virtualisation services and extreme core density, leading to low energy consumption and significant computing capabilities.

*ZeroPoint*, in Sweden, commercialises the memory compression innovations.

Data centers account for a huge consumption of power. If all the data centers in the USA alone were a country, their energy consumption would rank 12th in the world. As the capacity and number of data centers increase, so do the financial and environmental impacts of their vast energy use. EUROSERVER's innovation will take efficient and scalable ARM processors and use the flexibility of a System-on-Chip (SoC) design at the system level to create a new type of server.

This evolution is comparable to the transition from mainframe computers to mass-produced personal computers (PCs) in the 1980s, which in turn evolved into modern servers. With smartphones the contemporary equivalent of 1980s PCs, now is the time to take advantage of their architectural flexibility and evolve them to create the energy-efficient servers of the future.

Isabelle Dor, Research Engineer at CEA and EUROSERVER Coordinator, said: “EUROSERVER is delivering vital energy savings for data centers and CEA/LETI is proud to coordinate this important EU-funded project. The SoC architectures and advanced packaging solutions being developed bring us one step closer to scalability and power efficiency in data centers. We are also delighted that two startups have been created to leverage innovations from the project.”

“ARM is committed to enabling energy-efficient computing. Together, the consortium helped define a set of Reliability, Availability and Serviceability (RAS) requirements for enterprise servers,” said John Goodacre, director of technology and systems, ARM. “ARM subsequently enhanced its processor architecture with [the ARMv8.2-A release](#), which included a specific extension in support of RAS.”

“This ambitious European project has benefited from ST’s expertise in complex SoC architectures and ARM-core integration, along with silicon technology and packaging techniques,” said Patrick Blouet, Collaborative R&D programs manager, STMicroelectronics.

Simone Cabasino, President in NEAT, noted: “We are happy to design, develop and bring-up the board and the system for the project, and we are also proud to be a technology partner of the KALEAO startup.”

Julian Chesterfield, Director of the Emerging Technology Group at OnApp Ltd. reports: “The EUROSERVER design highlights the trend for power efficient and high density computing environments entering the data center. As a cloud infrastructure provider, our customers will benefit from the improvements in the virtualisation platform, being able to handle more end-users while at the same time benefiting from lower electricity costs.”

Giampietro Tecchiolli, CEO of KALEAO Ltd., stated: “We started KALEAO with the goal to revolutionise the server market by enabling true convergence at web-scale with our KMAX products. EUROSERVER has been a source of partnerships, inspiration, expertise and technology contributions. In sharing many of the EUROSERVER paradigms, we use ARM cores in order to reduce the costs and energy for a server while achieving unprecedented compute density.”

Per Stenström, Professor at Chalmers University of Technology, Sweden, said: “This project gave us the opportunity to develop novel memory optimisations, including memory compression and hybrid memory management technologies, for servers and high-performance platforms.”

Then, as founder and CTO of ZeroPoint Technologies AB, Per Stenström added: “Our results at Chalmers in EUROSERVER are so promising that we created this spin-off company with the mission to commercialise these memory compression technologies; we are very happy with the interest that we have already seen among several potential customers.”

Manolis Katevenis, Head of the Computer Architecture Lab at FORTH/ICS, said: “The new UNIMEM architecture, to which we made key contributions, allows communicated data to enter directly into receiver memory, thus reducing overhead. We are glad to have built prototypes and systems software for UNIMEM,

and to have supported KALEAO through their Development Center in the Science and Technology Park of Crete.”

Emil Matus, Senior Researcher at *TUD, the Dresden University of Technology*, noted: “TUD aims to advance the software defined mobile network infrastructure by exploiting the EUROSERVER high density computing architecture for 5G radio access dataflow applications. This project allowed us to develop the dataflow framework with dynamic resource management capability, enabling the exploration and efficient deployment of Cloud-RAN wireless algorithms.”

Paul Carpenter, Senior Researcher at *BSC, the Barcelona Supercomputing Center*, added: “BSC is advancing the state of the art in energy-efficient systems and runtime software to support memory capacity sharing, energy-efficient scheduling of tasks and workloads and energy-aware virtual machine placement in cloud infrastructure.”

**About EUROSERVER:** this project is funded by the European Union, under FP7 Grant Agreement 610456. For more information, visit [www.euroserver-project.eu](http://www.euroserver-project.eu) or contact Ms. Isabelle Dor - [isabelle.dor@cea.fr](mailto:isabelle.dor@cea.fr)

**About KALEAO:** visit [www.kaleao.com](http://www.kaleao.com)

**About ZeroPoint:** visit [www.zptcorp.com](http://www.zptcorp.com)

## Annex 3: Inauguration event of the Kaleao-Crete development center - Agenda



### KALEAO-Crete Development Centre

*Science and Technology Park of Crete (STEP-C), Vassilika Vouton, Heraklion*

### INAUGURATION

*Thursday, 30 June 2016*

#### Agenda

FORTH AMPHITHEATRE	
16:00 – 17:00	KEYNOTE SPEECH Prof. Christoforos Kozyrakis, EPFL and Stanford University
17:00 – 17:40	PRESS CONFERENCE
17:40 – 17:45	Prof. Costas Fotakis, Alternate Minister of Research and Innovation
17:45 – 17:50	Mr. Stavros Arnaoutakis, Regional Governor of Crete
17:50 – 17:55	Mr. Vasilis Lambrinos, Mayor of Heraklion
17:55 – 18:00	Prof. Constantine Stephanidis, Director, Institute of Computer Science, FORTH
18:00 – 18:05	Dr. Artemis Saitakis, Director, Science & Technology Park of Crete
18:05 – 18:10	Ms. Isabelle Dor, Coordinator, EuroServer Project
18:10 – 18:20	Dr. Julian Chesterfield, Director of Emerging Technologies, OnApp Ltd.
18:20 – 18:25	Prof. Manolis Katevenis, Head, Computer Architecture & VLSI Systems Lab, FORTH-ICS
18:25 – 18:30	Dr. Iakovos Mavroidis, Head, KALEAO-Crete Development Centre
18:30 – 18:40	Prof. John Goodacre, Co-Founder and Chief Scientific Officer, KALEAO Ltd. (UK)
STEP-C, Building B	
19:00	Inauguration of the KALEAO-Crete Development Centre, Mr. Paul Arts, VP of Engineering, KALEAO Ltd. (Padova, IT)
STEP-C, Patio in front of Building B	
19:20 – 21:00	Cocktail Party, light Live Music

## Annex 4: HiPEAC Newsletter – January 2017



## Technology transfer

# EUROSERVER: transferring and using power efficiency know-how

## MORE COMPUTATIONS FOR LESS ENERGY

The EU-funded project EUROSERVER has developed a new approach for ARM-based technology to halve the cost of powering data centres. Based on the concept of chiplets, where multiple silicon subsystems are mounted in an integrated device, along with an associated new groundbreaking system architecture, the project has enabled more energy-efficient servers and has even inspired startups motivated by the new technology.

Delivering the potential to reduce energy consumption in data centres by at least half, the breakthrough leads to substantial reduction in the total cost of acquisition and operation (total cost of ownership (TCO)).

EUROSERVER created system architecture and runtime software innovations: the sharing of peripheral devices, access to system wide memory, compression of data to better utilize memory and lightweight hypervisor capabilities. These are being demonstrated with applications across the data center and telecommunications domain. All reduce energy consumption and have been developed for systems built around energy-efficient 64-bit ARM@v8-based architecture.

Two startups have already been launched, inspired by the technology created during the project:

**KALEAO Ltd.**, with headquarters in the UK and labs in Crete and Italy, has introduced a unique new generation of web-scale, true-converged server appliance that features physicalized resource sharing, OpenStack virtualization services and extreme core density, leading to low energy consumption and significant computing capabilities.

**ZeroPoint**, in Sweden, commercializes the memory compression innovations.

Data centres account for a huge consumption of power. If all the data centres in the USA alone were a country, their energy consumption would rank 12th in the world. As the capacity and number of data centres increase, so do the financial and environmental impacts of their vast energy use. EUROSERVER's innovation will take efficient and scalable ARM processors and use the flexibility of a System-on-Chip (SoC) design at the system level to create a new type of server.

This evolution is comparable to the transition from mainframe computers to mass-produced personal computers (PCs) in the 1980s, which in turn evolved into modern servers. With smartphones the contemporary equivalent of 1980s PCs, now is the time to take advantage of their architectural flexibility and evolve them to create the energy-efficient servers of the future.

## GREEN COMPUTING NODE FOR EUROPEAN MICRO-SERVERS

At the time of writing, the consortium is in the final stages of results evaluation that will be released in the project workshop at the HiPEAC 2017 Conference in Stockholm (25 January 2017). These results compare Intel XeonD, ARM Juno, Gtabyte MP30AR0 ARM X-Gen1 and the EUROSERVER prototype platforms.

The the EUROSERVER platform is based on a Xilinx UltraScale+ FPGA that demonstrates novel technologies built in the project. A number of relevant workloads are being evaluated including web-server hosting (LAMP/WAMP), distributed databases (HADOOP) and network communications (C-RAN). ARM based processors currently dominate the mobile market and EUROSERVER is attempting to integrate the full stack as a power-efficient alternative to the Intel-based designs that currently dominate the data centre.

Please find the most up-to-date set of results on the EUROSERVER webpage.



EUROSERVER has received funding from the European Union's FP7 programme under grant agreement no.610456. For more information, visit [www.euroserver-project.eu](http://www.euroserver-project.eu) or contact Ms. Isabelle Dor - [isabelle.dor@cea.fr](mailto:isabelle.dor@cea.fr)  
About KALEAO: visit [www.kaleao.com](http://www.kaleao.com)  
About ZeroPoint: visit [www.zptcorp.com](http://www.zptcorp.com)



## Annex 5: Date 2016 – EUROSERVER paper

## EUROSERVER: Share-Anything Scale-Out Micro-Server Design

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**Abstract**—This paper provides a snapshot summary of the trends in the area of micro-server development and their application in the broader enterprise and cloud markets. Focusing on the technology aspects, we provide an understanding of these trends and specifically the differentiation and uniqueness of the approach being adopted by the EUROSERVER FP7 project. The unique technical contributions of EUROSERVER range from the fundamental system *compute unit* design architecture, through to the implementation approach both at the *chiplet* nanotechnological integration, and the *everything-close* physical form factor. Furthermore, we offer optimizations at the virtualisation layer to exploit the unique hardware features, and other framework optimizations, including exploiting the hardware capabilities at the run-time system and application layers.

## I. INTRODUCTION

There is growing business interest in *microservers*, i.e. clusters of high-density, low-power servers, which are suited to the growing number of hyperscale workloads found in modern data-centres [1]. Although still in their infancy and not yet widely used in production, microservers show promise of allowing the total compute, network, and storage resource capacity of a data-centre to be utilized with high flexibility and efficiency for a wide range of diverse workloads.

The EUROSERVER FP7 Project Consortium develops a micro-server solution tailored for the workloads running on today's cloud infrastructure [2]. The EUROSERVER platform combines several architectural key features, such as highly efficient ARMv8 processors, an innovative scalable memory scheme called *Unimem*, a lightweight hypervisor platform suitable for micro-servers called *MicroVisor* and the use of Hybrid Memory Cube (HMC) technology to maximize memory storage density and bandwidth. EUROSERVER adopts an innovative structure based on interconnected compute “coherence islands” for an optimal balance between data locality and transfer efficiency. The compute SoC internal structure is organized around several independent *chiplets* implementing the

coherence islands. The coupling between chiplets is realized via high-speed serial links. Physically, the system is integrated onto a cost-effective organic interposer solution.

The emerging key differentiator for EUROSERVER is improved resource utilisation [3]. Just as cloud computing and virtualisation enables companies to consolidate workloads from many distributed and under-utilised hardware platforms into smaller numbers of servers, EUROSERVER proposes to more efficiently exploit micro-server and low-power hardware in order to pave the way towards the next generation of more power-efficient servers.

The rest of this paper is organized as follows. Section II presents a review of industry trends towards the development of commercially viable microservers. In Section III we present the system approach of the EUROSERVER consortium to address both technical and economic challenges so as to enable commercially viable devices that can be also optimized for market specific requirements. We also outline our software stack that supports cloud workloads on top of a microserver platform. Finally, Section IV summarizes our conclusions.

## II. REVIEW OF INDUSTRY TRENDS

In this section we present a snapshot summary of the trends in the area of micro-server development and their applications in the broader enterprise and cloud markets.

The most dominant trend across the server market continues to be based on adaptation of technology around the historic PC architecture based platform. This platform has evolved over the decades since it was first introduced in support of the early personal computer, but fundamentally, even the most modern server still follows the same model:

- The platform is complete, in the sense that it can only exist in a complete form. The balance between the processing/memory and I/O are fundamentally defined

The whole paper can be uploaded at: <https://www.date-conference.com/proceedings-archive/2016/html/1022.xml>

## Annex 6: EUROSERVER workshop program – HiPEAC 2015

### EUROSERVER : Green Computing Node for European Micro-Servers

22 January 2015

The workshop goal is to explore the alternative to EUROSERVER main innovative topics (i.e. memory management, distributed execution, IO virtualisation and power management) and to confront the project vision with other projects or industrial perspectives

#### Agenda

2pm – 2.45 pm « **Towards PetaRAM servers with Scale-Out NUMA** »

by Boris Grot (School of Informatics, University of Edinburgh)

2.45pm – 3.15pm « **Platform device assignment to KVM-on-ARM Virtual Machines via VFIO** »

by Antonios Motakis (Virtual Open Systems)

3.15pm – 3.40pm « **Microvisor : A Scalable Hypervisor Architecture for Microservers** »

contributions from X. Ragiadakou, M. Alvanos, J. Chesterfield, J. Thomson, M. Flouris - OnApp

*presented by Julian Chesterfield*

3.40pm – 4pm ~Coffee break~

4pm – 4.25pm « **Software Mechanisms for ARM Microserver Internal/External Communication Using Shared Memory and RDMA** »

contributions from D. Poullos, J. Velegrakis and M. Marazakis – Institute of Computer Science (ICS)-FORTH.

*presented by Dimitrios Poullos*

4.30pm – 4.55pm « **Energy-aware Scheduling for Task-based Applications** »

contributions from F. Juarez, J. Ejarque and Rosa M. Badia – Barcelona Supercomputing Center (BSC)

*presented by Jorge Ejarque*

5pm – 5.25pm « **Blaze Memory : A highly Efficient Memory Compression Add-on in Server Systems** »

contributions from A. Arekalis, C. Alverti and P. Stenström – Department of Computer Science and Engineering, Chalmers University of Technology

*presented by Per Stenström*

## Annex 7: EUROSERVER workshop program – HiPEAC 2017

### EUROSERVER: Assessment and Perspective for the Future of Microserver servers

25 January 2017

Through invited talks and discussion, the workshop highlights the project's technical results and impact. Representatives of KALEAO and ZeroPoint have been invited to participate, in order to offer their practical perspective on the commercialisation of project results.



▶ 10:00 – 11:00: **Panel Discussion**

Kaleao, Zeropoint Technologies



▶ 11:00 – 11:30 : **coffee break**



▶ 11:30 – 1:00: **Technical session**

BSC, Chalmers, Forth, OnAPP, TUD



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**EUROSERVER Workshop**



▶ **Panel session**

- ▶ *Presentation of Kaleao scale-out hyperconverged server platform*  
John Goodacre - Kaleao
- ▶ *Presentation of ZeroPoint Technologie unique memory compression system*  
Per Stenström – ZeroPoint Technologies

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**EUROSERVER Workshop**



▶ **Technical session**

- ▶ *New approach for memory management capacity across multiple nodes based on UNIMEM architecture and Xen's TMEM abstraction*  
Luis Garrido - BSC
- ▶ *HW Techniques for high-performance and fair management of hybrid memory*  
Dmitry Knyagin - Chalmers
- ▶ *Efficiency concerns for in-memory data centre workloads running on energy-efficiency servers*  
Manolis Marazakis - FORTH
- ▶ *Fine-Tuning the performance of low power micro-servers; experiences and findings from the EUROSERVER project*  
Michail Flouris – OnAPP
- ▶ *Data flow modeling and run-time scheduling for CRAN applications,*  
Emil Matus - TUD

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