PUBLISHABLE EXECUTIVE SUMMARY

NANOPACK is a European large-scale integrating project aiming at the development of new technologies and materials for low thermal resistance interfaces and electrical interconnects, by exploring the capabilities offered by nanotechnologies (such as carbon nanotubes, nanoparticles and nano-structured surfaces) and by using different mechanisms to enhance interparticle contact formation, compatible with high volume manufacturing technologies. Several key research areas relative to thermal management interconnects and packaging are addressed by European industrial and academic partners: thermal interface materials, assembly, reliability, and characterisation; supported by world class modelling and simulations. The benefits of the technologies were evaluated in different applications to demonstrate improved performance of microprocessors, automotive and aerospace high-power electronics.

As the project reached its end, the main materials and process developed in the project were implemented in a series of five relevant industrial demonstrators and one characterization tester. The demonstrators addressed a wide range of applications:

- ***high power amplifier***
- ***microprocessors***
- ***automotive electronics***
- ***security systems***
- ***off-shore electronics***

Each application had specific requirements which lead to specific thermal interface materials (TIM) and technological choices among a variety of products and processes such as highly conductive adhesives and greases, metallic nanosponges, carbon nanotube-based thermal pads or metal-polymer composites. The criteria for material selection were ranging from thermal conductivity and thermal resistance performance to targeted bond-line thickness and assembly pressure. Even though it was found that there exists no "universal" TIM which meets all requirements at once. for each criterion an outstanding material has been developed.

Fine characterization of the chosen technologies (performance and reliability) was performed and major conclusions could be drawn:

- ***Partners found in each of the application areas that the selected TIM materials showed a stable performance before, during and after the tests. For example, even those materials which increased their thermal resistance over time slightly remained below the acceptance criteria. These positive results show that the reliability tests carried out on the TIMs themselves at the material selection stage were sufficient and gave the right prediction.***
- ***When used in the demonstrators, some NANOPACK materials outperform commercial TIMs but all the materials were found acceptable in terms of their overall performance.***
- ***All the material evolutions during the aging tests are acceptable regarding to an industrial use and are therefore good candidates for the usage in Automotive and Avionics Systems.***
- ***For all NANOPACK materials it can be stated, that their final application in industry depends on their cost-effectiveness.***

➢ Main scientific and technological achievements

Thermal Interface Materials

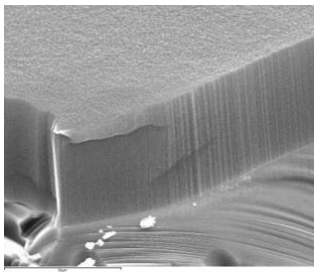
These materials are typically found between the microprocessor chip and heat spreader, as well as between the heat spreader and heat sink. Interface materials are subject to challenging requirements, including the ability to reduce mechanical stress between regions with vastly differing thermal expansion coefficients, the ability to be reworked, low viscosity at application temperatures, and high thermal conductivity.
At the beginning of the project, common TIMs included a variety of polymer-based materials with high thermal conductivity particle inclusions, typically with diameters of 2-25 µm.
The effective thermal conductivities of particle-filled polymer interface materials were typically about one order of magnitude higher than the polymer matrix alone, i.e. of the order of 2-4 W/mK.
The thermal resistance of interfaces found in commercial products could be substantially larger than anticipated values (typically 10-20 Kmm²/W) owing to resistances at the TIM boundaries and small voids.

The materials and processes developed in the project consequently improved the state-of-the-art:

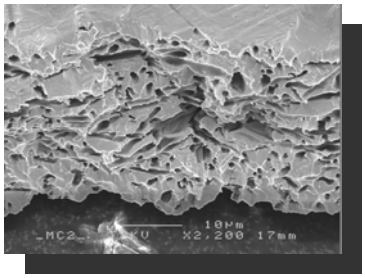
High performance Electrically Conductive Adhesives (ECA) using bimodal fillers in a bi-epoxy matrix with flexibilizers. Main characteristics are: k=10W/mK, Tg>180°C, visc<60 Pa.s, Res=6.10^{-5} Ωcm. These materials were transferred to a Swedish spin-off from Chalmers University: Smart High Tech SHT AB for commercialization.

High k greases for high BLTs have been produced with thermal conductivities in the range of 11 W/mK, using bi- and tri-modal materials (CNT, micro Ag/graphite, silicone) for high BLT > 75µm.

Thermal interfaces based on Vertically Aligned CNTs infiltrated by paraffin have a thermal resistance of Rth=4.0 Kmm²/W for a BLT=50µm, resulting in an effective thermal conductivity of keff=17 W/mK. A T° decrease of up to 5°C (31% reduction of the temperature increase) was demonstrated using VACNT based interfaces for high power LED cooling as compared to using a commercial grease. Furthermore, a process allowing the transfer of the VACNT assembly in a thermal interface via metal or specially formulated and synthesized polymer (« HLK5 ») allow transfer of the VACNT assembly while keeping low thermal resistance (1.4mm²K/W for a 10µm BLT).



Metal-polymer nano-composite made of Polymer (Polyimide) fiber network infiltrated with PCM metal alloy show extremely high thermal performance: 18 W/mK of effective conductivity with InSnBi alloy (Eutectic 60°C) and more than 24 W/mK with pure In (Eutectic 160°C). This technology has demonstrated its efficiency by comparison with commercial material (TC5022) used to assemble HP LEDs (24W): Rth decrease by 65%. It is now being transferred for volume manufacturing.



The main results of the NANOPACK project concerning the major issues of Thermal Interface Materials are reported in the following table:

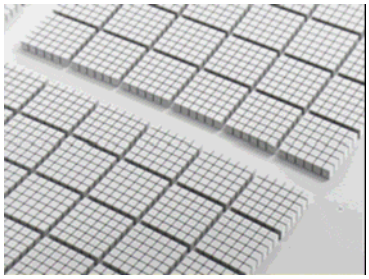
Criteria	State-of-the-art	NANOPACK Goals	NANOPACK Achievement
k_{TIM}	4 W/mK	20 W/mK	24 W/mK
R_{th}	20 Kmm²/W	2 Kmm²/W for BLT<35 µm 5 Kmm²/W for BLT>35 µm	VaCNT: 1.4 Kmm²/W for BLT 10µm sintered-Ag = 50 x lower Rth cf. soldered (5 times lower BLT for same reliability, 10 x thermal conductivity)
BLT	35-100 µm	10-100 µm	6 µm

k = thermal conductivity; R = thermal impedance; BLT = bond line thickness

All the initial goals have been reached.

Thermal Interface Assembly

As the industry has known for several decades, the bulk conductivity of materials mixed with particles is strongly related to the volume percentage of particles mixed into the viscous oil matrix. However as the interface material is mixed with an ever larger amount of particles, it is difficult to squeeze the material to the same thin gap as a low filled material due to the high viscosity of the material and the formation of particle stacks that block further compression. A new material with improved bulk conductivity is only useful if it can be squeezed to an equivalent or thinner thickness than existing materials.



Researchers involved in the NANOPACK project discovered a new technology to reduce the required load to squeeze high viscosity materials and to prevent particle stacking during bond line assembly. The technology, called **Hierarchical Nested Channel (HNC)**, uses a network of channels formed into one of the interface surfaces to provide parallel flow paths for the high viscosity material and also to define a more uniform radial pressure drop as the material flows out of the interface – preventing segregation of the particles from the oil matrix. It has been tested on 20 materials: from 20 to 90 % improvements have been observed on 1-250cm^2 interfaces. As example, with the EVAC low-viscosity screen-printable non-adhesive formulation, the final BLT was reduced by 78% and reached 98% faster than the non-HNC case.

The main results of the NANOPACK project concerning the major issues of Thermal Interface Assembly are reported in the following table:

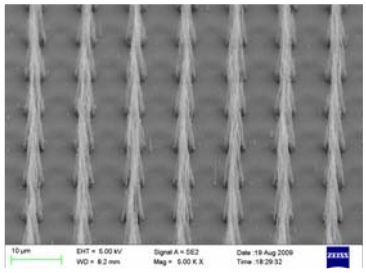
Criteria	State-of-the-art	NANOPACK Goals	NANOPACK Achievement
Assembly pressure (20x20mm)	5 bar	2 bar	Material dependent: max. reduction to 50% with HNC
Assembly load	800 N	< 200 N	60 N
Cure/Reflow T°	210-260 °C (Pb free)	< 150 °C	Nano-TIM 60 – 180°C

All the initial goals have been reached.

Interconnects

Electrical interconnects in high power devices are often another important heat dissipation path. These interconnects should be able to withstand hugh current densities and have a good long term reliability.

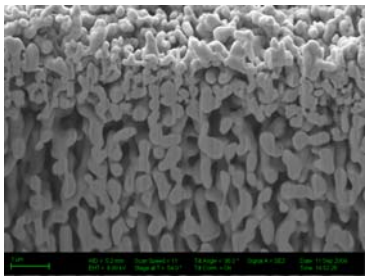
CNT interconnect structures were actively pursued for next generation ULSI devices. CNT interconnects, especially CNT via structures, can not only support a large current density but they also can be used as heat spreaders to dissipate heat from local hot spots. In 2013 the ITRS predicts a current density of 3.3x106 A/cm², a value which, to date, can only be supported by CNTs, where current densities of 1010 A/cm² in nanotubes without heat sinks have been reported. Flip chip assembly using CNT bumps was realized with 150°C transfer of the 10µm (and even 4µm) pitch CNT bumps on patterned adhesive. Electrical characterization yielded 2 Ω for 3x3mm².



CNT interconnects

Pure metal contacts were also considered. As is well known, pure metals show a thermal conductivity of one order of magnitude higher than solder alloys for eutectic die attach, which are one class of materials of choice for power applications. However, to reduce the process temperature and make a metal bond feasible one has to exploit a nano effect: Interdiffusion of nano-powders forms a pure metal interconnect at much lower temperatures (T < 350 °C) and is therefore eligible for use with silicon power dies.

Ag-Sintered & Au-Nanosponge : these technologies take thermal benefit from the high k of Ag and Au and mechanical benefit from the porosity of the structure (accommodation of the empty space under constraint). The Au-nanosponge is produced by etching Ag from electroplated Au-Ag alloy to obtain open-porous nano-scale (15 nm) structures. The Ag-sintering technic is a monometal Ag powder bonded at low T° and low pressure for a high resulting conductivity: k= 370W/mK.



Au-Nanosponge

The main results of the NANOPACK project concerning the major issues of Interconnects are reported in the following table:

Criteria	State-of-the-art	NANOPACK Goals	NANOPACK Achievement
Pitch interconnects	200 µm	< 150 µm	Chalmers CNT 10 µm (direct growth) 40µm (transfer)
Electrical interface	10 mW	5 mW	4m W (Nano-Sponge)
Processing T°	> 200 °C	< 150 °C	120 °C (glue) 150°C (solder)

All the initial goals have been reached.

Thermal Characterisation

Advanced methods in the study of thermal properties in the nanometer scale need to be applied to understand better the issues in nanomaterials and nanodevices since agreement between theory and experiment is generally unsatisfactory. The deployment and improvement of the most suitable techniques, methods such as *time-domain thermoreflectance* and the *3-omega,* were addressed to understand thermal conductivity as well the study of confined acoustic phonons to understand their properties and role in thermal transport in nanoelectronic relevant materials and structures thereby pushing the state of the art in this field

The main results of the NANOPACK project concerning the major issues of Thermal Characterisation are reported in the following table:

Criteria	State-of-the-art	NANOPACK Goals	NANOPACK Achievement
3-ω method in nm-scale	A few W/mK in III-V semiconductor alloy epitaxial films of 700 nm thickness.	Keep the sensitivity of few W/mK applied to crystalline samples with sub 100 nm thickness.	Sub 100nm if substrate conductive Sensitivity below 1 W/mK*
Use confined acoustic phonon data for thermal simulations in the nanoscale	None available. Confined phonons have recently been observed in 30 nm thin films of SOI.	Provide measurements to underpin simulation tools and enhance their predictive nature for thermal properties in the nm-scale	8nm thin films measured Numerical code for phonon dispersion available
Steady state thermal resistance resolution	5-10 Kmm²/W	1 Kmm²/W	1 Kmm²/W

*** Very difficult to discriminate R_{tbr} and reduction in λ**

All the initial goals have been reached.

Interface reliability

Apart from thermal performance, thermo-mechanical reliability is the other important aspect for successful development of cooling solutions, as thermally induced mechanical stresses and strains can cause interface failure, which then leads to decisive conductivity reduction in the heat path, thus causing fatal failure by overheating. So thermo-mechanical design is a key-issue for thermal management concepts.
Interface failure evaluation by a combined experimental and computational study requires the knowledge of failure criteria. These failure criteria, which enter the simulation as a critical parameter thus allowing prediction of interface failure, have to be determined experimentally.

During the project, a simple method was developed to quickly determine subcritical crack propagation, A modified compact tension (MCT) specimen has been designed and optimized for comparison with numerical results obtained from FE simulations for crack propagation for NANOPACK materials.

The main results of the NANOPACK project concerning the major issues of Interface reliability are reported in the following table:

Criteria	State-of-the-art	NANOPACK Goals	NANOPACK Achievement
Speed of test cycle by lifetime models	Trial and errors as long as needed	6 weeks	1000 Test Cycles for LTM in 6 weeks MCT = simple, fast low-cost test for subcritical data.
Lifetime models for new technologies of low-Rth TIMs	Not available	Lifetime models based on physics of failure mechanisms	LTM established for sintered-Ag die attach. Plastic strain as failure criterion. Calibrated for 3 design parameters.

MCT = Modified Compact Tension; LTM = Life Time Model

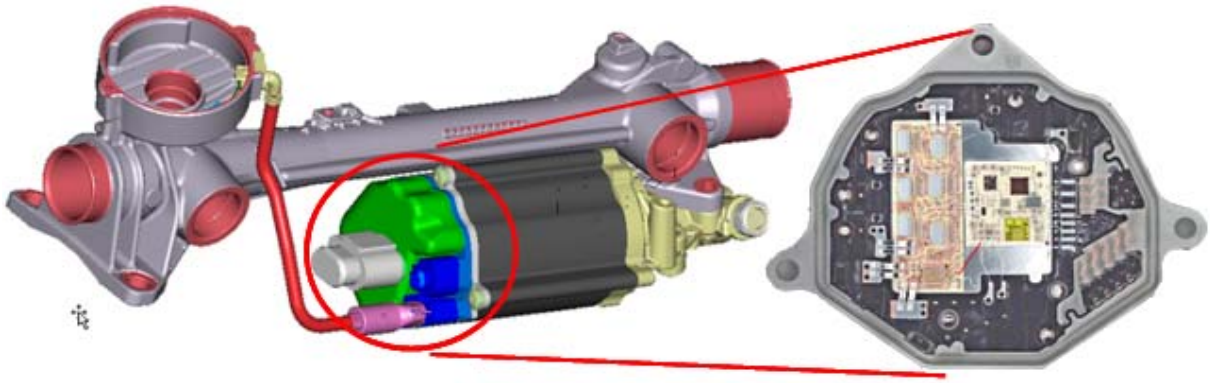
All the initial goals have been reached.

➢ NANOPACK Demonstrators

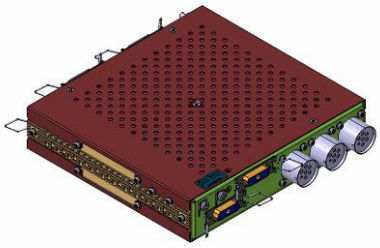
The demonstrators for different markets/applications (e.g. automotive, avionics, supercomputing) were defined and technologies were selected. Following the design of the demonstrators, suitable TIMs were found for each demonstrator, as the requirements were different in terms of material classes (greases, thermal pads, adhesives…). The demonstrators where then built and thermal measurements were performed as well as reliability tests.
A description of the demonstrators is given below, and the major achievements are summarized in a table. The details of the built-up and characterization can be found in the appropriate deliverables available online at www.nanopack.org.

Automotive Applications (Bosch)

Bosch worked on the power amplifier module from a commercial electrical power steering unit used in cars (automotive). Main components of this module are power transistors mounted on a direct bonded copper (DBC) ceramic substrate. To limit the heat created in the transistors, the DBC substrate is mounted on an Al-base-plate as a heat spreader using TIMs. This heat flow can be optimized by reducing the BLT, increasing the thermal conductivity of the TIM or by reduction of the thermal interface resistance between Al and DBC.



Avionic Applications (Thales)



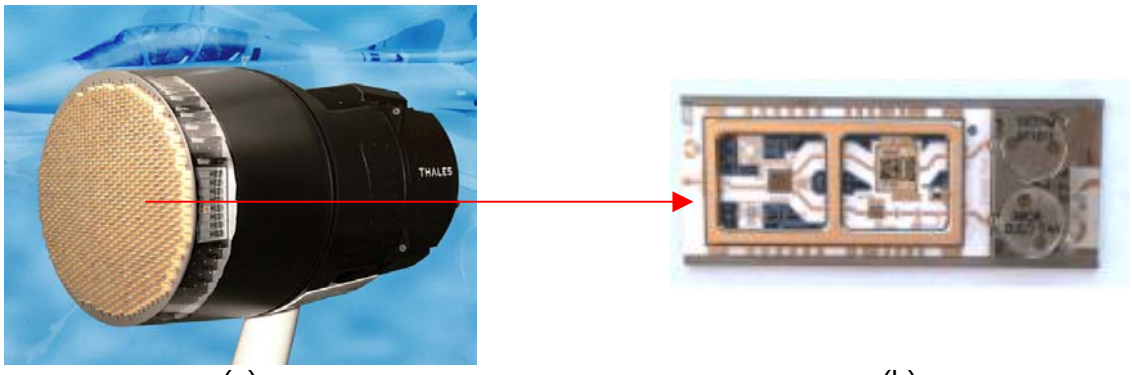
THAV worked on avionics equipments used in civil avionics for In Flight Entertainment Systems (IFE). This equipment is representative of the main thermal constraints which are encountered in most of their products: this equipment is a Seat Electronic Box (SEB) which is placed just under the passenger seat in small enclosed zones. This SEB has many hot spots and is cooled only by natural air convection. For the thermal management of this equipment a two-phase change systems like heat pipe or loop heat pipe was proposed in order to transfer the heat from the component to the SEB wall (with heat pipe) or from the SEB wall to an external heat sink or cold structure (for instance the old mechanical structure of the seat) with the use of loop heat pipe.

This thermal management induces many thermal interfaces that need to be correctly managed in order to keep a good efficiency for global thermal path.
The demonstrators integrates many thermal interfaces inside the SEB:

- between components and heat pipe
- between PCB and heat pipe
- between heat pipe and mechanical structure.

Aerospace Applications (Thales)

Active phased array antennae are key products of THALES who sells them as major equipments in integrated systems for high-end defense, security, surveillance, space or telecom applications. They are compound of multiple (up to several thousands) individual T-R modules, whose role is to Transmit/Receive signals synchronously with phase and amplitude control between them. This antenna architecture allows to steer the beam electrically (i.e. without any mechanical movement), to shape the beam or to generate several beams. Moreover, if one of the T/R modules breaks down, the performance of the whole antenna is not decreased and the maintenance is simplified. In brief, this type of antenna provides a very powerful and agile radar system.

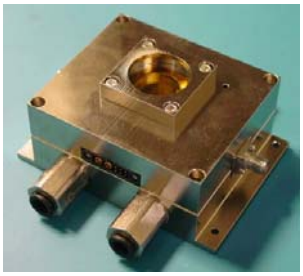


(a) (b)

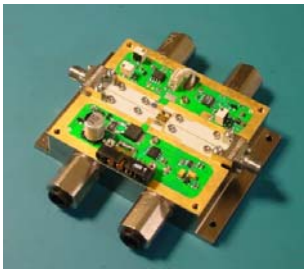
(a) THALES Phased Array Antenna; (b) T/R module

A typical T/R module is composed of a transmitter path, a receiver path, a circulator to switch from one path to the other one and a radiating element to emit/receive the signal. TRT realized a high power amplifier (HPA) demonstrator in a THALES representative application, i.e. a X-band RF power amplifier. Packaging the HPA requires the use of thick and highly conductive grease and electrically conductive adhesive as die attach. The thermal management is thereby a key element in

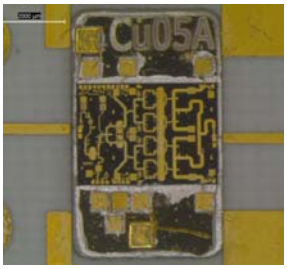
the success of the antenna. The HPA (High Power Amplifier) demonstrator is aimed to evaluate the performance of new high performing TIM (among which the Vertically Aligned Carbon NanoTubes). The thermal interface of interest is between the HPA die and the chip case (TIM1). In this demonstrator the packaging of the HPA is designed to be representative (in terms of staking, dissipated power, material and interfaces thickness and surface roughness) of a face down BGA (Ball Grid Array) HPA that could be used in active Phased Array Antenna T/R modules.



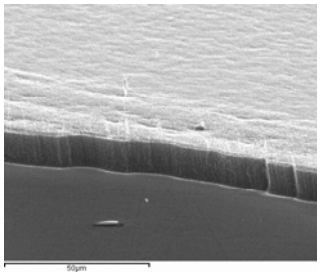
HPA Module



HPA circuit



HPA MMIC



VACNT as TIM1

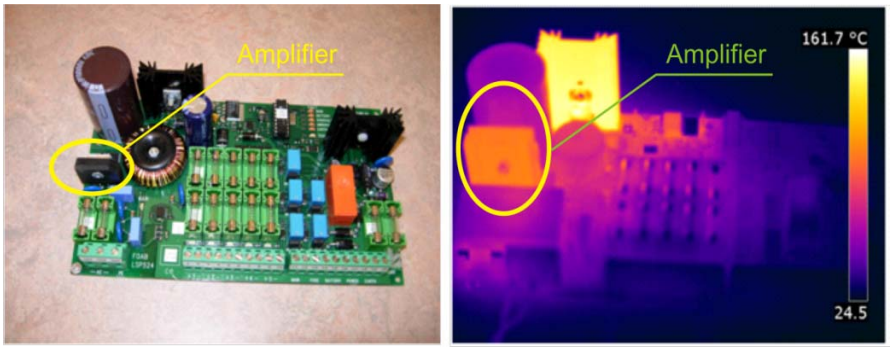
Microprocessor for IT Applications (IBM)

The future trend in IT industry will be to replace the traditional air heat sinks with high efficiency liquid coolers. The application of high efficiency micro-channel coolers reduces the overall thermal resistance from the microprocessor junction to the coolant, whereby the impact of a low TIM resistance becomes more prominent. The objective of the present effort was to demonstrate the feasibility of the developed materials and processes to provide low resistance thermal interfaces (<2 Kmm²/W) usable for TIM1 or TIM2 interconnects in microprocessor. A commercial available HS22 blade was chosen for the demonstrator with a high performance Intel Xeon X5560 CPU. The blade was modified, where we replaced the traditional air heat sink with a liquid cooled micro-channel cooler.

The figure besides depicts an image of a liquid cooled HS22 blade. The CPUs are cooled by two cooper micro-channel cold plates, which are built into the package lids. The cold plates itself provide a thermal resistance of 10 mm^2K/W. A dramatic reduction in TIM resistance should demonstrate a strong impact on the overall thermal performance of the cooling solution.

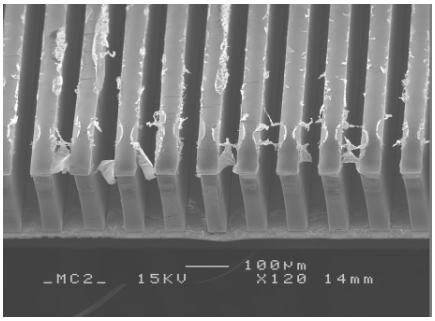
Integrated Microcooling for HP electronics (FOAB)

FOAB aimed to develop a miniaturized heat sink which enables effective heat dissipation in a security system. The amplifier in the security system is a high-power component and is typically cooled down by natural convection. The temperature on the amplifier can go up to 130 ˚C when working, as shown in the figure below.



Left: the high-power amplifier located in a security system.
Right: infrared image showing the temperature profile over the circuit board

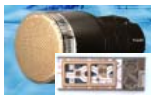
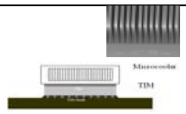
A microchannel cooler was designed for high efficiency on-chip cooling based on simulation results. The structure of the microchannel cooler is illustrated above. The fins used to form microchannels are made of carbon nanotubes (CNTs), which show great potential in thermal management in electronics due to their extremely high thermal conductivity.



CNT fins transferred onto demonstrator platform

In order to fabricate the microchannel cooler structure, a CNT transfer technique has been developed. An ultrafast metal enhanced CNT transfer technique was used to address the most challenging obstacles to overcome in using CNTs in electronics: the weak van der Waals force and the high electrical and thermal resistance between as-grown CNTs and the supporting substrate.

The main results of the NANOPACK project concerning the demonstrators are reported in the following table:

Partner	Demonstrator	Approach	State-of-the-art	NANOPACK Goals	NANOPACK Achievements
MicReD		Harware based numerical derivation	Measurement resolution: 0.012K Sampling rate: 1µs	Measurement accuracy: 5-10% at 10 W/mK Sampling rate: 0.1µs	Measurement accuracy <5% at 10W/mK ☺
IBM	 2 demonstrators: TIM2 & HNC +TIM2 for IBM Blade HS 22	Reduce gap, increase conductivity, surface optimization	Rth: 13 Kmm²/W BLT ~ 50 µm	Rth: 4 K/mm²/W, BLT ~ 50 µm @1bar, Area 20x20mm	Rth: 19 Kmm²/W 😐 BLT = 70 µm @ 1bar 😐 Area 20x20mm ☺ Reliability: Good ☺
TRT	 2 demonstrators: Airborne Phased Array Antenna, Transmitter/Receiver Module	Rth reduction by surface optimization and improved thermal conductivity	Power density 0.44 W/mm²	Power density 22 W/mm²	Max Power density: 21 W/mm² ☺ 19% reduction of the temperature increase with VaCNT TIM ☺
THAV	 Seat Electronic Box (SEB) for In Flight Entertainment	Heat pipe spreaders using nano TIM	Rth: 100 Kmm²/W	Rth < 20 Kmm²/W BLT 100-250µm	Rth < 20 Kmm²/W BLT ☺ BLT = 160 µm ☺ Conduct.> 10.5 W/m.K 😐 Good aging behaviour ☺
Bosch	 Electrical power steering (ESL3)	Rth reduction by surface optimization and improved thermal conductivity	Rth 20 Kmm²/W BLT 100-150 µm	Rth < 40 Kmm²/W BLT < 100 µm Visc. = 30-200Pa.s	Rth <= 40 Kmm²/W ☺ BLT = 80 – 100* µm ☺ Viscosity = 200–300 Pa.s 😐 * Through process change
FOAB	 Flip chip backside cooling with nano-TIM and microcooler		Power density: 2 W/mm² Stability 1000h at 85°C/85%r.h.	Power density: 3 W/mm² Stability 2000h at 85°C/85%r.h	Power density > 17 W/mm², stability 250 h in 20-85 °C ☺ ☺

The major conclusions and lessons learned from the NANOPACK project are

- It is not possible to develop a “universal” TIM which meets all the requirements for different demonstrators. For example: the high filler content results in high conductivity, but causes high viscosity and leads to difficulty to process the grease. A compromise must be found to meet both requirements. Efforts have been made to reach high conductivity/low resistance with suitable processability.
- To find the optimal TIM, it is necessary to define the relevant material properties which are essential for the assembly/product (thermal conductivity, viscosity, industrial process compliance,…)
- In selecting a TIM for an assembly, it is important to consider both the thermal properties but also the stability of these properties over lifetime. Therefore, material testing is necessary to select potential TIMs, but it is essential to do reliability testing on an assembly close to reality.

➢ Further information

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