Nano Packaging Technology for Interconnect and Heat Dissipation

June 2009 **Newsletter #3**

NANOPACK is a European large-scale integrating project aiming at the development of new technologies and materials for low thermal resistance interfaces and electrical interconnects, by exploring the capabilities offered by nanotechnologies (such as carbon nanotubes, nanoparticles and nano-structured surfaces) and by using different mechanisms to enhance interparticle contact formation, compatible with high volume manufacturing technologies. Several key research areas relative to thermal management interconnects and packaging are addressed by European industrial and academic partners: thermal interface materials, assembly, reliability, and characterisation; supported by world class modeling and simulations. The benefits of the technologies will be evaluated in different applications to demonstrate improved performance of microprocessors, automotive and aerospace high-power electronics and radio-frequency switches.

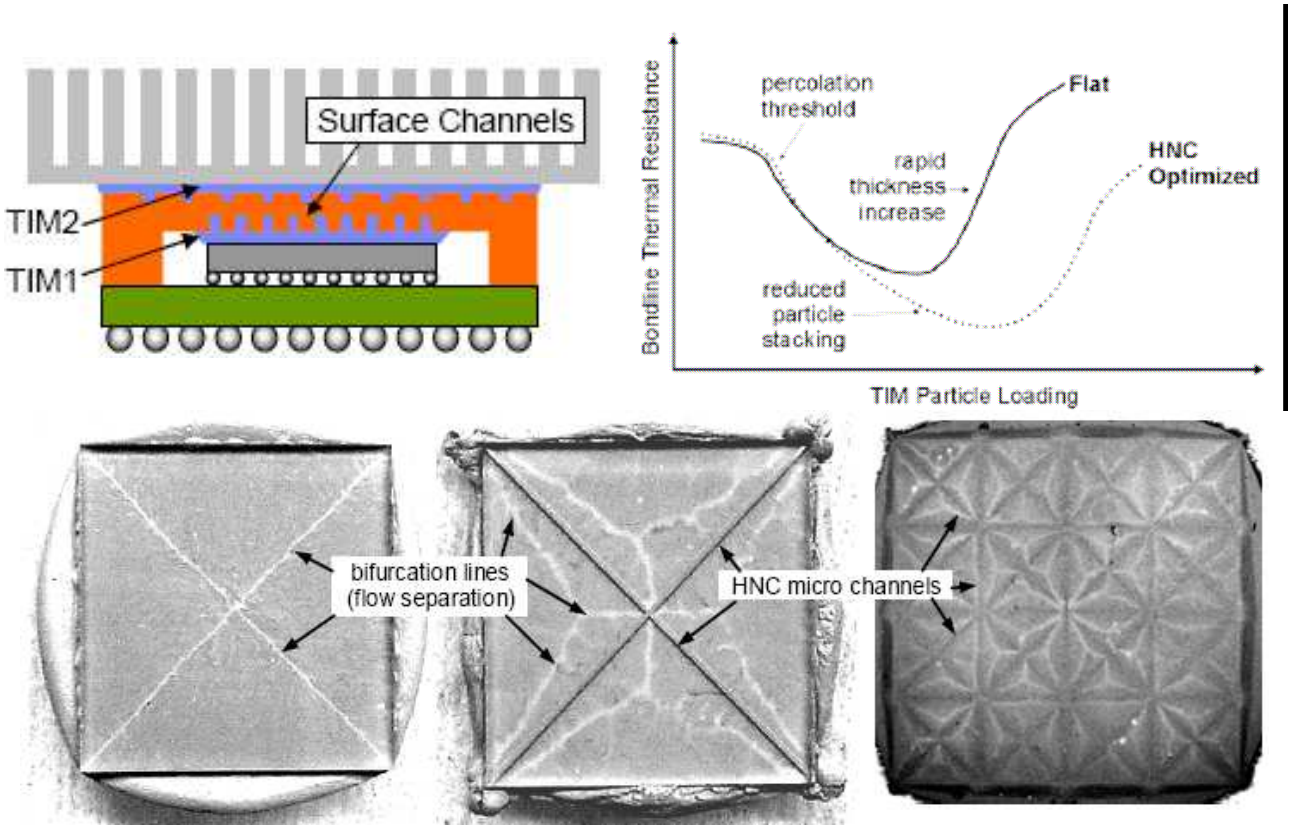
At midterm of the project, this third issue of the NANOPACK newsletter intends to present the major events of the project's and consortium's lives as well as the major advances in the fields of material development, process optimization, test system construction and modelling.

Congratulations to the IBM team for the IEEE Harvey Rosten Award for Excellence 2008!

Alongside the IEEE Semitherm conference in San Jose, on March 19, Ryan Linderman, Thomas Brunschwiler, Urs Kloter, Hilton Toy and Bruno Michel were rewarded for their outstanding work in the field of thermal analysis of electronic equipment.

Awarded were the concept, implementation and application of:

- directing particle placement by means of channels cut into the surface of a chip or heatsink and,
- reducing the gap thickness despite higher viscosity andhigher particle fill factor by means of a hierarchical set of channels.
- formulating a thermal paste with higher matrix viscosity to delay the onset of particle stacking to higher fill factors



The award committee especially mentioned the exemplary way how research from different fields like biology, physics, materials sciences, and engineering was combined in an interdisciplinary fashion and how a research concept was brought to a technological application in a short time.

The NANOPACK consortium is very proud that the scientific and technical excellence of one partner is world wide recognized. Congratulations!

Progress in Material Developments

Highly thermally conductive adhesives (up to 9.5 W/mK) and greases (up to 6 W/mK)

A previous state-of-the-art survey has revealed that the thermal conductivity of high-performance thermal greases and adhesives falls in the range of 3 to 5 W/mK (for instance one of the best commercially available thermal greases measured by the consortium is Shin-Etsu G-751 with 4.7 W/mK). Several trimodal greases have been developed on the basis of graphitized carbon nanofibers, metal and graphite micro particles, dispersed in a silicone with dilutes epoxy matrix. Varying the loading grades has allowed reaching bulk thermal conductivities up to 6 W/mK. These greases still have to be improved by reducing the viscosity which is actually high and prevents from reaching low BLTs.

The performance obtained with the new adhesives is even higher since 9.5 W/mK have been reached in cross plane direction. Two remarkable products have been developed: silver flakes and micro silver spheres have been dispersed in mono- and multi-epoxy matrix. The respective thermal conductivities are 6 and 9.5 W/mK. These adhesives are electrically conductive ($6.10^{-5}\Omega$.cm). The shear strength of the mono-epoxy matrix products has been measured to 14MPa which is also remarkable and suggests excellent mechanical and reliability properties.

Electrically conductive adhesives for die attach applications

Die attach applications require the use of adhesives with thermally conductive properties but also electrically conductive properties as well as a good workability and a high resistance to high working temperatures. To reach all these properties, highly filled materials must be used to fulfil thermal and electrical requirements, but particular efforts must also be carried on the matrix to reach high reliability and high resistance to temperatures.

Heat resistant conductive adhesives composed of a multi-functional epoxy matrix containing Ag flakes (85 wt%) have been developed. The adhesives are potentially stable up to 200-250 ˚C because the primary relaxation mechanism of the matrix resin occurs at ~250 ˚C. Adhesives cured under appropriate curing conditions exhibited relatively low electrical resistivity and high thermal conductivity (up to 25 W/mK in plane direction and 5 W/mK in cross direction). Because the reactive diluent influences the electrical and thermal properties as well as the thermo-mechanical properties of the adhesives, the selection of the most appropriate reactive diluent will be the key to developing conductive adhesives that exhibit superior heat resistance.

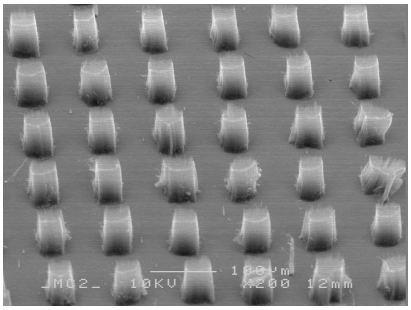
Other bimodal electrically conductive adhesives (Ag flakes + Ag nano-spheres in mono-epoxy matrix) developed by Chalmers have been applied on special designed die attach by FOAB for shear and reliability tests. The shear strength showed higher value (14MPa) than other types of commercial products. Preliminary reliability tests are very positive.

Screen-printable electrically conductive adhesives have also been fabricated with carbon nanotubes or nano-fibers as fillers to study the enhancement of electrical conductivity over temperature post treatment.

Progress in Process Optimization

Fine pitch electrical and thermal interconnects based on carbon nanotubes

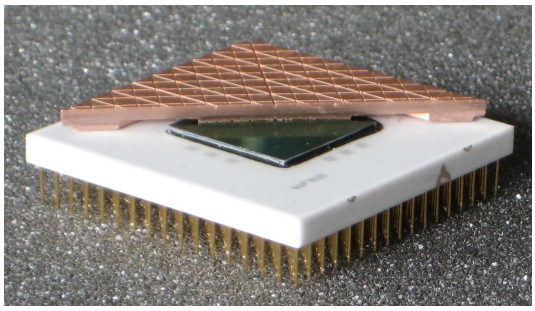
In this work led by Chalmers, CNTs are proposed as a promising candidate material to make future flip chip interconnects due to their good mechanical, electrical and thermal properties. To realize CNT-based interconnects, the main effort has been on the development of CNT flip chip bumps on different materials, with a concern with the compatibility with existing materials and processes. Post-growth processes, such as deposition of metallic layers on CNTs and low temperature transfer of CNTs (using patterned isotropic conductive adhesive films) have been developed to overcome the difficulties of utilizing directly synthesized CNT bundles as flip chip bumps.



CNT bumps transferred on Si/Au substrate with a low temperature process

Surface modification techniques for thermal interfaces

Increasing bulk conductivity of TIMs is one of the research routes followed by the consortium to reduce the total interface resistance. Another route corresponds to surface modification techniques to reduce the BLT and contact resistance of interfaces. One demonstrated and promising approach is to modify the interface surfaces by implementing hierarchical mini- and micro-channel structures in the solid interface to control the bond line formation during assembly. This technology is called hierarchically nested channels (HNC). Others approaches able to further reduce the interface resistance in thin BLT interfaces that are currently considered in the consortium include: Sintered-Ag interconnects, Au-nano-sponges surface enhancement and CNT-based technologies.



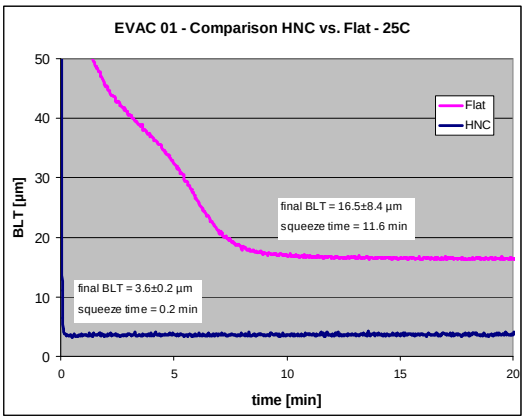
Sample of HNC patterned into Cu by injection molded/sintered

Hierarchically nested channels (HNC):

Over 20 materials have been characterized by IBM with HNC and BLT reductions from 20 to 90 % have been found. The technology was first developed as a “TIM1” (silicon chip to lid) solution, but current work [1] shows greater benefit on larger interfaces like power electronics modules. Particularly interesting for Nanopack is the combination of HNC with an Electrovac TIM material

[1] B. Smith, W. Glatz, and B. Michel, ”Mini- and microchannels in thermal interfaces: spatial, temporal, material, and practical significance,” 2009, Electronics Cooling, Vol. 15 (1), Feb.2009 .

containing carbon nano-fibers to augment heat conduction. The figure on the right shows that HNC has significant effect on the final BLT and squeeze time for low-viscosity screen-printable non-adhesive formulation tested. Final BLT for the tested paste is reduced by 78% and reached 98% faster than the non-HNC case. HNC may be integrated at different packaging levels and for different interface sizes. The simplicity of the HNC designs allows applying different patterning methods to a broad range of materials.

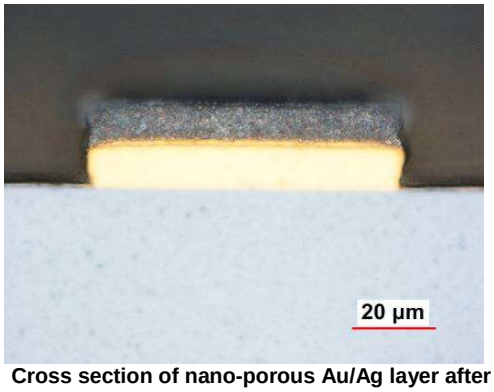


HNC effect on large area interface filled with paste engineered by Nanopack project partner Electrovac

Sinter Ag-Interconnect:

This method is based on the fact that pure silver metal has a very high thermal conductivity and can be deformed easily due to the good ductility. Applied as powder layer it compensates for planarity issues. The small particle size enhances surface diffusion and results in time and temperature decrease during sintered bonding. An Ag-sintering layer can be applied either by dispensing or by stencil printing of an Ag suspension and is therefore applicable using standard equipment. The main focus of the sintering activities at the moment is the optimization of the deposition of the Ag suspension as well as the bonding process to ensure a reproducible quality. Samples are then characterized by thermal measurements and destructive shear testing with analysis of the surfaces.

Au-nano-sponge surface enhancement:

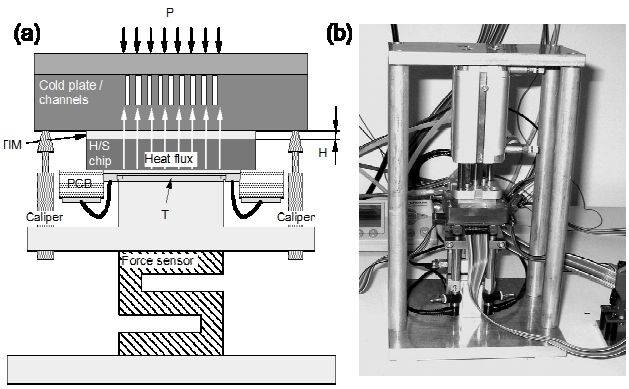


Cross section of nano-porous Au/Ag layer after 10 min etching time

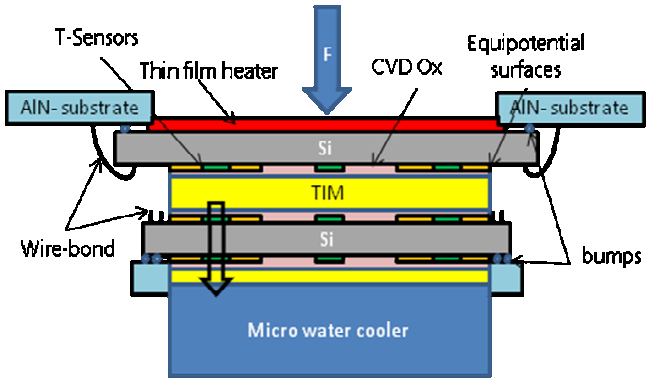
Nano-porous structures deposited by electroplating combine the advantage of a wafer level process with the benefit of a large contact area. The idea behind the nano-sponge is to decrease the interface resistance by the accommodation of porous structure to different particle diameters and profiles, increase the effective contact area of TIM particles with the substrate surface and absorbing of excessive TIM binder materials. The gold nano-sponge is produced by electroplating an Ag-Au alloy followed by etching the Ag, which leaves a nonporous Au of up to 80% empty space. It was found that an Ag content of minimum 65 % is necessary to form an optimized stable nano-porous Au structure after etching.

Progress in test systems set up

The Nanopack consortium has built up a comprehensive measurement capability for testing of packed particle based TIMs.



Schematics (a) and photograph (b) of setup for mechanical and thermal TIM - BLT measurements at IBM. This setup mimics a processor, thermal interface, heat sink geometry as close as possible.



schematic cross-section of Sissy-tester

All specific needs of Nanopack with respect to packed particle based TIMs can be satisfied with the setups built. Thermal and electrical characterization of different interface materials (electrically conductive adhesives, pastes, phase change materials) for various applications can be performed under specific conditions, i.e. appropriate assembly pressure and temperature for specific interface shape and size. With the presented setups the consortium could successfully overcome the lack of adequate commercial tools for TIM measurements and gain in depth experience for thermal and electrical measurements. The setups allow monitoring the progress of Nanopack's material development activity (WP 2). Additionally most of the setups allow incorporation of at least one of the surface modification techniques developed in WP 3.

- A thermal tester for thermal pastes and greases is designed to closely mimic a processor, thermal interface, and heat-sink geometry. The tester is build according to the ASTM standard D5470-06 (achieved accuracy ±1 Kmm²/W) and also measures thermal interface material's thickness (with ±2µm accuracy).
- The field of power electronics is a potential application for Nanopack's enhanced thermal interfaces. Current commercial solid state power-switches exhibit power densities similar to those in computer chips, but are usually packaged in modules significantly larger in size. In order to investigate the formation of the bond line for large area thermal interfaces, a dedicated test setup was developed at IBM to measure 200x140 mm² areas.
- A specific apparatus has been set up to measure the electrical conductivity of electrically conductive adhesives (resistance >50µΩ with 5µΩ resolution)
- The Sissy-tester, whose name is derived from "Si-Si" as two silicon dies face each other in a steady state measuring configuration, is to measure the temperatures on TIM interfaces in 5 positions for localised temperature measurement to capture gradients, parasitics and tilt.
- The TIMA tester offers the capability to test interfaces with modified surface techniques such as nano-sponge and HNC and to measure in-situ BLT and pressures.

Progress in Modelling and Simulations

Effective thermal conductivity of bimodal and trimodal thermally conductive adhesives have been simulated, and results were compared with experimental results.

The filler alignment, like silver flakes in the matrix, affects the thermal and electrical conductivity. The best thermal and electrical conductivity was obtained in the in-plane direction with high flake content. The effective conductivity in vertical direction is much lower than the conductivity in plane direction even with high silver flakes content. The results show that 33 v% of silver flakes and 7 v% silver spherical micro particles provide the best thermal and electrical conductivity in bimodal case.

The thermal conductivity and electrical conductivity is improved by adding the nano-scale filler particles to form trimodal TCA through creating more conductive paths. Experimental and simulation results show that the optimized ratio of the different filler content in trimodal TCA for TIM applications is 0.5v% of MWCNT nano particles regarding the electrical conductivity.

NANOPACK Workshops

On 26th February 2009, Chalmers organized a very successful workshop in Gothenburg on "Thermal transport in electronics and MEMS".

This event, co-sponsored by the Swedish Foundation for Strategic Research (SSF) ProViking program, Swedish National Science Foundation, IEEE CPMT Nordic chapter and NANOPACK, gathered academic and industrial experts of thermal management issues in electronics and allowed to present the project and to establish contacts with external partners. Besides the lectures of NANOPACK partners, the consortium was very please to welcome and listen to expert speakers such as Prof Gerald Mahan (Penn State University), Prof Per Larsson-Edefors and Prof Per Hyldgaard (Chalmers University), Per Ingelhag (Ericsson), and Mattias Gustavsson (Hotdisc AB) and to exchange on various hot topics from nanoscale heat transport to the user's view of integration issues.

A similar event organized by IBM will be held on 1st July at IBM Research Lab in Zurich. It will gather invited talks on various topics from multiscale modelling to an overview of recent packaging developments.

NANOPACK Publications

In the last months, several NANOPACK partners such as Chalmers, IBM and IEMN have published results related to the project in international refereed journals and magazines:

- J. Liu, T. Wang and E.. Campbell, *Thermal management technologies for electronics based on multiwalled carbon nanotube bundles*, IEEE Nanotechnology Magazine, Vol 3 No 1, March 2009.
- B. Smith, W. Glatz, and B. Michel, *Mini- and Microchannels in Thermal Interfaces: Spatial, Temporal, Material, and Practical Significance,* Electronics Cooling Magazine, Feb. 2009, Art. 2.
- Y. Pennec, B. Djafari Rouhani, H. Larabi, J. Vasseur and A.C. Hladky-Hennion, *Low frequency gaps in a phononic crystal constituted of cylindrical dots deposited on a thin homogeneous plate*, Phys. Rev. B, 78, 104105, 2008.

NANOPACK has also been remarked by active participations to famous international conferences such as the MRS Spring Meeting 2009 (ICN), ICEP 2009 (Chalmers), SEMI-THERM 2009 (IBM) and EPTC 2008 (MicReD):

- P.-0. Chapuis, M. Schmidt, J. Cuffe, M. Prunnila, J. Ahopelto and C. M. Sotomayor Torres, *3ω measurement of thermal conductivities of Thermal Interface Materials in the range 10-300 K*, Materials Research Society (MRS) Spring Meeting, San Francisco, April 13-17, 2009.
- Yan Zhang, Cong Yue, Johan Liu, Zhaonian Cheng and Jing-yu Fan, *Study of the Filler Effect on the Effective Thermal Conductivity of Thermal Conductive Adhesive*, International Conference on Electronics Packaging (ICEP 2009), Paper 16B1-1-3, Kyoto, 14-16 April 2009.
- M. Inoue and J. Liu, *Thermal conductivity of Electrically Conductive Adhesives Containing Fillers with Multi-modal Particle Size Distributions*, International Conference on Electronics Packaging (ICEP 2009), Paper 16B1-1-4, Kyoto, 14-16 April 2009.
- B. Smith, A. Bonetti, T. Gnos, and B. Michel, *Flow-induced Spatial Non-uniformity and Anisotropy in Electrically Conductive Adhesives*, SEMI-THERM 2009, March 17-20, San Jose, California.
- András Poppe, Andras Vass-Varnai, Gábor Farkas, Marta Rencz, *Package characterization: simulations or measurements?*, Proceedings of the 10th Electronics Packaging Technology Conference (EPTC'08). Singapore, Singapore, 2008.12.10-12.

Don't miss the special NANOPACK session, to be held during the 15th International Workshop on Thermal Investigations of ICs and Systems, THERMINIC, in Leuven, Belgium, on 9th October 2009. Nine scientific papers related to NANOPACK subjects will be presented and discussed by project partners and external speakers.

Remember to visit us at:
http://www.nanopack.org/

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