Nano Packaging Technology for Interconnect and Heat Dissipation

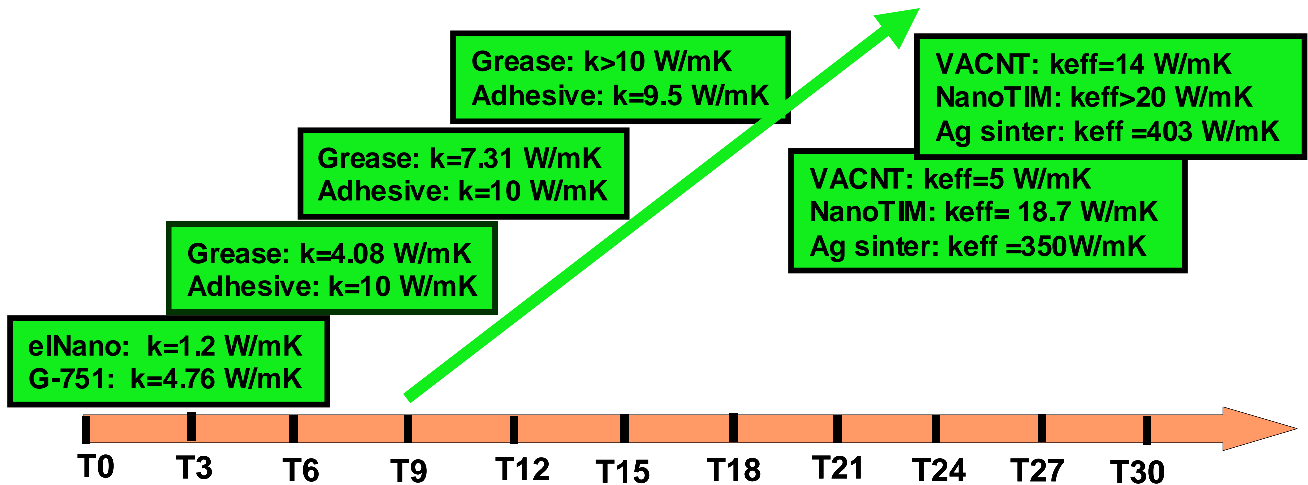
June 2011 Newsletter #5 & 6

NANOPACK is a European large-scale integrating project aiming at the development of new technologies and materials for low thermal resistance interfaces and electrical interconnects, by exploring the capabilities offered by nanotechnologies (such as carbon nanotubes, nanoparticles and nano-structured surfaces) and by using different mechanisms to enhance interparticle contact formation, compatible with high volume manufacturing technologies. Several key research areas relative to thermal management interconnects and packaging are addressed by European industrial and academic partners: thermal interface materials, assembly, reliability, and characterisation; supported by world class modelling and simulations. The benefits of the technologies will be evaluated in different applications to demonstrate improved performance of microprocessors, automotive and aerospace high-power electronics and radio-frequency switches.
The phase of development of materials and process have ended and the project now focuses on the fine characterization of these technologies (performance and reliability) and on their implementation in relevant industrial demonstrators. Thus, we summarize below the main materials and processes developed and describe the demonstrators that are now under construction.

Progress in Material and Porcess Developments

The materials and process developed in the project are:
- **High performance Electrically Conductive Adhesives** (ECA) using bimodal fillers in a bi-epoxy matrix with flexibilizers. Mains characteristics are: k=10W/mK, Tg>180°C, visc<60 Pa.s, Res=6.10-5Ωcm. These materials are being transferred to a Swedish spin-off from Chalmers University: Smart High Tech SHT AB for commercialization.
- **High k greases for high BLTs** have been produced with thermal conductivities in the range of 10 W/mK, using bi- and tri-modal materials (CNT, micro Ag/graphite, silicone) for high BLT > 75µm.
- **Hierarchical Nested Channel (HNC)** allow to reduce BLT and squeeze time during assembly. It has been tested on 20 materials: from 20 to 90 % improvements have been observed on 1-250cm2 interfaces. As example, with the EVAC low-viscosity screen-printable non-adhesive formulation, the final BLT was reduced by 78% and reached 98% faster than the non-HNC case.
- **Ag-Sinter & Au-Nanosponge** : these technologies take thermal benefit from the high k of Ag and Au and mechanical benefit from the porosity of the structure (accommodation of the empty space under constraint). The Au-nanosponge is produced by etching Ag from electroplated Au-Ag alloy to obtain open-porous nano-scale (15 nm) structures. The Ag-sintering technique is a monometal Ag powder bonded at low T° and low pressure for a high resulting conductivity: k= 403W/mK.
- **Thermal interfaces based on Vertically Aligned CNTs** infiltrated by paraffin have a thermal resistance of Rth=7.3 Kmm²/W for a BLT=100µm, resulting in an effective thermal conductivity of keff=13.7 W/mK
- **Metal-polymer nano-composite** made of Polymer (Polyimide) fiber network infiltrated with PCM metal alloy show extremely high thermal performance: 18.7 W/mK of effective conductivity with InSnBi alloy (Eutectic 60°C) and more than 24 W/mK with pure In (Eutectic 160°C). This technology has demonstrated its efficiency by comparison with commercial material (TC5022) used to assemble HP LEDs (24W): Rth decrease by 65%. It is now being transferred for volume manufacturing.

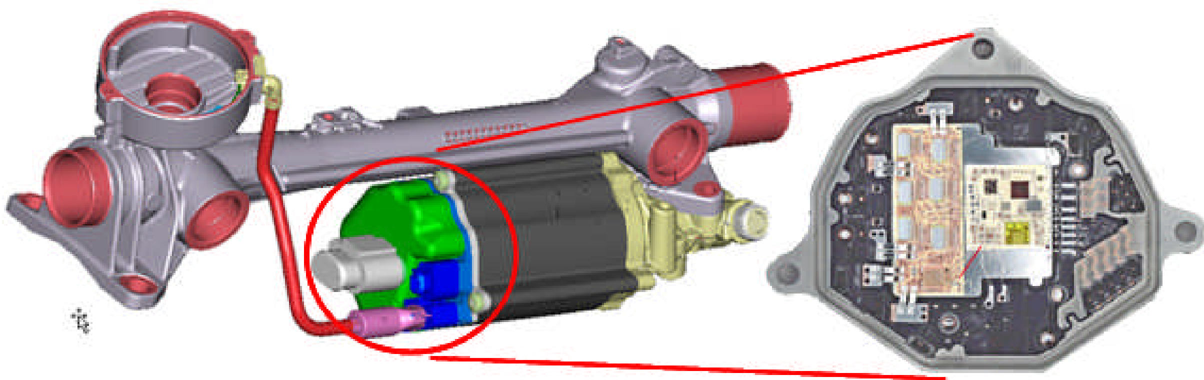
All these materials are now under intensive testing for reliability evaluation.



NANOPACK Demonstrators

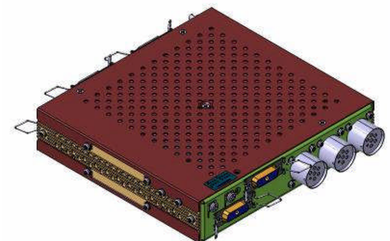
Automotive Applications (Bosch)

Bosch will work on the power amplifier module from a commercial electrical power steering unit used in cars (automotive). Main components of this module are power transistors mounted on a direct bonded copper (DBC) ceramic substrate. To limit the heat created in the transistors, the DBC substrate is to be mounted on an Al-base-plate as a heat spreader using TIMs. This heat flow can be optimized by reducing the BLT, increasing the thermal conductivity of the TIM or by reduction of the thermal interface resistance between Al and DBC.



Avionic Applications (Thales)

THAV will work on avionics equipments used in civil avionics for In Flight Entertainment Systems (IFE). This equipment is representative of the main thermal constraints which are encountered in most of our products: this equipment is a Seat Electronic Box (SEB) which is placed just under the passenger seat in small enclosed zones. This SEB has many hot spots and is cooled only by natural air convection. For the thermal management of this equipment we are proposing to use two-phase change systems like heat pipe or loop heat pipe in order to transfer the heat from the component to the SEB wall (with heat pipe) or from the SEB wall to an external heat sink or cold structure (for instance the cold mechanical structure of the seat) with the use of loop heat pipe.



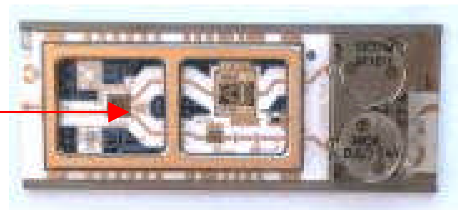
This thermal management induces many thermal interfaces which need to be correctly managed in order to keep an good efficiency for global thermal path.
The demonstrators will integrate many thermal interfaces inside the SEB:

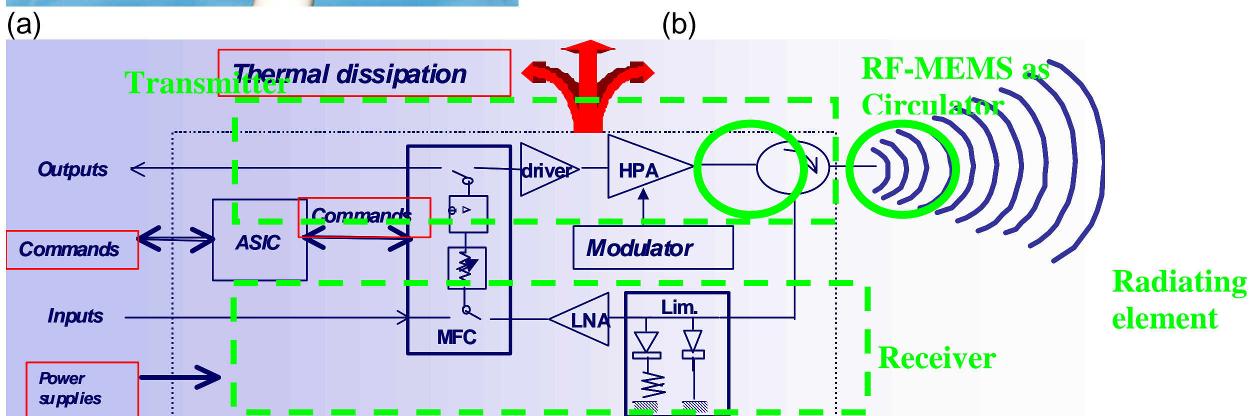
- between components and heat pipe
- between PCB and heat pipe
- between heat pipe and mechanical structure.

For the cooling of the SEB, we will use two cold plates which will simulate the Loop Heat Pipe evaporator. We will make aging tests and thermal cycling tests.

Aerospace Applications (Thales)
Active phased array antennae are key products of THALES who sells them as major equipments in integrated systems for high-end defense, security, surveillance, space or telecom applications. They are compound of multiple (up to several thousands) individual T-R modules, whose role is to Transmit/Receive signals synchronously with phase and amplitude control between them. This antenna architecture allows to steer the beam electrically (i.e. without any mechanical movement), to shape the beam or to generate several beams. Moreover, if one of the T/R modules breaks down, the performance of the whole antenna is not decreased and the maintenance is simplified. In brief, this type of antenna provides a very powerful and agile radar system.

(a)


(b)



(c)

(a) THALES Phased Array Antenna; (b) T/R module (c) Scheme of a T/R module
As depicted in the figure above a typical T/R module is compound of a transmitter path, a receiver path, a circulator to switch from one path to the other one and a radiating element to emit/receive the signal. In the framework of WP 7, TRT will realize two demonstrators related to these applications:

- a high power amplifier (HPA)
- a RF-MEMS switch

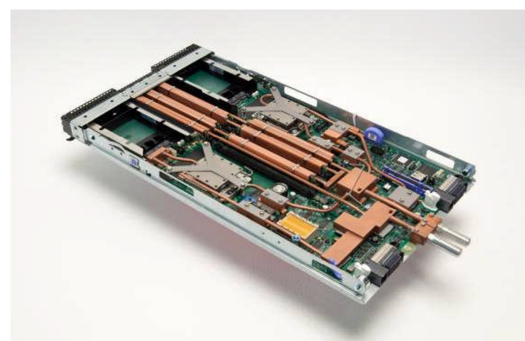
Packaging the HPA or the MEMS requires the use of thick and highly conductive grease and electrically conductive adhesive as die attach. The current T/R modules, based on GaAs technology will use in the future GaN technology and will target an increase of 50% of RF power. The thermal management is thereby a key element in the success of the antenna.

Microprocessor for IT Applications (IBM)

The objective of the present effort is to demonstrate the feasibility of the developed materials and processes to provide low resistance thermal interfaces (<2 Kmm²/W) usable for TIM1 or TIM2 interconnects in microprocessor. The future trend in IT industry will be to replace the traditional air heat sinks with high efficiency liquid coolers. The application of high efficiency micro-channel coolers reduces the overall thermal resistance from the microprocessor junction to the coolant, whereby the impact of a low TIM resistance becomes more prominent. We chose a commercial available HS22 blade for the demonstrator with a high performance Intel Xeon X5560 CPU. The blade will be modified, where we replaced the traditional air heat sink with a liquid cooled micro-channel cooler. We will apply a TIM material developed in the project (see WP2) and, depending on our preliminary studies we will use this paste in combination with an HNC (see WP3) structured cooler surface. We evaluate the performance of the materials developed in WP2 in combination with and without the HNC surface modification with our TIM1 tester described in WP4. A material suitable for the demonstrator should significantly outperform our reference, a commercial available paste (Shin-Etsu X-23-7783D).

IBM Demonstrator	**Properties of Shin-Etsu X-23-7783D used for this family of TIM applications**		**Requirements NanoPack TIM**
TIM2 for Intel Xeon X5560 CPU in experimental liquid-cooled IBM BladeCenter HS22	Grease		Grease
	K	4.5 W/mK	**> 10 W/mK**
	Rth	10 mm^2K/W	**< 5 mm^2K/W**
	Ω	1 x 10^4 MΩm	1 x 10^4 MΩm
	BLT	50 µm @ 1 bar	50 µm @ <1 bar
	Area	CPU cap size	CPU cap size
	Temperature	-50 – 120ºC	-50 – 120ºC
	Cost	1000 USD/kg	1000 USD/kg
	Reliability	Manufacturability qualified	Promising

The figure besides depicts an image of a liquid cooled HS22 blade. The CPUs are cooled by two cooper micro-channel cold plates, which are built into the package lids. The cold plates itself provide a thermal resistance of 10 mm^2K/W. If we apply a standard TIM, the total thermal resistance is more than doubled. Consequently, a dramatic reduction in TIM resistance should demonstrate a strong impact on the overall thermal performance of the cooling solution.

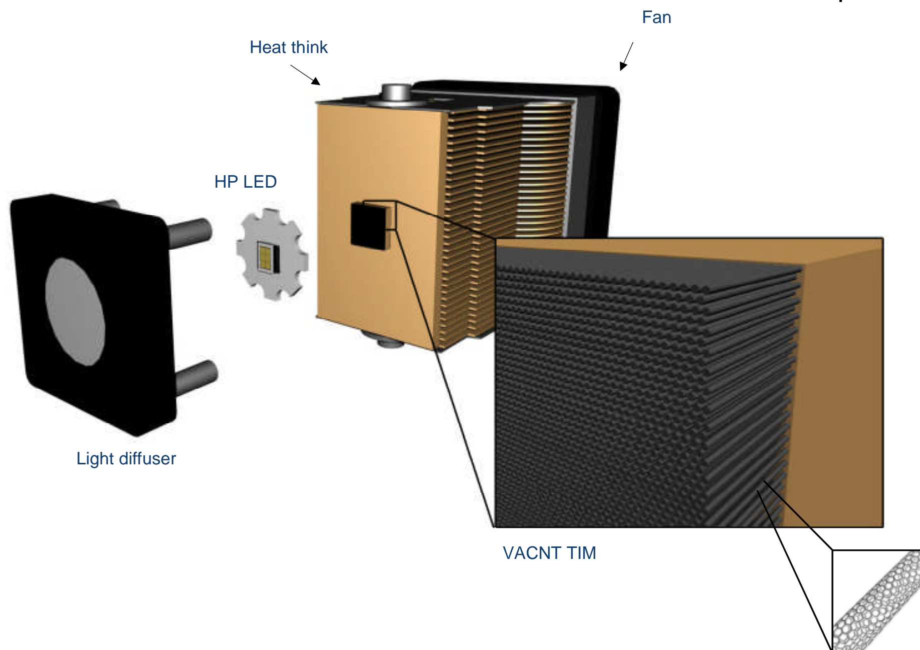


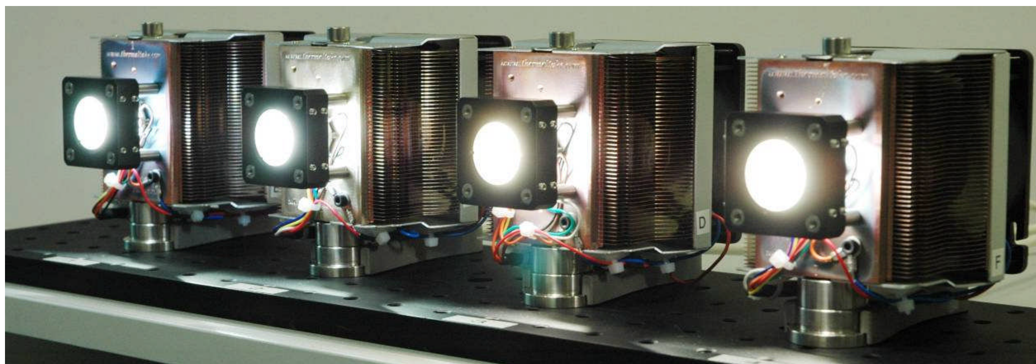
LED Demonstration (Thales)

In order to demonstrate the efficiency of the thermal interface based on the Vertically Aligned Carbon NanoTubes (VACNT) developed by TRT in the framework of WP3, TRT has also built a demonstrator integrating this technology into LED lighting vehicle. 4 High Power LED (OSRAM OSTAR LE3 W modules) emitting 280 lm for a thermal load of 21W have been mounting on a Cu baseplate in 4 different conditions:

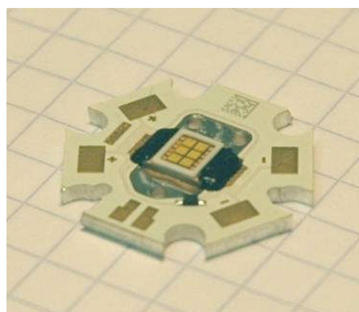
- direct contact Cu-LED
- Use of a commercial thermal grease
- Use of pure VACNT
- VACNT infiltrated with paraffin matrix.

A temperature sensor mounted on the LED substrate allows to monitor its temperature.





Picture of the 4 LED running with different TIM



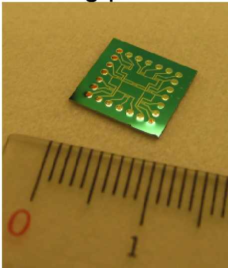
OSRAM LED

Monitoring the T° of the 4 LED

We demonstrate a T° decrease of 3 and 5°C using VACNT based interfaces compared to the 37°C of the LED cooled using commercial grease.

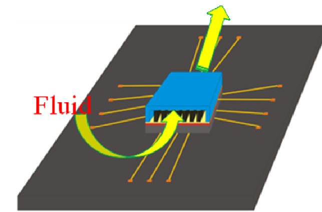
Integrated Microcooling for HP electronics (FOAB)

FOAB will demonstrate a power module cooled by a novel microchannel cooler. In the last period, we have designed and developed a power die which enables real time temperature measurements on the surface. This functional power die has been manufactured and calibrated acting as a working platform for the demonstrator.



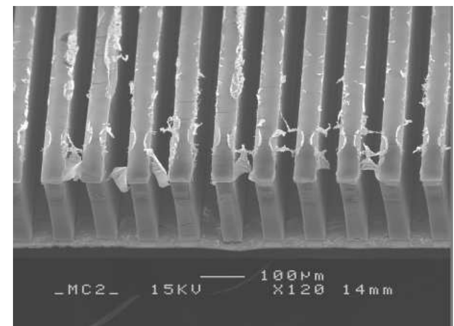
Demonstrator Platform

Side view of the microchannel cooler mounted onto a Si substrate



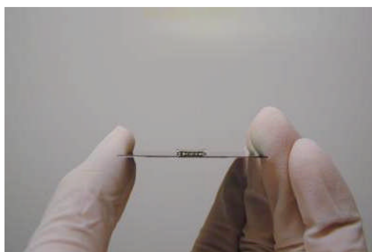
3D schematic of the microchannel cooler indicating fluid flow through the channels fabricated on the chip surface

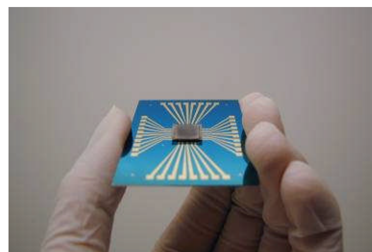
We have designed a microchannel cooler for high efficiency on-chip cooling based on the simulation results from wp6. The structure of the microchannel cooler is illustrated above. The fins used to form microchannels are made of carbon nanotubes (CNTs), which show great potential in thermal management in electronics due to their extremely high thermal conductivity.



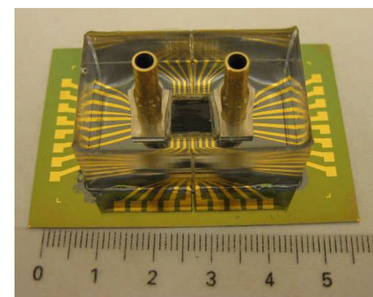
In order to fabricate the microchannel cooler structure, a CNT transfer technique has been developed. As it's well known, two of the most challenging obstacles to overcome for using CNTs in electronics are the weak van der Waals force and the high electrical and thermal resistance between as-grown CNTs and the supporting substrate. In our method, an ultrafast metal enhanced CNT transfer technique is used to address these problems by using the TIM provided by Chalmers group. The CNT fins are fabricated onto the demonstrator platform thus an on-chip microchannel cooler structure is made. The figure beside shows the CNT fins transferred onto the demonstrator platform using thus developed method.

Once the CNT fins have been fabricated onto the test platform, a lid is covered on top of the CNT fins so that the micro channels are formed for fluid flow. Afterwards, the test platform is soldered onto a Si substrate and fluid path is made. The whole structure is finally encapsulated by PDMS as shown in the last figure. Coolant including air and water will be used to evaluate the cooling performance of the on-chip fabricated microchannel cooler.





Side and top view of the test platform soldered onto Si substrate



PDMS encapsulated CNT based microchannel cooler

NANOPACK Workshops

A special NANOPACK session was held during the 16th International Workshop on Thermal Investigations of ICs and Systems, THERMINIC, in Barcelona, Spain, on 8th October 2010. 11 scientific papers related to NANOPACK subjects were presented and discussed by project partners and external speakers. This session was a very good opportunity to discuss and compare the different approaches, and will serve to gain new ideas to achieve the goals of the NANOPACK projects.

During the ICT exhibition 2010, hold in Brussels on 27-29th September 2010, the Nanopack consortium showed on a 9m² stand:

- a 8' movie explaining the stakes of Nanopack
- LED demonstrators (Chalmers and TRT) illustrating the performance of the Nanopack TIM compared to commercial products and the use of Carbon-Nanotube-based interfaces
- A microcooler demonstrator (electronic chip for telecom) (FOAB)
- IBM, THAV and Bosch came with their demonstrators (product where Nanopack technologies are inserted)
- BME+MicRed and IZM+Nanotest+IBM brought the characterisation tools they have elaborated during the project.

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- T. Brunschwiler, G.I. Meyer, S. Paredes, W. Escher, and B. Michel, Direct Waste Heat Utilization From Liquid-Cooled Supercomputers, Proc. 14th Intl. Heat Transfer Confernce, August 8-13, Washington DC, USA, IHTC14-23352, 1-12 (2010) **(Key note Talk and Paper)**.
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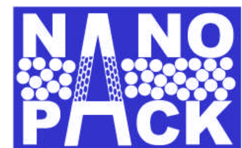

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Further Information at http://www.nanopack.org/