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SEVENTH FRAMEWORK PROGRAMME

Nano Packaging Technology for Interconnect and Heat Dissipation

NANOPACK

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WORK PACKAGE 6: Modelling and simulation

DELIVERABLE D6.7

FE-Model for interface characterization and lifetime prediction of final assembly demonstrators

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ABSTRACT:

This deliverable "FE-Model for interface characterization and lifetime prediction of final assembly demonstrators" is related to Task 6.7 Development of FE-Model for interface strength.

Given that there is wide variety of interconnect systems technologies it was decided by the NANOPACK consortium to exemplarily focus on the development of a lifetime model for interface strength of the low pressure sinter-Ag die attach interconnect technology development at IZM (WP3 and Task 5.5). The strength of this type of interconnect is currently unknown and is therefore the most important issue for lifetime estimation.

Due to unknown material behavior of sinter-Ag a combined experimental/numerical approach for the development of an elastic-plastic material model was applied. Based on nanoindentation data simulation was tuned to fit the experimental indentation measurement. As a result a Ramberg-Osgood type material model was determined.

The thermo-mechanical reliability of chip-on-board (COB) assemblies for power applications are studied by experiment and simulation. Thereby the main focus is set on the characterization methods and low cycle fatigue failure behaviour of the die-attach material under thermal cycling conditions.

1 INTRODUCTION

The thermal interface resistance is one of the major bottlenecks in advanced thermal packaging solutions. Over the last couple of years this trend has become more and more apparent as well as the need for new developments in advanced thermal technology [1-3].

Previous investigations have shown the excellent thermal conductivity (close to bulk silver) and high mechanical strength of sinter silver [4]. These results are very promising for using this material as die attach in high power electronic devices.

On integrating microelectronic systems with this technology it is of great importance to assure the function of these systems and its individual constituents. Thus it is indispensible to analyse their reliability systematically in order to generate lifetime models and design guidelines for lifetime prediction. These models need to reflect the physics-of-failure which has to be reproduced consistently by experiment and simulation. Therefore in this deliverable the analysis of stresses and strains of the die attach is carried out with respect to processing technology and external thermal loads in automotive application. As this work considers a new technology a systematic approach drawing upon both simulation and experimental methods has to be applied.

First modified COB test vehicles were fabricated and the sinter silver was characterized and reported in deliverable 5.4. Hence materials may behave differently in their mechanical properties if fabricated in smaller dimensions, this characterization is a challenge. Mostly no standard methods can be applied due to the impossibility to fabricate standard test specimens. Therefore, methods like nanoindentation in conjunction with FE simulations are applied to determine elasto-plastic material behaviour. This is necessary as the desired material parameters (like Young's modulus and yield stress) cannot be obtained directly but have to be extracted from the simulation.

Then, an FE-model of the COB is generated and material data is implemented. Simulation runs allow locating and monitoring accumulated plastic strain over the process steps and through several thermal cycles. These response parameters can be used to generate a lifetime model for this kind of die attach (e.g. by a Coffin-Manson or Paris-Erdogan approach) when compared to experimental lifetime data.

2   SPECIMEN FABRICATION

2.1   SINTERING ON DCB (DIRECT COPPER BONDING) SUBSTRATE

First sintering test modules were assembled using Si chips and DCB substrates both with Ag metallization (see Figure 1). To ensure a uniform Ag-sintering bond interface, the Ag suspension was stencil-printed with oversized geometry. Two chip sizes 6x6 mm² and 9x9 mm² were bonded and two initial Ag sintering layers, 75 µm as well as 150 µm, were used. The samples were then tested by thermal cycling between 0℃ and 85℃ and -55℃ and +125℃.

**Figure 1: Left: Light microscopy image, top view of the chip sintered on DCB;
Right: Cross section of a Ag-sintered Si chip on DCB**

The modules were analysed by CSAM inspection. After 500 cycles most of the samples tested between -55 and 125℃ failed due to crack formation inside the DCB substrates. This failure mode can be seen clearly as light grey area during CSAM inspection as shown in Figure 2, where the side view of a failed test sample after 500 cycles is displayed.

During thermal cycling, failures within the Ag sintering layer were not detected by CSAM inspection. Instead damages of the die attach the ceramic substrate is broken. Therefore, it was decided to stop the thermal cycling test (TCT) with these test modules and to assemble new ones with different substrate material. Instead of DCB pure Cu was selected. An electroplated Ag metallization was first deposited on the Cu. Again two chip sizes (6x6 mm² and 9x9 mm²) and two thicknesses of the printed Ag suspension (75 µm and 150 µm) were selected. A total number of 56 test modules was assembled and tested by TCT (0/+85℃ and -55/+125℃) and analysed by CSAM inspection.

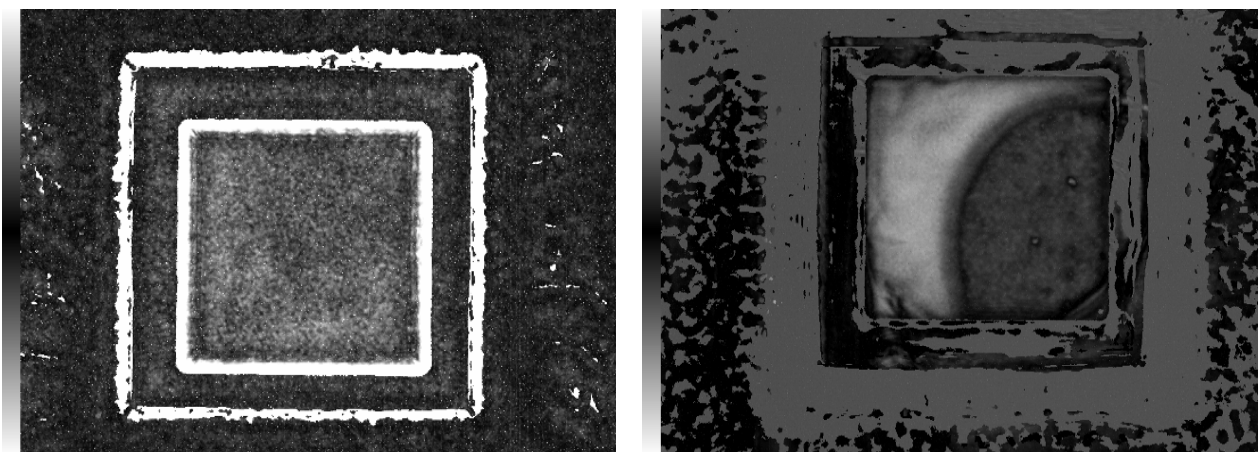**Figure 2: Left: CSAM image of a module (6x6 mm², 150 µm, 150 cycles 0/85℃);
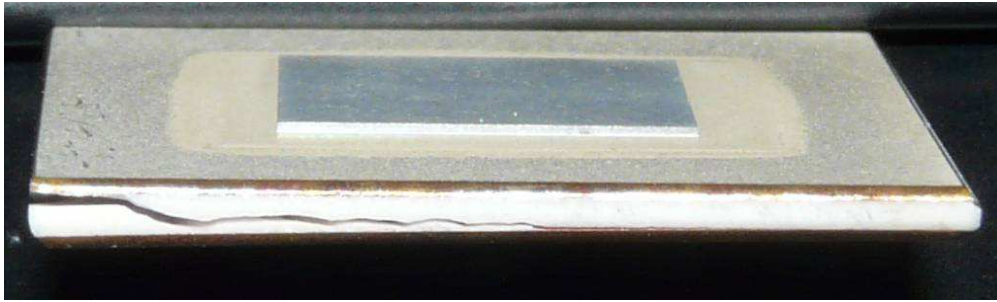Right: CSAM image of a module (6x6 mm², 150 µm, 500 cycles -55/125℃)**

Figure 3: Light microscopy image of a broken DCB substrate after 500 cycles between -55°C and +125°C (9x9 mm², 75 µm)

2.2 SINTERING ON PURE COPPER SUBSTRATE

For the second sintering test modules we used 1.5 mm thick plates of oxygen-free copper and plated a 3 µm thick silver layer onto the upper side. The Ag paste layer was applied by stencil printing of an Ag suspension by using a standard printing machine. Two different stencil thicknesses of 75 and 150 µm were used to achieve different bond thicknesses. After bonding the layer thickness of the die attache amounts to approximately 22 µm and 38 µm, respectively.

IGBT chips of 130 µm thickness with Ti/Ni/Ag metallization were placed into the printed silver paste after a short drying period. The backside was covered with a polymer sheet then force and temperature was applied to perform the sintering. A sintering temperature of 230°C and a bond pressure of 40 MPa were selected. The assemblies are depicted in Figure 4.
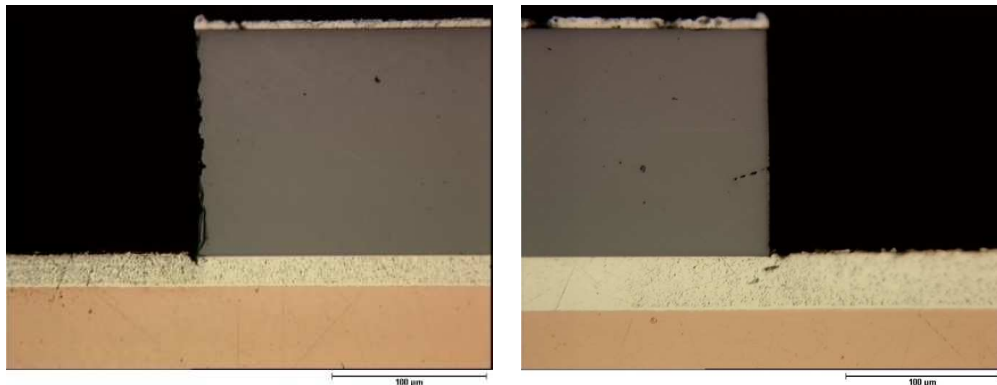

Figure 4: Cross section of the sintered IGBTs on copper substrate. Stencil thickness of 75µm (left) and 150µm (right) represents 22µm and 38µm in bonded state

For reliability investigations different geometries are needed. Specimens with die attach thicknesses of 22µm and 38µm as well as chip sizes of 6x6mm² and 9x9mm² were fabricated.

3 MATERIAL CHARACTERIZATION

3.1 NANOINDENTATION MEASUREMENT ON SINTER-AG

First, the material properties of the sinter silver layers need to be characterised. Therefore, the fabricated chip assemblies with a die attach thickness of 22µm and 38µm were cross-sectioned and polished.

The fabrication of specimens of that thickness for tensile testing is not feasible. Therefore we have opted for material characterisation by a combination of a nano-indentation experiment and a simulation of the indentation process. The measurements were carried out normal to the cross-sections of the die attach.

For the determination of correct values, the nano-indenter undergoes first a calibration process [5]. For that purpose indents in a material of known elastic modulus are made (fused silica). In the first step this calibration is applied to level out the load frame compliance using large area indents. After correction for the load frame compliance, the relation of contact stiffness and indent area vs. indentation depth h_c can be represented by equation 1.

$$A(h_c) = \frac{\pi}{4E_r^2}(S(h_c))^2 \qquad (1)$$

Here, E_r denotes the known Young´s modulus of the calibration sample and S the contact stiffness recorded as tangent on the force displacement curve upon unloading, therefore containing information about the elastic response of the layer. An underlying assumption for this formula is, that a Berkovich or Vickers indenter can be approximated by an indenter shape of rotational symmetry, leaving an indent-area equivalent to $A = \pi r^2$. The area versus indentation depth curve can be fitted by a polynomial expression (equation 2).

$$A(h_c) = C_0 h_c^2 + C_1 h_c + C_2 h_c^{1/2} + C_3 h_c^{1/4} + C_4 h_c^{1/8} + C_5 h_c^{1/16} \qquad (2)$$

Using equation 2, we can plot $h_c(r)$ and thus retrieve the actual indenter tip shape function, which is then, mapped onto the FE-model depicted in Figure 9 (simulative part of approach will be discussed below).
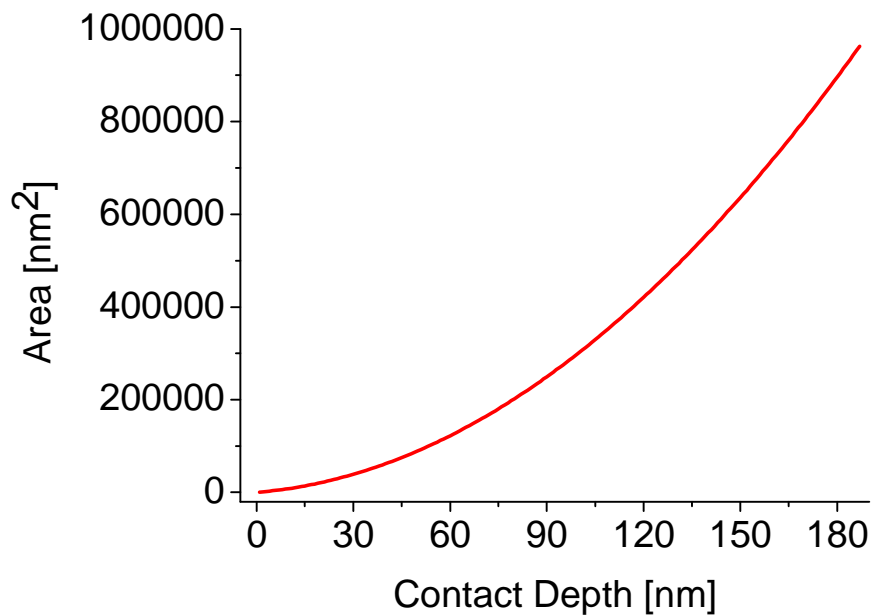
Figure 5: Calibration curve for Berkovich diamond-tip nanoindenter on fused silica

After the calibration process, the nanoindentation measurements were carried out on the die attach with a layer thickness of 22µm and 38µm. The results produced by indentation with constant maximum force of 2mN are depicted below in Figure 6, using equation 1 for the elastic modulus E_r and in Figure 7 using equation 3 for the hardness H.

$$H = \frac{P}{A(h_c)}$$

(3)

Here, P is the indentation force.

$$E_{r22} = 64{,}4 GPa \pm 3{,}2\ GPa$$
$$E_{r38} = 64{,}0 GPa \pm 4{,}0\ GPa$$

● Die Attach thicknes 22µm
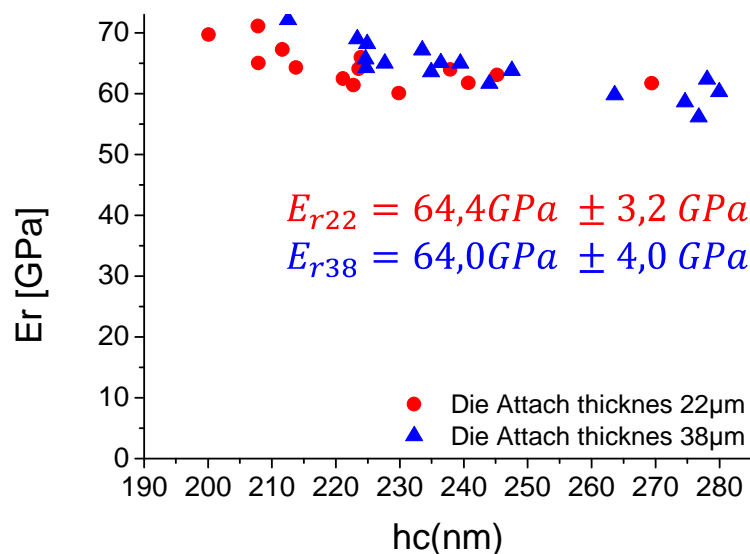▲ Die Attach thicknes 38µm

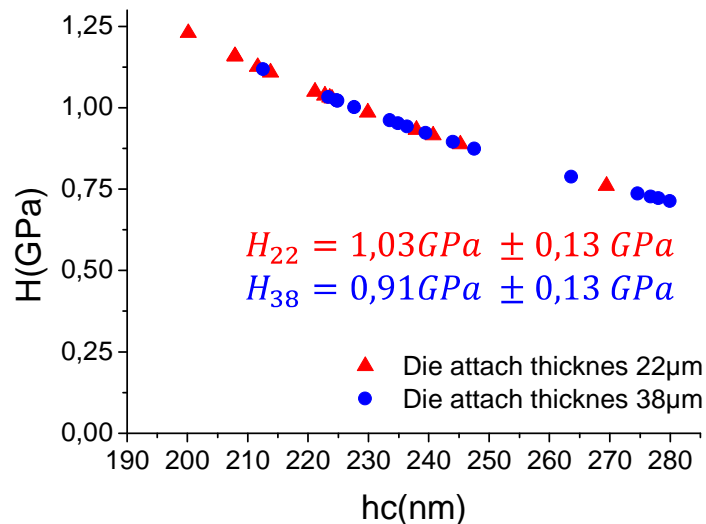**Figure 6: Reduced E-modulus calculated by indentation software**

Figure 7: Hardness calculated from standard equation 3

Owing to the fact that we want to get pure bulk behaviour from the indentation measurements the indents have to be as small as possible but big enough to avoid surface and interface effects. Experience has shown that indentation depths in the range of 250nm done with a Berkovich indenter are sufficient for this kind of situation.

Due to scatter of the measurements a pattern of 20 indents is used to get a trustable mean value of the Young´s modulus. Figure 8 shows the positions of the indentations and the corresponding modulus map of the 38µm die attach. The modulus map was manually overlaid on the topology scan made by the indenter after the indentation procedure. On the bottom left corner of the pattern two indents with small values in the range of 15 GPa can be pinpointed. This effect is probably caused by a cavity under the surface of indentation. These points are neglected for the following characterization procedure.
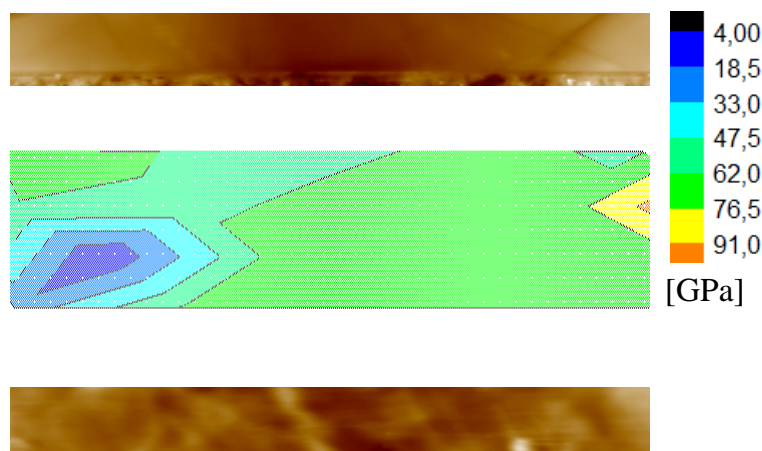

Figure 8: Surface topography and modulus map of the 38µm die attach indentation region

However, the main target of the indentation tests is a statement about onset and evolution of plasticity, which cannot be obtained from modulus or hardness values. As already mentioned before a combined experimental-numerical approach was applied to extract the desired material properties.

3.2 EXTRACTION OF RAMBERG OSGOOD COEFFICIENTS BY FE-SIMULATION

We have generated a FE model of rotational symmetry (Figure 9) to mimic the nanoindentation process. Rotational symmetry seems appropriate, as the whole calibration process hinges upon that assumption. From equation 2 the indenter tip shape function $h_c(r)$ was plotted and transferred on to the model geometry.
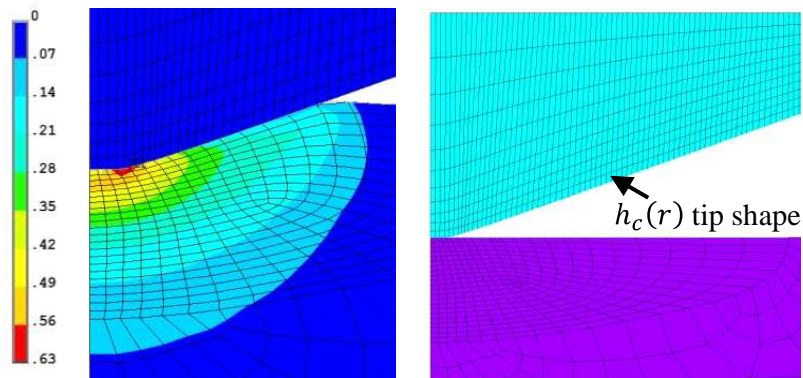

Figure 9: FE-Model for nanoindentation, rotational symmetry, and resulting plastic strain (Sinter Ag at 2mN). One notices the complex strain distribution below the tip

As constitutive equation for metal plasticity representation a four-parameter Ramberg-Osgood model [6,7] was implemented in terms of a multilinear elastoplastic material law with kinematic hardening (see Figure 10).

$$\varepsilon = \frac{\sigma}{E} + \alpha \frac{\sigma_{0.2}}{E} \left(\frac{\sigma}{\sigma_{0.2}} \right)^n$$

(4)

Here, E is the Young´s modulus; $\sigma_{0.2}$ is the stress at 0.2% plastic strain and α as well as n are constants.
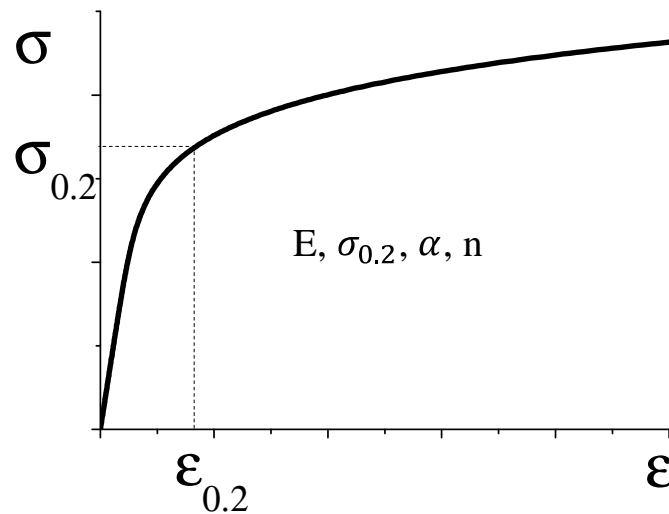
Figure 10: Scheme of the Ramberg-Osgood approximation to describe elasto-plastic behaviour

Now simulations were run parametrically with respect to these four parameters until an optimum fit to the indentation depth versus force curve was found. The optimization procedure started with fitting the E-modulus first, a quantity which governs the unloading behaviour. Then yield stress and the coefficients *α* and *n* were fit. As reference data for fitting all valid measured force-depth curves were averaged. The results of this fitting procedure are displayed in Figure 11 and Table 1.

Table 1: Ramberg-Osgood coefficients received from fit

Material	E-Modulus [GPa]	σ_0 [MPa]	α	n
SinterAg	64.0	181.0	0.752	4.16

A very good fit is obtained for the unloading curve, whereas the loading part has still room for improvement. This is believed to be due to the porosity of the Ag-sinter material which is not considered in the FE-model. However for the lifetime model a sufficiently good material model could be generated by the presented procedure.
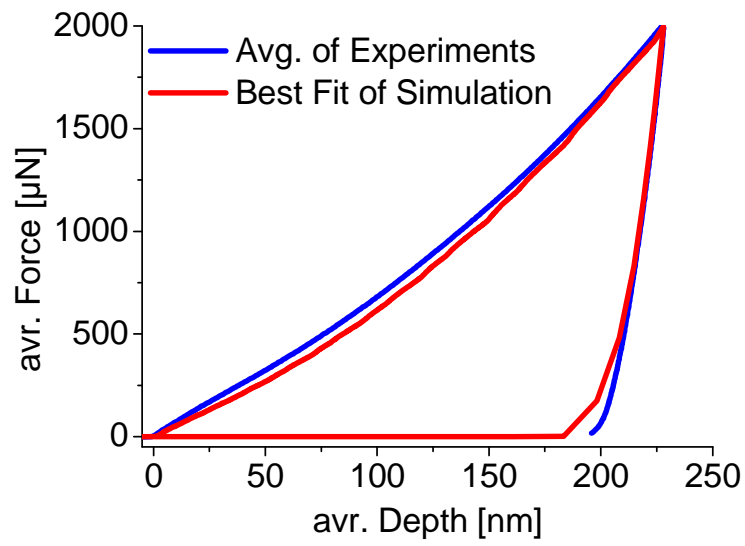
Figure 11: Correlation of experiment and simulation for nano-indentation in sinter Ag.

4 THERMAL CYCLING TEST IN SIMULATION AND EXPERIMENT

4.1 EXPERIMENTAL PART

In parallel to the simulation, test specimens as described in section 2 underwent thermal cycling according to Figure 12. Unfortunately only one set (9x9mm² die with die attach thickness of 22µm) of experiments seems to produce good results. The reason for this behaviour might be some problems in the fabrication process, which cannot be 100%ly solved throughout the remaining time of the project.
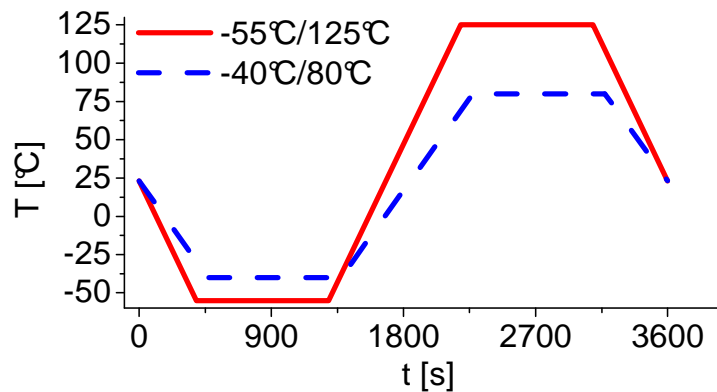

Figure 12: Simplified thermal cycle during TC testing.

To check the samples for delamination, scanning acoustic microscopy (SAM, Figure 13) and metallographic sectioning (Figure 14) was carried out. Altogether 20 specimens of the good set went under thermal cycling. Exemplarily Figure 13 shows the propagation of the delamination after 1000, 2000 and 3000 temperature cycles (TC) in the range of -55℃ and 125℃.
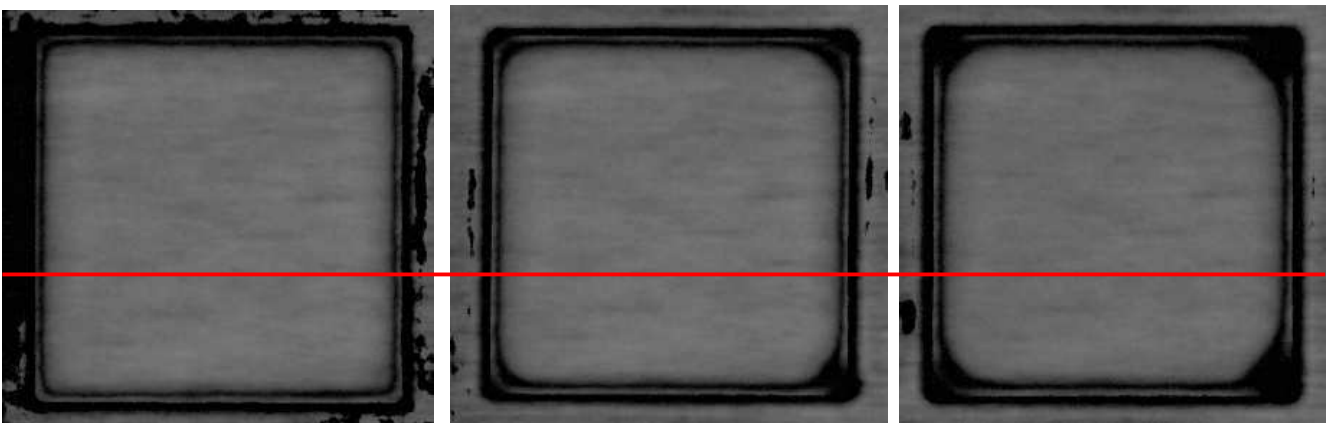

Figure 13: SAM scans of sinter Ag die attach after 1000 TC (left), 2000 TC (center) und after 3000TC (right). The red line represents roughly the position of cross sectioning.

SAM is only a good method to determine delamination and crack length if the crack is far enough from the chip edge. In this case there is very slow crack propagation so that metallographic sections of the specimens need to be carried out. The planed testing will on-going for at least another 2000 TC which will be reached at the end of the project.

The propagation of die attach damage is depicted in Figure 14. On the REM record of the cross section on top we can see the state of the die attach after 1000 TCs. The crack length in this region is about 90µm from the edge of the chip. The microscopic picture below shows the crack length after 2000 TCs. The crack length here is about 168µm. At the moment no cross section of the die attach state after 3000TC is available. Specimens coming from the same set cycled in the range of -40℃ to 80℃ don't show any damage after 2000 TCs. Here als o no cross section of the die attach state after 3000TC are available yet.
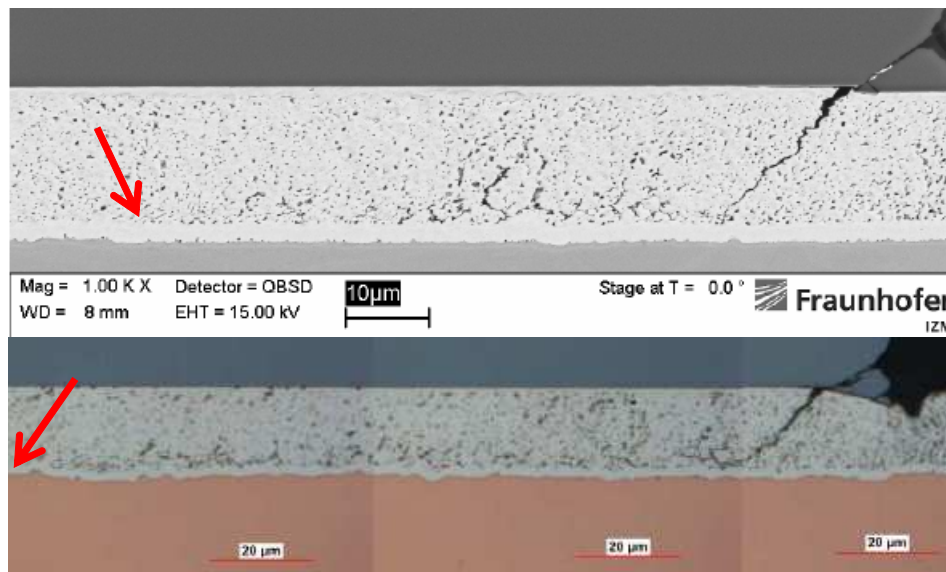
Figure 14: Crack propagation in die attach after 1000 TC (top) and after 2000 TC (bottom) @ -55℃/125°C. The red arrow pinpoints the tip of the crack.

4.2   SIMULATIVE PART

Now we have an experimental indication how damage progress under the investigated conditions develops. In the next step the damage process will be physically modeled by transferring the experiments to an FE-Model. Therefore a full parametric model of the COB was build (Figure 15).

Figure 15: Expanded 1/4 FE-Model of the 9x9mm² IGBT on a 20x20mm² Cu substrate
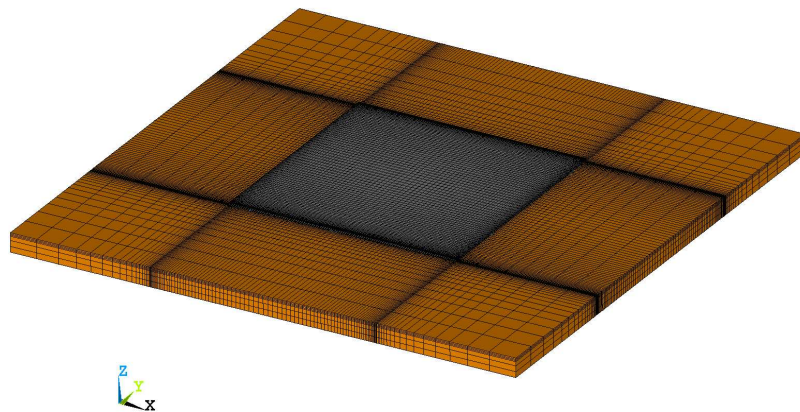
Material data shown in Table 2 were implemented and the original test matrix described in section 2 was performed.

Table 2: Material data used in simulation

Material	E [GPa]	σ_0 / T [MPa]	ν	CTE [ppm]	α / n
SinterAg (Fit)	64.0	181.0	0.3	19.0	0.75 / 4.16
Silicon	168	-	0.28	2.6	-
Copper	110	180 / 6500	0.34	16.5	-

The question is where in the model and how to evaluate the plastic strain. One possible approach could be to do the damage evaluation in the same way as is usually done for solder balls from, e.g. flip-chip assemblies [8]. This procedure averages the creep strain rate over the region where damage occurs to avoid singularities and numerical effects on interfaces [9, 10]. The idea now is to do the same averaging of the plastic strain rate for the sintered silver as it was performed in similar cases for another solder die attach [11].

As for solder material the accumulating creep strain is describing the failure behavior for sintered silver it is the accumulated plastic strain. As can be seen from the FE-simulation in Figure 16, there is an area of high plastic strain rate running along the perimeter of the silver layer, indicating the region of beginning damage.
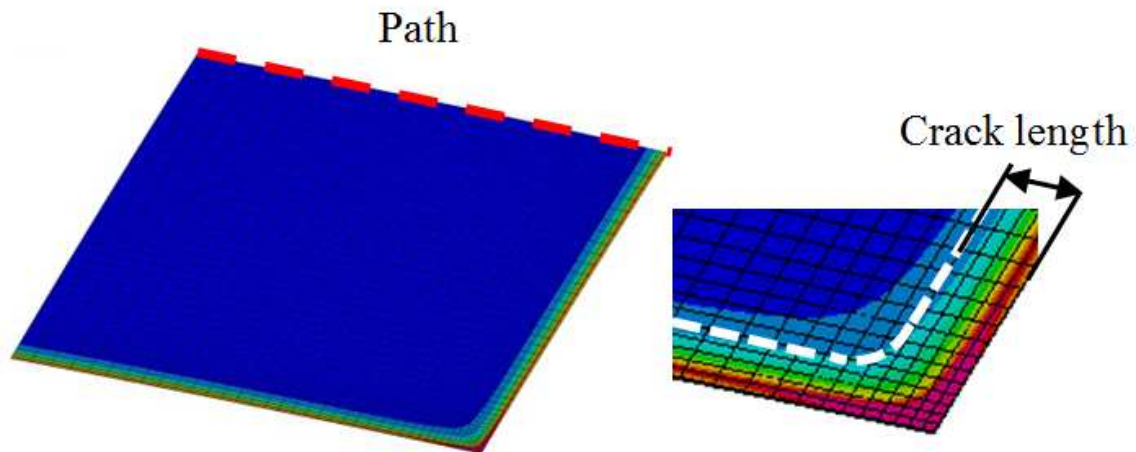
Figure 16: Failure criterion is the accumulated equivalent plastic strain rate per temperature cycle. The data path for analysis is the red dotted line. White line shows the crack front.

For the evaluation the plastic strain rate is mapped on to the path reaching from the edge to the center of the die attach. It is located in the die attach 4µm above the copper substrate. Equation 5 is used to do the averaging of the path data [11].

$$\varepsilon_{pl}^{avg} = \frac{1}{\alpha} \int_0^\alpha \varepsilon_{pl}(s) ds \qquad (5)$$

4.3 RESULTS BY COMPARING OF EXPERIMENT AND SIMULATION

Because of the mechanical effect of massive delamination on the chip assembly this approach can only be valid for cracks much shorter than the chip size. Assuming a value of 10% area delamination as failure criterion should be provide cracks short enough to fulfil these demand [11]. The assumed critical crack length corresponding to 10% area delamination is app. 230µm for the 9x9mm² chip sizes and app. 150µm for the 6x6mm² chip sizes, respectively. This lies within the result we get from the experiments. Here for the 9x9mm² chip size and a die attach thickness of 22µm the crack length is about 168µm after 2000 TCs.
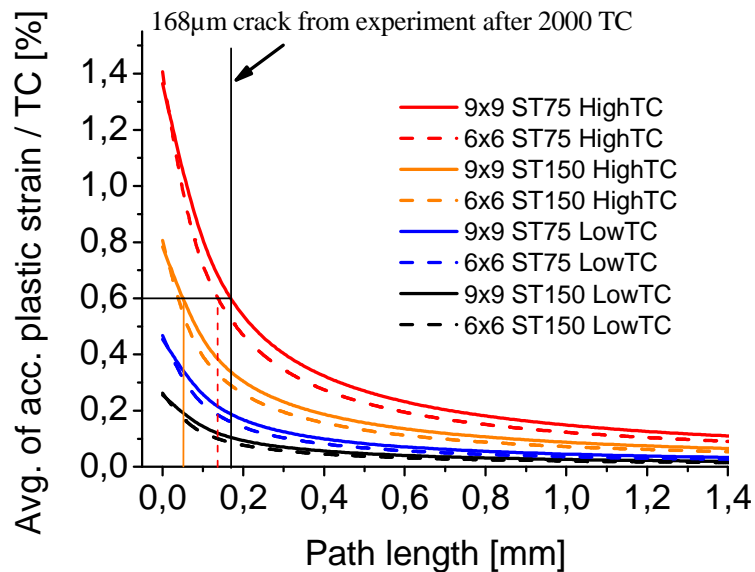
Figure 17: Averaged accumulated plastic strains per TC plotted over the path length. The failure criterion is the crack length of 168µm from experiment.

Comparing the results from simulation depicted in Figure 17 as expected the amount of the plastic strain rate strongly depends on the temperature profile. Specimens loaded with the high TC (-55℃ to 125℃) show much more damage potential than the ones loaded with the low TC (-40℃ to 80℃). Furthermore plastic strain rate drops with rising stencil thickness. The influence of the chip size seems to be relatively small.

Referring to the experimental result where the crack length reaches 168µm after 2000 TCs the average of the plastic strain rate for these length amounts according to the simulation is approx. 0.6%. On the assumption that specimen with similar geometric properties show similar mechanical stress behaviour we can compare these results to other simulations. Doing so the crack length after 2000 high TC, e.g. in the die attach of the specimen with 6x6mm² chip size and 75µm stencil thickness (dotted red graph) lies about 136µm and for the one with a 9x9mm² chip size and 150µm stencil thickness (orange graph) only at 50µm.

In the experiment we never observed any damage in the die attach of the specimen with 9x9mm² chip size and a stencil thickness of 75µm at low TC loading. In the simulation (blue graph) the value of 0.6% plastic strain per TC never is reached for any crack length so crack growing can assumed to be much slower than in the high TC loading.

5 CONCLUSIONS

In this deliverable a general approach defining a life-time model for thermal die attach was developed. A sinter-Ag die attach was choosen as demonstator. The whole processes from fabrication, material characterization up to the numerical assisted evaluation of reliability aspects were numerically modeled. It was found that in general the damage behavior correlates with the numerical approach done by FE-modeling which allows to compare the effects of geometric and material design parameter on the die attach reliability.

Due to described problems with the test vehicles a new set of test specimens were fabricated and prepared to undergo the cycling procedure again. From these experimental results it is straight forward to develop a lifetime model on the combination of experimental data and numerical simulations developed within this deliverable.

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