

1. Publishable summary

Introduction:

The NANOFUNCTION Network of Excellence aims to integrate at the European level the excellent European research laboratories in order to strengthen scientific and technological excellence in the field of novel nanoelectronic materials, devices and circuits for developing new integrated functions and to disseminate the results to the wide scientific and industrial communities. The NoE is particularly focusing on the convergence of Advanced More than Moore (MtM) for adding functionalities to ICs and Beyond-CMOS, which could be integrated on CMOS platforms. In particular, the interest of these nanodevices for the development of innovative applications with increased performance in the field of nanosensing, energy harvesting, nanocooling and RF, for the development of future nanosystems, is thoroughly investigated. There are two main motives for using nanoscale devices in the MtM domain: i) miniaturisation remains a major enabler for price reduction, functionality multiplication, and integration with the electronics; ii) nanoscale structures can improve device's intrinsic performance or enable new functionality. As a very good example, nanowires have received much attention from the R&D community as future components for electrical circuits based on CMOS compatible processes. These activities have been initiated to address the future need of IC technologies beyond the physical limits of CMOS, but nowadays other very interesting research activities are devoted to using NW to create innovative MtM products.

This work is carried out through a network of joint processing, characterisation and modelling platforms. The consortium works closely with European industry and feeds back data and know-how on devices that deliver the required performance. This interaction will strengthen European integration in nanoelectronics, help in decision-making and ensure that Europe remains at the forefront of nanoelectronics for the next decades. A strong link has been established between modelling/simulation, processing and characterization activities within each WP/task. During the third year of Nanofunction, close links have been developed with other European and National Projects. We have studied some of the main scientific and technical challenges put forward by European nanoelectronics community in this field. The scientific results obtained in the joint Nanofunction projects, showing significant improvements over the state-of-the-art, and the integration and spreading of excellence activities organized by Nanofunction Partners, are summarized below for all the Work Packages.

All these activities will contribute to the durable integration of the partners. However, some very important specific actions have been developed for the strengthening of this durable integration: i) a new Partner became a Member of the Sinano Institute in 2013 (Univ. of Siegen), which is a legal entity (Scientific Association) created in January 2008 for the coordination of the European Academic Community working in the field of Nanoelectronics ; ii) the Joint Processing, Joint Characterization and Modelling Platforms, which have been developed and used in the framework of the Sinano, Nanosil and Nanofunction NoEs for our joint research activities, have been strengthened and are fully integrated as open Research Infrastructures in the Sinano Institute ; iii) a lot of Nanofunction partners have been strongly involved in the ENI2 initiative (European Nanoelectronics Infrastructure for Innovation) launched by STMicroelectronics, which is embedded in AENEAS. ENI2 proposes a long term strong European structuring with 3 levels representing all the European nanoelectronics activities in the full value chain: level 1, led by the Academic Community represented by the Sinano Institute –including all the Nanofunction Academic Partners- for long term research, level 2 managed by the pre-industrial European Institutes, and level 3 coordinated by the European industry including ST, Infineon, NXP, Micron, ASM, Thales and IBS; iv) a joint Workshop between Nanofunction/Sinano/ENI2/New Member States/Formal Soviet Union Countries was organized in

April 2013 in Kiev, in order to strengthen the collaboration between Eastern and Western Europe and propose future joint projects in the framework of H2020.

i) WP1 “Nanosensing with Si based nanowires”

Work package 1 “Nanosensing with Si based nanowires” focus on Si based nanowire FETs as sensors taking advantage of the mature and reliable CMOS process technology. A primary focus is placed on nanowires for detection of molecules in gases or liquids for gas monitoring, chemical analysis or biotechnology. Implementation of nanowires in arrays is an efficient and low cost approach to achieve fast acquisition of information. To permit silicon nanowires and arrays to reach their full potential as sensors, it will be necessary to integrate active elements, at each location of the array, to function as highly sensitive and selective sensors of molecules. Sensor arrays also provide the possibility of having different sensing elements in the array and thereby simultaneously detect various molecules. We explore the use of Si based nanowires / nanowire-FETs for improvement of sensitivity, resolution, selectivity and response time of the sensor. Special emphasis is put on the integration with CMOS technology in order to achieve low cost More Than Moore solution for a sensor with a high density ($>1000/\text{mm}^2$) of nanowires each working as individual sensing elements. The work package deals with nanowire fabrication, nanowire functionalization, simulation and modeling and nanowire sensor integration with CMOS readout circuits. During the first year of Nanofunction CMOS compatible nanowire fabrication processes has been developed and the pros and cons of different process schemes was evaluated with respect to a sensor array application. Silicon nanowires were fabricated to be distributed between partners for sensing experiments. During the second year nanowire functionalization techniques in liquid and vapour phase for DNA grafting was developed and evaluated. Localized functionalization of the nanowires was confirmed by fluorescence images. The fundamental detection limit of silicon nanowires as charge sensing element was evaluated using a non-equilibrium Green function quantum microscopic approach for transport. It was shown that single charge detection is possible in dry environment and that the sensitivity is reduced in liquid ionic solutions due to ionic screening effects. Furthermore a straight-forward implementation of an “electrolyte” material into the commercial TCAD simulator was demonstrated. This approach has the advantage of exploiting all the features of the TCAD tools but a disadvantage of the relatively simple treatment of the electrolyte. A silicon nanowire based sensor was designed with 1024 individual nanowire pixels together with associated read-out circuits. During the third year a process was developed to integrate the silicon nanowire pixels into a fully depleted SOI CMOS process. The full process enables high density of individually accessible silicon nanowires ($\sim 3900 \text{ mm}^{-2}$) using co-integration with CMOS. Furthermore a full impedance sensing circuit was designed and fabricated to measure both magnitude and phase of silicon nanowires.

ii) WP2 “Exploration of new materials, devices and technologies for Energy Harvesting”

The first Task investigates nano-materials and devices for harvesting energy from vibration in the ambient. During the third year, the activities were focused on three complementary objectives:

- the development of large-area AlN piezoelectric MEMS transducers based on a new device architecture, designed to increase the generated voltage and output power. The characterization of the fabricated prototypes has shown voltages around 400-500mV and output powers exceeding 1uW, demonstrating the capabilities of this technology for energy generation;
- FEM modeling of piezoelectric energy harvesters which were designed and fabricated by CNR-NANO and IUNET. Models including the coupling of electromechanical and electrical properties

when the device is connected to an electrical load represent a key step for the design and optimization of mechanical energy harvesters;

The second Task is devoted to thermal to electrical energy conversion. Several paths are being followed.

One path consists in improving the manufacturability and the robustness of thermocouple based technology by developing a new insulation platform based on local formation of porous silicon. A complete thermoelectric generator (TEG) has been demonstrated, including the device and its appropriate package and housing. The TEG shows excellent output characteristics reaching an output power of $0.4\mu\text{W}/\text{cm}^2$ for a temperature difference of 10°C .

Another path consists of improving the thermoelectric properties of Si-based materials, as an alternative to some presently used materials which include rare or toxic elements, and for the integration opportunities that they offer. In particular, it is expected that material nanostructuring would allow electron conduction to be preserved while heat conduction should be decreased by phonon confinement (in ultra thin Silicon membranes, superlattices or nanowires) or by phonon scattering (with additional interfaces, heterojunctions or rough surfaces). VLS growth of axial Si/SiGe nanowires with excellent composition gradients has been demonstrated. The influence of low dimensionality on thermal and thermoelectric properties has been studied from both experimental and theoretical points of view. 3D atomistic approaches are being used to simulate phonon properties and heat flux in confined structures, taking into account spatial fluctuations. A full-quantum mechanical theory, coupled to self-consistent electron transport calculations, has been developed in order to extract thermoelectric factors of merit such as Seebeck coefficient and ZT parameter of nanowires. A strong improvement of the ZT factor of merit was obtained for a limited amount of roughness ($ZT \approx 0.74$ at room temperature for $3 \times 3 \text{ nm}^2$ square nanowires with 0.2 nm rms roughness, to be compared to $ZT \approx 0.01$ in bulk silicon). Experimentally, thin films and membranes of different materials have been studied. While thickness reduction was found to lead to a decrease on thermal conduction in crystalline Si self-suspended films, a more complex dependence was obtained with SiN_x , probably due to thickness dependent crystallinity.

A more fundamental study aims at better understanding an alternative mechanism, the *spin* Seebeck effect, which generates spin currents and associated voltages in the presence of a temperature gradient in a ferromagnet. The voltage is generated transverse to the temperature gradient, in a good electrical conductor, so that thermal and electrical conductivity can be fully separated, with the promise of efficient thermoelectric devices in a longer term. While the effect has been validated in Py, the efforts are now focusing on the exploration of Fe based materials, which proved difficult to process although they should theoretically lead to larger magnon drag effects.

Finally, we are also exploring an alternative route to thermoelectric processes in order to generate electrical power from temperature changes without the need for a cold source. It consists in coupling a shape memory alloy, which generates strain, to a piezoelectric material, which generates electric power under strain. The device is designed so as to enter into oscillation when heated across the thermoelastic transition of the shape memory alloy. Preliminary experimental results were obtained with TiN and PZT. They reached $4\text{-}5 \mu\text{J}/^\circ\text{C}$ with expected values for an optimized structure in the range of $25\text{-}50 \mu\text{J}/^\circ\text{C}$.

The third Task, the perspectives for advanced Si-nanowire (Si-NW) and CdTe core-shell based solar cells have been investigated. In particular, different technological options for the fabrication of Si-NW have been implemented and experimentally tested. In this context, electromagnetic simulators for the optical analysis of nano-structured cells have been used to perform electro-optical simulation in order to analyze the potential of NW-based solar cells.

The overall primary objective of the last Task was to review present and future technology capabilities of partners in terms of energy harvesting, storage and power management circuits and devices in the μW range & develop integration plans exploring opportunities for integration of such devices & circuits.

The net outcomes of these activities are as follows: (further details available in D2.4)

1. The co-development of miniaturized magnetic components for ultra-low voltage integrated power converters by IUNET & TYNDALL. Several sets of prototypes are available.
2. A table of availability of technology platforms from the partners was created.
3. An application orientated set of short and longer term roadmap for future development of transducers, power management and storage devices. This was created at 3 levels:- discrete, MEMS & NEMS. This is important to understand how these technologies need to converge for integration to meet certain application requirements
4. A Tyndall prototype nano/micro-battery cell was developed and tested.
5. A plan was developed for testing a IUNET device at Tyndall.
6. UCL developed a Dual-Mode DC/DC for 1V (min. 0.9 V) source that can operate down to 25 nW. Chips are available. The power management unit was simulated & submitted to fab, designed for $PV > 2 \mu W$.
7. Collaborative development by Tyndall & IUNET on power management circuits
8. Models for electromagnetic vibrational energy harvesting (VEH) devices were created by Tyndall. (These were added to the table of available platforms)
9. Simulation results from VTT were compiled based on a VTT platform but with human type vibrations in mind
10. Test results from TEG devices developed by NSCDR-IMEC as part of task 2.2 New materials and devices for Thermoelectric Energy Harvesting.

iii) WP3 “Nanocoolers”

This final year has culminated in some well co-ordinated activity with some excellent outcomes. Exchanges have been particularly valuable enabling fabrication and measurements to be undertaken. Three deliverables were completed during this period.

The rudimentary Si bolometer has been fully characterised and yields quite outstanding performance figures, notably NEP of $5 \times 10^{-18} \text{ W Hz}^{-0.5}$ and a response time of $< 1.5 \mu\text{s}$ at a temperature of 220 mK. A fully optimised bolometer promises world beating detector performance in the terahertz range using basic cryogenic apparatus, likely with good detector performance well into the infra-red. A Warwick/VTT patent will be filed shortly and the bolometer is the subject of a major £2M proposal for further study involving Warwick, VTT, Cambridge University and QMC Instruments Ltd. Intrinsic to this bolometer, is the greatly improved Si/Al tunnel junction (subject to a VTT/Warwick patent) which has yielded record electron temperature reductions from 300 mK to 90 mK, with temperature reductions from 1K to 30 mK in prospect. A venture capital company (Midven) and a major cryogenic company (Oxford Instruments) have expressed interest in the terrestrial applications of these bolometers. Studies by VTT/Warwick indicate that the electrical connection to the outside world is challenging but is likely possible via a SiGe bipolar technology. However, a fully depleted CMOS or single electron transistor (all devices operating at the cryogenic base temperature) may offer advantages.

Thermal isolation via epitaxial-compatible platforms included studies by ICN/VTT/Warwick on phonon transport using contactless laser probing and thermal conductivity (k) measurements on Warwick's 60 nm Ge membranes. These showed the increasing impact of low dimensionality with decreasing temperature, with x40 reduction in thermal conductivity compared to bulk Ge at 75 K. Work on an embryonic SOI membrane process was started. Continuing work on porous silicon (PS) platforms by IMEL/VTT took thermal conductivity (κ) measurements in sponge-like PS down to 20 K showing κ reduction levelling off but still four orders of magnitude lower than bulk Si and comparable to behaviour of insulators (e.g. SiO_2). IMEL also developed a clean metal PS fabrication process, suitable for epitaxy trials.

Overall Nanofunction has made very significant contributions in helping Europe maintain its pre-eminence in nano-cooling activity.

iv) WP4 "Exploration of new materials, devices and technologies for RF applications"

The main focus of WP4 was to explore the potential of nanowires (NWs) and other nanostructured materials in RF applications. The targeted applications include the development of Si-based substrate materials for the integration of RF passive devices on them, the development of novel device architectures and topologies, and the investigation of metal nanowires and nanostructured materials for their use as building blocks in RF interconnects and nano-antennas. The frequency range to be explored was from dc to 220 GHz.

The main achievements are as follows:

1. Porous Si was fully investigated as a local substrate material on Si for the on-chip integration of RF passives. A detailed study of its dielectric properties at RF was carried out at NCSR/IMEL, using coplanar waveguides as test structures. The dielectric permittivity of porous Si was determined using two methods of broadband dielectric characterization:
 - Following the Conformal Mapping approach and using analytical expressions to correlate S-parameters to the dielectric properties of the substrate.
 - Using full-wave 3D simulations for various values of the substrate dielectric parameters and comparing them to the measured S-parameters. The study was performed for porous Si layers of different porosity and morphology.
2. A full comparison between the state-of-the-art RF substrate trap-rich high resistivity Si and porous Si was undertaken (NCSR/IMEL and UCL). It was found that both substrates have excellent RF shielding properties that compare well with those of quartz. The advantage of porous Si is that it can be fabricated locally on a low resistivity Si wafer, so as high performance on-chip passives can be integrated on the Si wafer with CMOS logic devices.
3. Novel high performance slow-wave coplanar waveguides (s-CPWs) and filters on porous Si were investigated (NCSR/IMEL and FMNT/INP). Different devices were fabricated and characterized. For a proof-of-concept, low-pass step-impedance filters with a cut-off frequency equal to 30 GHz were first designed. Filters were also designed, combining CPW and S-CPWs technology on porous Si. This combination aims at (i) increasing the electrical performance of the filters, with a wide rejection bandwidth, and (ii) reducing the filters length because of the high characteristic impedance ratio between CPWs and S-CPWs attributed to the demonstrated high characteristic impedance achievable for CPWs on porous Si. First results demonstrated the superior performance of S-CPWs on porous Si compared with those on low-resistivity Si.
4. Al single wire lines in microstrip and CPW configuration were investigated (FMNT). A characterisation method was developed for each type of lines, together with corresponding modelling. After characterisation up to 100 GHz, line parameters were extracted. Good agreement between model and measurements was found. Cu single and multiple nanowire lines on a porous Si substrate were investigated (FMNT and NCSR/IMEL). The nanolines were characterized up to 110 GHz. Some measurements were also performed up to 210GHz. Corresponding modelling and simulation was developed. Nano antennas were designed, fabricated, characterized and modelled (FMNT and NCSR/IMEL). Some designs were realized on porous Si and the advantages of using this substrate at mm-wave frequencies were demonstrated.
5. The magnetic properties of different nanomodulated structures of various configurations have been investigated. These nanostructures were fabricated by using different technologies/combinations of technologies (electrodeposition, nanoimprint lithography). A generalised model has been developed for different anisotropy symmetry. Additionally, it was investigated how these unique nanostructure of continuous ferromagnetic film can induce magnetic dipoles at sub-micron scale at pre-defined

locations and play a key role to tune the global static and dynamic magnetic properties of the film due to dipole-dipole interactions. Gradual formation of magnetic dipoles and their tunability have been studied in detail by MFM imaging and other high resolution magnetic measurements. Change in dynamic properties due to strong dipole-dipole interaction is found as a unique observation.

6. The magnetic properties of nano particles embedded in porous silicon with vertical pores were investigated (collaboration of Tyndall with NCSR/IMEL).

v) WP5 “Integration and Spreading of Excellence”

Integration activities in Nanofunction are measured through the number of joint processing, characterization and modeling activities organized within each WP/Task as well as cross Task/WP activities. 27 joint activities were launched during this third year. Furthermore, the number of Task/WP as well as cross Task/WP meetings is chosen as an indicator of integration: 39 “technical” meetings were organized during this third period, including 2 cross-Task/WP meetings. “Who is Who Guide” was placed on the Nanofunction web-site to inform partners about specific competences available within Nanofunction community, search by “competence” is available. Exchanges of personnel further strengthened the expertise exchange and complementarity between partners. Two calls for exchanges were issued during this third year. 63.5 weeks of exchanges were selected by the Nanofunction Executive and Scientific Committee (E&SC).

Additionally to the integration within Nanofunction, the cooperation with other EU and national projects was stimulated. Screening of the national projects of relevance performed by Nanofunction partners revealed 9 national projects in the fields related to Nanofunction. 13 new projects (both EU and national) launched by Nanofunction members this year demonstrate the high activity level of the network.

Spreading of excellence within and beyond Nanofunction is carried out through the support and organization of workshops/schools/trainings, which are available for a wide scientific community. 9 events were organized by Nanofunction partners during this third year, of which 5 were supported by Nanofunction.

Links with New Member States and Eastern Europe were reinforced with the support of the International Workshop on Functional Nanomaterials and Devices, which was held in April 8th-11th, 2013, in Kiev, Ukraine, with the support of an exchange between St Petersburg State Polytechnical University and a Nanofunction partner and with the organisation of an International Joint Sinano/Nanofunction/NMS/FSU/ENI2 Workshop “*Advanced process and device integration and innovative nanofunctions in Nanoelectronics*”.

The Virtual Centre of Excellence was strengthened by the integration of a new partner in the More than Moore/Beyond CMOS domains in the Sinano Institute since February 2013. The Sinano Institute is also strongly involved in the ENI2 initiative (European Nanoelectronics Infrastructure for Innovation) which is now embedded in AENEAS.

Dissemination of knowledge was additionally implemented through the Nanofunction website, issuing poster/ presentations given by Nanofunction partners at different international scientific events as well publications in high-level international journals:

- 54 publications among which 15 of them are joint.

- 135 conference/workshop presentations, among which 44 were invited presentations and 41 are joint.

Nanofunction web site:

<http://www.nanofunction.eu/>

Contacts:

- Scientific and project: Francis Balestra (balestra@minatec.grenoble-inp.fr)
- Administrative and financial: Sylvie Pitot (Sylvie.Pitot@grenoble-inp.fr)