1. Publishable summary

Introduction:

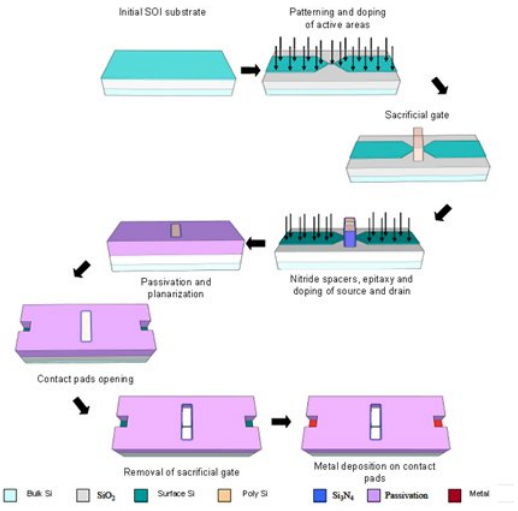
The NANOFUNCTION Network of Excellence aims to integrate at the European level the excellent European research laboratories in order to strengthen scientific and technological excellence in the field of novel nanoelectronic materials, devices and circuits for developing new integrated functions and disseminate the results in a wide scientific and industrial community. The NoE is particularly focusing on the convergence of Advanced More than Moore (MtM) for adding functionalities to ICs and Beyond-CMOS, which could be integrated on CMOS platforms. In particular, the interest of these nanodevices for the development of innovative applications with increased performance in the field of nanosensing, energy harvesting, nanocooling and RF is thoroughly investigated.
It is worth noting that novel MtM technologies will certainly have in the future strong link with Beyond CMOS technologies. The interaction between classical approaches and Beyond CMOS disruptive functions will offer significant opportunities for emerging markets. There are two main motives for using nanoscale devices in the MtM domain: i) miniaturisation remains a major enabler for price reduction, functionality multiplication, and integration with the electronics; ii) nanoscale structures can improve device's intrinsic performance or enable new functionality (such as ultra-high-sensitivity detection for chemical and biological applications). As a very good example, nanowires have received much attention from the R&D community as future components for electrical circuits based on CMOS compatible processes. These activities have been initiated to address the future need of IC technologies beyond the physical limits of CMOS, but nowadays other very interesting research activities are devoted to using NW to create innovative MtM products.
Other fields in which nanostructured materials and nanodevices could be very interesting are: i) energy autonomous systems using energy harvesting; these systems will become very important in the future for the development of "green/sustainable" applications; ii) high-performance, small size, low cost RF circuit based on new passives; optimisation of antenna architectures; iii) electronic cooling in CMOS compatible nanoscale systems by the management of the heat transfer. The integration of many different types of devices will be needed in the future, e.g. bio-sensors, NEMS devices, energy scavenging systems and RF interfaces, it is therefore very valuable to join our effort in this NoE to overcome the major challenges we are facing for the development of these future nanoelectronics systems.

This work is carried out through a network of joint processing, characterisation and modelling platforms. The consortium works closely with European industry and feeds back data and know-how on devices that deliver the required performance. This interaction will strengthen European integration in nanoelectronics, help in decision-making and ensure that Europe remains at the forefront of nanoelectronics for the next decades. A strong link has been established between modelling/simulation, processing and characterization activities within each WP/task. During the first year of Nanofunction, close links with other European Projects, the ENIAC Nanoelectronic Technology Platform, the AENEAS organization and National projects in the same fields have been established in order to enhance the overall efficiency of the European Research in Nanoelectronics. We have studied some of the main scientific and technical challenges put forward by European nanoelectronics community in this field. The scientific results obtained in the joint Nanofunction projects, showing significant improvements over the state-of-the-art, and the integration and spreading of excellence activities organized by Nanofunction Partners, are summarized below for all the Work Packages.
All these activities will contribute to the durable integration of the partners. However, some very important specific actions have been launched for the strengthening of this durable integration: i) five new Partners became Members of the Sinano Institute in 2011, which is a legal entity (Scientific Association) created in January 2008 for the coordination of the European Academic Community working in the field of Nanoelectronics ; ii) the Joint Processing, Joint Characterization and Modelling Platforms, which have been developed and used in the framework of the Sinano, Nanosil and Nanofunction NoEs for our joint research activities are now integrated as open Research Infrastructures

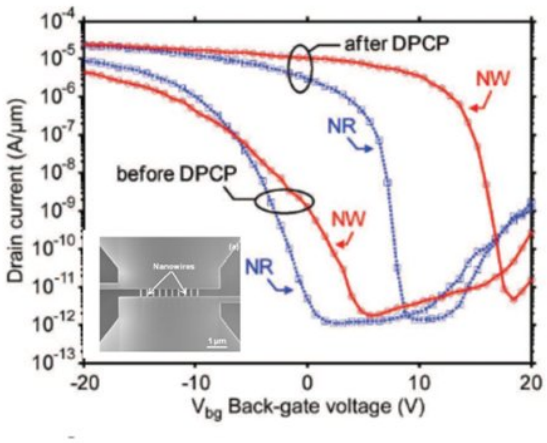
in the Sinano Institute ; iii) Nanofunction Partners and Sinano Institute Members have been strongly associated to the new initiative launched in 2010 by STMicroelectronics called ENI2 (European Nanoelectronics Infrastructure for Innovation). This Infrastructure propose a long term coordination of the three levels of R&D activities needed in the nanoelectronics domain (Academia, Institute, Industry) ; iv) many Nanofunction Partners have been involved in the FET Flagship "Guardian Angels" proposal dedicated to future autonomous ultra low power systems for health and environmental monitoring, selected as a pilot project in FP7

i) WP1 "Nanosensing with Si based nanowires"

Work package 1 "Nanosensing with Si based nanowires" focus on Si based nanowire FETs as sensors taking advantage of the mature and reliable CMOS process technology. A primary focus is placed on nanowires for detection of molecules in gases or liquids for gas monitoring, chemical analysis or biotechnology. Implementation of nanowires in arrays is an efficient and low cost approach to achieve fast acquisition of information due to parallel data recording. To permit silicon nanowires and arrays to reach their full potential as sensors, it will be necessary to integrate active elements, at each location of the array, to function as highly sensitive and selective sensors of molecules. Sensor arrays also provide the possibility of having different sensing elements in the array and thereby simultaneously detect various molecules. We explore the use of Si based nanowires / nanowire-FETs for improvement of sensitivity, resolution, selectivity and response time of the sensor. Special emphasis is put on the integration with CMOS technology in order to achieve low cost More Than Moore solution for a sensor with a high density (>1000/mm^2) of nanowires each working as an individual sensing elements. The work package deals with nanowire fabrication, nanowire functionalization, simulation and modeling and nanowire sensor integration with CMOS readout circuits. During the first year of Nanofunction CMOS compatible nanowire fabrication processes has been developed and pros and cons of different process schemes was evaluated with respect to a sensor array application. Silicon nanowires were fabricated to be distributed between partners for sensing experiments. Functionalization of silicon nanowires were explored for gas detection of a nerve gas simulant and a highly sensitive, fast and selective nanowire sensor was demonstrated. Flourescence were used to confirm that DNA grafting occurs either on the sides of the nanowire or on the top depending on the functionalization precursor. Single on-chip gold nanowires were shown to be excellent electrochemical sensors of glucose with high sensitivity. A methodology for implementing an electrolyte in commercial TCAD was achieved and analyte diffusion in a nanowire array was studied with implications for the pitch between nanowires in an array. Nanowire readout circuits were studied and designs to integrate a high density of nanowires with CMOS readout circuits were evaluated.



Developed CMOS compatible silicon nanowire process within Nanofunction..



Highly sensitive and selective detection of nerve gas simulant using silicon nanowires.

ii) WP2 "Exploration of new materials, devices and technologies for Energy Harvesting"

Workpackage WP2, "Exploration of new materials, devices and technologies for energy harvesting" investigated the use of micro-/nano-technologies and devices for a new generation of energy harvesting applications. Activities proceeded along four main directions: vibration scavenging, thermoelectrics, nanostructured solar cells and power conversion, management and storage.

A first part of activities (T2.1) has concerned the investigation of nano-materials and devices for harvesting energy from vibration present in the ambient. The activities have focused on the investigation of silicon-integrated piezoelectric MEMS and NEMS transducers based on aluminum nitride (AlN) and on high-k (spring constant) MEMS structures for harvesting the ambient mechanical energy. In order to understand the real potential of these micro-power piezoelectric generators, MEMS/NEMS prototypes have been fabricated by adopting a novel fabrication protocol, and such devices have been characterized by investigating their electro-mechanical and physical/piezoelectric properties through ad-hoc dedicated workbenches and techniques. Modeling and simulations have been largely used to design MEMS/NEMS device topologies with optimum performances, i.e. low mechanical losses, high mechanical-to-electrical energy conversion efficiency, higher output voltage and power. Future activities will concern the exploration of challenges/advantages related to the parallel/series connection of MEMS devices in array structures, the wideband and low stress operations, and the three-axis mode vibration operations.

A second task (T2.2) was devoted to improve the thermoelectric properties of Si-based materials, as an alternative to some presently used materials which include rare or toxic elements, and for the integration opportunities that they offer. To this end, several materials systems are being developed and characterized. The main objective is to decrease heat conduction by inducing phonon confinement (in ultra thin Silicon membranes or nanowires) or by increasing phonon scattering (by introducing additional interfaces, such as heterojunctions, or due to surface roughness in nanowires).
Several key experimental results have been obtained along these lines. Control of growth parameters for the Ge/SiGe system has been improved, making it possible to consider both heterostructured nanowires and superlattice thick stacks. Phonon confinement effects in ultra-thin Si membranes and its impact on heat transport have been simulated and characterized experimentally, while the thermal insulation properties of thick porous Si layers, which could serve to isolate the hot plate of a planar thermoelectric generator from the rest of the wafer, are under investigation. The current focus is on 3D simulations of phonon properties in confined structures such as semiconductor nanowires in the presence of spatial fluctuations. Work addresses phonon bandstructures and heat flux within a full-quantum mechanical theory to be coupled to self-consistent electron transport calculations in order to extract relevant factors of merit of thermoelectric devices.
Another aim is a better understanding of an alternative mechanism, the spin Seebeck effect, which generates spin currents and associated voltages in the presence of a temperature gradient in a ferromagnet. The voltage is generated transverse to the temperature gradient, in a good electrical conductor, so that thermal and electrical conductivity can be fully separated, with the promises of efficient thermoelectric devices in a longer term.

As a third task (T2.3), the perspectives for advanced Si-nanowire (Si-NW) based solar cells have been investigated. In particular, different technological options for the fabrication of Si-NW have been implemented and experimentally tested. In this context, electromagnetic simulators for the optical analysis of nano-structured cells have been developed and benchmarked. Finally, in preparation of the activity planned for the second year, test structures for simulation and fabrication have been defined.

In the fourth task (T2.4), templates have been created by participants to define 'applications orientated' specifications for energy harvesting, storage and power management circuits and devices. Roadmaps for these devices and circuits have also been created. All of these will be used to help converging and define demonstrators integrating the technologies developed by participants. In addition, an assessment of materials and 3D nanostructuring strategy has been undertaken for energy storage input to the roadmap
Besides this, smart power converters based on digital control were developed either with commercial off-the-shelf components or in CMOS integrated technology.

iii) WP3 "Nanocoolers"

WP3 is concerned with the development of a new technology called "Cooltronics", whereby huge performance enhancements or regimes are enabled when critical components in an electronic circuit are cooled to ultra-low temperatures (< 100mK). A prime example is radiation sensors particularly those involving a superconductor (S). A pre-requite of this technology is to eliminate "wet" cryogenic fluids from the cooling process and this involves using electronic cooling (e-cooling) to cool the components from 300mK to the lowest temperatures.
A new type of electron cooler is being developed in this WP involving strained silicon (sSi) and a superconductor; we have shown that this combination enables the electrons in the sSi to be highly thermally isolated from the sSi lattice phonons, hence much more responsive to incoming radiation. Work on an electron bolometer sensor involving sSi has been started. Reduced temperatures also dramatically reduce electronic noise and good thermal isolation of the sensor is critical. To achieve this, new approaches to thermal isolation are being explored including using porous silicon (PS) platforms, which are very robust compared to the thin SiN membranes currently being employed. Initial work on PS and also on thin semiconductor (Si, Ge) platforms has been carried out.

iv) WP4"Exploration of new materials, devices and technologies for RF applications"

The objectives of this workpackage are as follows:

The main focus is to explore the potential of nanowires (NWs) and other nanostructured materials in RF applications on the Si wafer. The targeted applications include the development of substrate materials for the on-chip RF shielding from the Si substrate, the on-chip integration of RF and mm-wave passive devices on the developed low-loss substrates, and the investigation of nanowires as building blocks in RF interconnects and nano-antennas. The frequency range to be explored is from dc to 220 GHz.

WP4 is divided into 4 tasks. The first one is devoted to the development of adequate local substrates on the Si wafer that can provide efficient RF shielding from the lossy Si substrate. The second task is devoted to the design, fabrication and testing of passive devices and circuits integrated on the local porous Si substrate. The third task is devoted to an exploratory work on novel nanostructured nanocomposite materials for their potential application in RF and the fourth task is devoted to the investigation of the electromagnetic properties of single nanowires or assemblies of nanowires and the study of nanowire interconnects and nano-antennas.

In the fist year of the project, significant results were obtained, as follows:
In task 4.1 porous Si layers locally formed on the Si wafer were studied in view of their application in on-chip RF shielding. Porous Si layers with different porosity, structure and morphology were fabricated and characterized. Field emission scanning electron microscopy was used to characterize their structure and morphology while dc electrical measurements were used to determine their resistivity. The RF shielding properties of the different porous Si layers were investigated by integrating co-planar waveguides (CPWs) on them and measuring the S parameters for frequencies from 40 GHz up to 110 GHz. It was shown that the value of the porosity of porous Si layers has a direct effect on the power loss of the CPWs.

Broadband electrical characterization of the CPWs on the porous Si layers showed that the attenuation loss was significantly reduced. By comparing the obtained results with the existing state-of-the art technologies it was shown that the use of a local porous Si layer implemented with CPW formation using process steps of an existing CMOS technology competes very well with the best literature results obtained so far for on-chip RF shielding. Porous Si provides an effective shielding to the lossy Si substrate.

Another important advantage of the porous Si layer technology is the possibility of realizing low-loss high-characteristic impedance transmission lines (TLs). The attenuation loss for a CPW TL with characteristic impedance equal to 145 Ω is of the same order of magnitude with that of CPW TL with 50-Ω characteristic impedance. Such a result cannot be achieved with the existing advanced CMOS technologies because of the very narrow metal strips that result from the design.

In task 4.2, based on the results of broadband electrical characterization of coplanar waveguides (CPWs) realized on local porous Si layers, novel slow – wave surface coplanar waveguides (s-CPWs) were designed and are currently under realization. Electromagnetic simulations were carried out from dc to 40GHz using the 3-D FFM simulation tool ANSOFT HFSS. The simulations showed that the presence of the porous Si layer underneath the s-CPW TLs reduces significantly the attenuation constant, mainly at higher frequencies. The quality factor of the TLs was found to increase from 2.5 without porous Si to 27 with the porous Si layer underneath the TLs. Moreover, it was found that the effective dielectric constant can be a factor of 25 higher with the porous Si layer than in standard CMOS. This can lead to very short TLs and hence miniaturized mm-wave passive devices.

In task 4.3 the focus this year was to investigate different nanostructures for controllable magnetic anisotropy. Configuration of magnetization directions is one of the most significant challenges in application of magnetic materials in devices, since the magnetic properties are determined by magnetization configuration. One of the existing methods to control magnetization configuration is surface nanomodulation. Within this task, a micromagnetic simulation study of key features of complete nanomodulation-based directional anisotropy in continuous $Ni_{45}Fe_{55}$ magnetic thin films at room temperature was conducted. Several new ideas to produce symmetric directional anisotropy were introduced by simulations and validated by experiments. It was demonstrated that artificially created surface roughness produces in-plane anisotropy. A proper orientation of surface anisotropy can dominate intrinsic anisotropy of the magnetic film. The symmetry of roughness geometry enhances the effect. It was also possible to propose a model to obtain a controllable anisotropy in continuous magnetic thin-film.

In task 4.4 the main focus was to model and simulate nanowires for their use in nano-interconnects and nano-antennas. The nanowires are simulated by an equivalent electrical circuit in order to obtain a model that can be incorporated into existing CAD tools.

v) WP5 "Integration and Spreading of Excellence"

Integration activities in Nanofunction are measured through the number of joint processing, joint characterization and modeling activities organized within each WP/Task as well as cross Task/WP activities. 12 joint activities were launched during this first year. Furthermore, the number of Task/WP as well as cross Task/WP meetings is chosen as an indicator of integration: 16 "technical" meetings were organized during this year, including 3 cross-Task/WP meetings. "Who is Who Guide" was placed on the Nanofunction web-site to inform partners about specific competences available within Nanofunction community, search by "competence" is available. Exchanges of personnel further strengthened the expertise exchange and complementarity between partners. Four calls for exchanges were issued during this first year. 24.5 weeks of exchanges were selected by Nanofunction Executive and Scientific Committee (E&SC).

Additionally to the integration within Nanofunction, the cooperation with other EU and national projects was stimulated. Screening of the national projects of relevance performed by Nanofunction partners revealed 7 national projects in the fields related to Nanofunction. 7 new projects (both EU and national) launched by Nanofunction members this year demonstrate the high activity level of the network.

Spreading of excellence within and beyond Nanofunction is carried out through the support and organization of workshops/schools/trainings, which are available for a wide scientific community. 15 events were organized by Nanofunction partners during this first year, of which 6 were supported by Nanofunction.

Links with New Member States were initiated with the support for the participation of a Rimanian PhD at the MIGAS International Summer School 2011 and with the support for the participation of 2 researchers from Poland to the Nanofunction workshop in Helsinki.

The Virtual Centre of Excellence was strenghthened by the integration of new partners in the More than Moore/Beyond CMOS domains in the Sinano Institute since January 2011. And the Sinano Institute is also strongly involved in the ENI2 structure wich will led to a strong structuring and long term coordination of the 3 levels of European actors.

Dissemination of knowledge was additionally implemented through the Nanofunction website, issued poster, presentations given by Nanofunction partners at different international scientific events as well publications in high-level international journals:
- 12 publications among which 2 of them are joint.
- 58 conference/workshop presentations,among which 10 were invited presentations and 25 are joint presentations.

Nanofunction web site:
http://www.nanofunction.eu/

Contacts:

-Administrative and financial: Sylvie Pitot (Sylvie.Pitot@grenoble-inp.fr)
-Scientific: Francis Balestra (balestra@minatec.grenoble-inp.fr)