1. PUBLISHABLE SUMMARY

WADIMOS - WAVELENGTH DIVISION MULTIPLEXED PHOTONIC LAYER ON CMOS

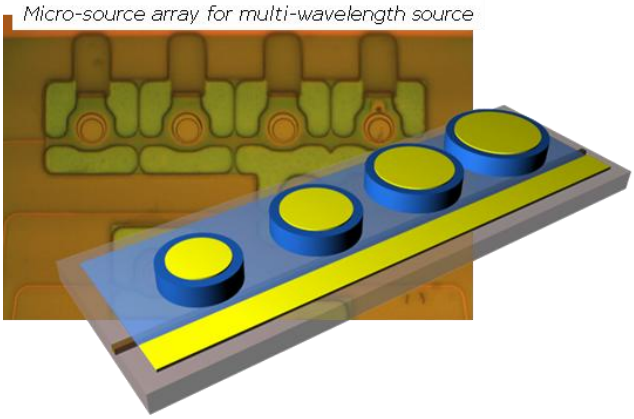
Abstract: WADIMOS is a EU funded research project aiming at demonstrating a photonic interconnect layer on CMOS. WADIMOS has six partners and a total budget of 3.2MEuro. The project started on Jan. 1, 2008 and will run for three years.

BACKGROUND

The enormous computing power of multi-processor systems and manufacturing tools now on the drawing table will require data transfer rates of over 100Terabit/s. These data rates may be needed on-chip, e.g. in multicore processors, which are expected to need total on-chip data rates of up to 100TB/s by 2015, or off-chip, e.g. in short distance data interconnects, requiring up to 100TB/s over a 10m to 100m long distance. The only viable technology for transmitting this level of information is using optical interconnects. Besides a huge data rate, optical interconnects also allow for additional flexibility through the use of wavelength division multiplexing. This additional flexibility may be employed for more intelligent interconnect systems, such as the optical network-on-chip system also investigated in this project.

OBJECTIVE

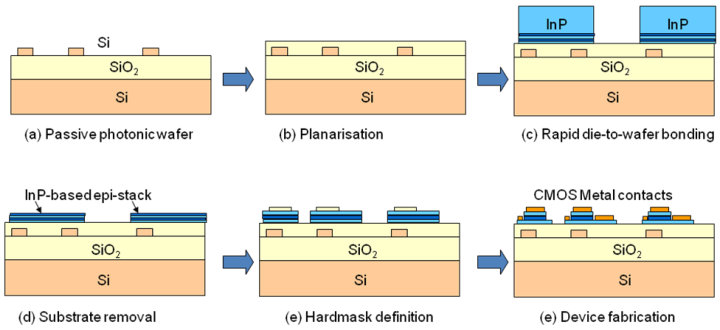
WADIMOS will build a complex photonic interconnect layer incorporating multi-channel microsources, microdetectors and different advanced wavelength routing functions directly integrated with electronic driver circuits and demonstrate the application of such electro-photonic ICs in two representative applications:



- *Optical Network on Chip for ST Microelectronics multi-processor chips*. Inter-processor communication rates will soon reach an aggregated bandwidth of several hundred GHz. Several new electrical interconnect architectures are currently under investigation but despite these efforts still the International Technology Roadmap for Semiconductors predicts that interconnects will become the bottleneck of integrated systems-on-chip. Therefore, WADIMOS works on the realization of an optical NoC. The photonic layer will include complex wavelength division multiplexing functionality both for increasing the data rate and for increasing the routing flexibility since there is a broad consensus that this is the only approach really bringing added value to the network-on-chip.
- *Terabit optical datalink for MAPPER.* Mapper lithography is a semiconductor equipment company focusing on the development and manufacturing of a new and highly competitive maskless lithography machine using thousands of electron beams for writing the desired patterns. The electron beams are controlled by shutters in a beam blanker ship, which are controlled by an optical signal. This requires a data-rate of over 100TB/s between the subfab, where the patterns are generated, and the actual lithography equipment. At this moment, each of the thousands ebeam gates requires a separate optical beam, delivered through a separate optical fiber for controlling it. We will investigate if optical wavelength multiplexing can be used to decrease the number of optical fibers required

TECHNOLOGY PLATFORM

Nowadays a technology platform, which can fulfill the requirements of the applications described above, does not exist and until recently it also did not seem realistic to believe this level of photonic circuit integration would even be possible. However, the recent emergence of the new research domain that is now commonly called "Silicon Photonics" has completely changed this picture. The high refractive index of silicon in the near infrared allows for the fabrication of very compact photonic circuits. Moreover, these circuits can be fabricated using the advanced and very reliable processing tools also used for the fabrication of electronic circuits. In recent years, the different basic functions necessary for realizing complex photonic ICs were all demonstrated – among others by the partners of this consortium and we believe this technology now has reached the level whereby these individual functions can be combined into much more complex circuits and directed towards specific applications, such as on-chip optical networks and terabit optical links.

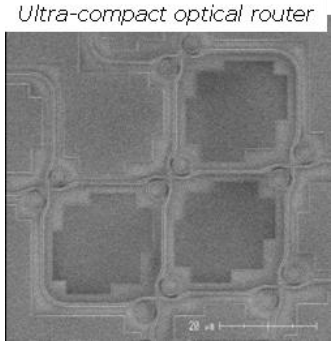


The basic technology was developed in the context of the FP6 project PICMOS. It is based on an optical layer consisting of silicon nanophotonic waveguides integrated with III-V micro-optoelectronic components. A waferscale compatible heterogeneous integration approach based on a rapid die-to-wafer bonding process was developed. WADIMOS will extend this technology platform considerably:

- In PICMOS only single point-to-point links were demonstrated. Within WADIMOS, we are demonstrating complex wavelength routing based functionality.
- In PICMOS, only part of the process was carried out in a CMOS pilot line. Within WADIMOS, we are developing the processes for fully processing the III-V optoelectronic components in a CMOS-pilot line
- Improved optoelectronic devices will be developed, including:
    - Faster and lower power consumption micro-sources
    - Detectors integrated in the same epitaxial layer as the micro-sources
    - Complex passive circuitry, including optical router and novel "scissor" devices
- In WADIMOS, two practical applications – optical network on-chip and terabit link for massive parallel ebeam writer – are studied in detail and functional demonstrators will be realized.

PROJECT TEAM

The project includes partners from industry (STM, MAPPER) as well as major research institutes and universities (IMEC, CEA-LETI, INL, UNITN). Both partners with a strong background in electronics as partners with an outstanding track record in photonics are part of the consortium. ST Microelectronics is one of the world leading suppliers of electronic IC's while IMEC and CEA-LETI are the largest European research institutes on microelectronics. Mapper Lithography, a Delft University spin-off is developing a massively parallel ebeam writing system for future electronic circuit fabrication. On the other hand, UNITN, INL and the IMEC photonics research group are part of the world's leading research groups on optics and photonics.


Ultra-compact optical router

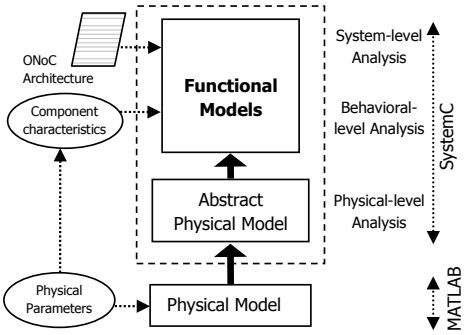
IMEC coordinates the project and designs ultra-compact SOI waveguide circuits for routing and demultiplexing. IMEC also contributes to the fabrication of the μsources and their integration with the waveguides. **ST Microelectronics** is investigating the viability of optical networks-on-chip and designs the required CMOS-circuits. **CEA-LETI** develops the integration process and fabricates the photonic layer in a standard CMOS pilot line, including the III-V based microsources. **INL** is involved in the design and fabrication of the microsource arrays, contributes to the optoNoC system studies and is responsible for the design of the optical

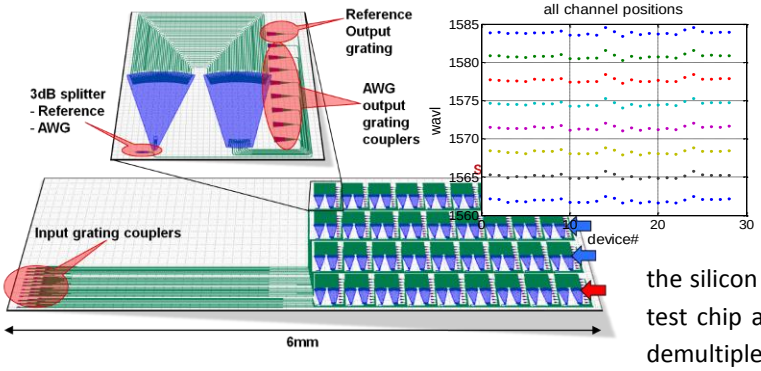
routers. **UNITN** is designing innovative optical WDM circuits based on coupled ring resonators. **MAPPER** is responsible for the system studies related to the terabit optical link.

MAIN RESULTS FOR YEAR 2

During year 1 the theoretical ground work for the project was laid out and the supporting processes for realizing the fully integrated network were developed. The main objective for year 2 was to use these processes for realizing the first demonstrators.

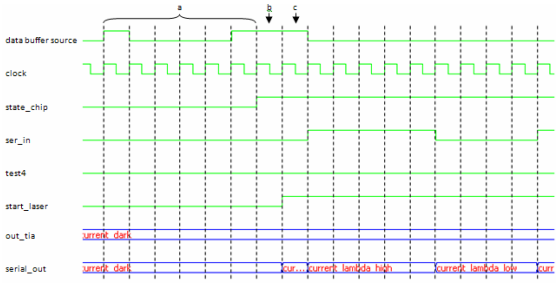
In WP1 (The design study for the **optical network-on-chip** or ONoC) we have completed the development of a reconfigurable ONoC model that can be used for analyzing the network at three hierarchical levels: system level, behavioral level, and physical level, built on a novel protocol stack architecture for the ONoC. The proposed model has been integrated successfully inside an industrial development environment (ST OCCS GenKit) using an industrial standard (VSTNoC) protocol. Such an environment allows to define a system and its interconnect placing and connecting the ONoC, configuring it according to the specific application, simulating and characterizing the whole system (and in particular the interconnect) in terms of performance metrics (latency, throughput).

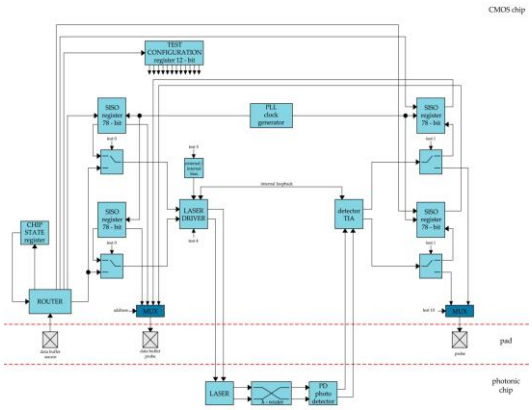




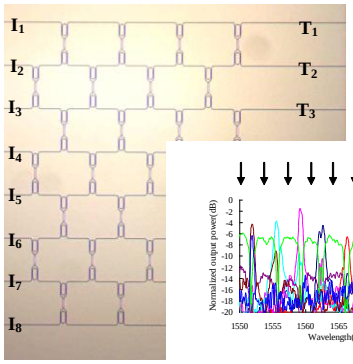
In the context of the demonstrator fabrication for the **MAPPER** terabit data link, we proofed the high yield of the silicon nanophotonic waveguide fabrication process. We realized a test chip addressing over 200 channels, using 36 identical wavelength demultiplexers. All channels were operational. These chips will now be integrated with photodetectors and in a next step with CMOS receiver circuits.

In WP3, we are developing the **CMOS circuits** needed to drive the ONoC demonstrator. Starting from the global CMOS chip architecture and definition we completed the front-end design and simulation of both the analog and digital components. The analog part includes the laser and receiver drivers and is running up to 4GHz. The digital part includes both the components needed for the actual ONoC (serializers, buffers …) and the components needed for testing the circuits in different configurations. A dedicated 4GHz PLL (phase locked loop) to clock the analog parts was designed and validated. VHDL models were developed for the analog drivers and the optoelectronic components and integrated with the digital models. In this way the top level operation of the whole chip could be simulated.



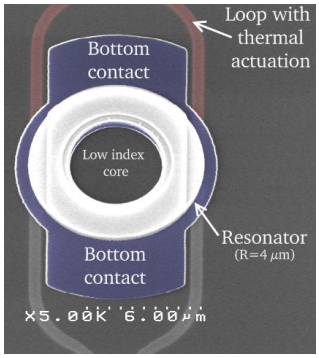


The passive optical components needed for routing and filtering the optical signals based on their wavelength are studied in WP4. During year 2 we characterized the circuits, which were designed and fabricated in the first

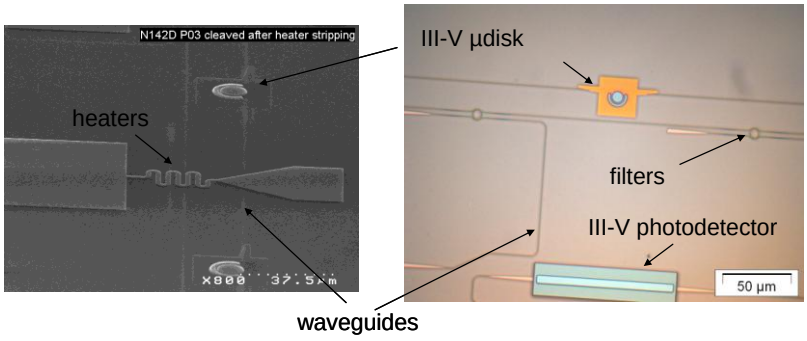


project year. This included the characterization of all the basic components required for building a ring resonator based wavelength router. Using these results a full 8x8 router was designed and fabricated. We also improved the performance of flat passband AWG-based demultiplexers, required for the terabit link demonstrator. Thorough characterization of "Side-Coupled Integrated Spaced-Sequences of Resonators" or SCISSORS, by taking top view scatter images, has led to a better understanding of their operation and sensitivity to fabrication issues. New designs have been prepared and the characterization setup has been improved to allow for phase tuning of a double input signal. In the manufacturability study we characterized the influence of wafer thickness variations, slit uniformity and pattern density on the uniformity. We made a proposal for uniformity improvement based on exposure dose compensation and fabricated integrated micro-heaters to allow tuning or trimming of wavelength selective circuits.

In WP5, which is focusing on the **active devices** we demonstrated this year devices with substantially improved output power (under CW operating conditions) and lower threshold current, fabricated on small samples. This was made possible by an improved epitaxial layer design and growth, improved etching and better heat sinking. The WADIMOS target of a 150μW seems within reach. We also experimentally demonstrated thermal tuning of the resonance wavelength of the microdisk lasers. Based on a thorough design study, we proposed the racket-shape micro ring resonator, which allows unidirectional lasing and wavelength tuning. Next to these we finalized the development of the fabrication processes required for the 200mm wafer compatible fabrication of the demonstrators, including CMOS compatible contacts for n- and p-type III-V semiconductors and an improved plasma etch process.



WP6 is devoted to the **integration process** and coordination of the **demonstrator** fabrication. During year 2 we worked on the fabrication of the first generation demonstrator (WAD1), including the transmitter for the terabit link. The processing was delayed several times due to equipment failure and (to a lesser extend) unexpected processing issues but is now nearing completion. The demonstrator will include sources, detectors and thermally tunable filters. In the mean time we also completed the mask file definition of the second generation demonstrator and its fabrication has started.



CONCLUSION

During year 2 considerable progress has been made in the project. A full performance exploration and scalability analysis of the ONoC was carried out and the CMOS design for the demonstrator has been completed. The passive circuits for the different demonstrators were fabricated and thoroughly characterized. We demonstrated microdisk lasers with record low threshold and substantial processing improvements in epitaxial layer growth, etching and metallization. New concepts for tuning and trimming of these devices were proposed and investigated in detail. The first worldwide demonstration of III-V-active devices fully fabricated in a CMOS pilot line is nearing completion and the second demonstrator run has started.