1. PUBLISHABLE SUMMARY

WADIMOS - WAVELENGTH DIVISION MULTIPLEXED PHOTONIC LAYER ON CMOS

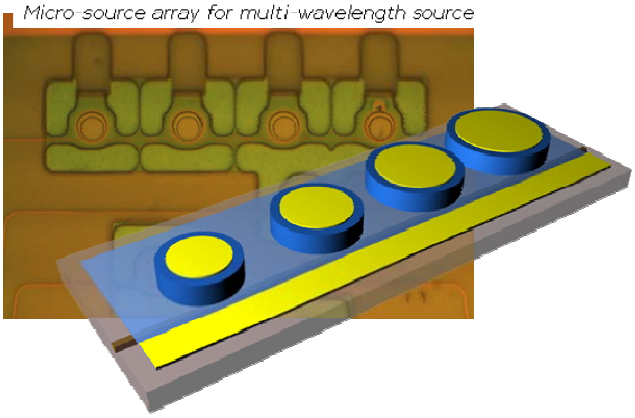
Abstract: WADIMOS is a EU funded research project aiming at demonstrating a photonic interconnect layer on CMOS. WADIMOS has six partners and a total budget of 3.2MEuro. The project started on Jan. 1, 2008 and will run for three years.

BACKGROUND

The enormous computing power of multi-processor systems and manufacturing tools now on the drawing table will require data transfer rates of over 100Terabit/s. These data rates may be needed on-chip, e.g. in multicore processors, which are expected to need total on-chip data rates of up to 100TB/s by 2015, or off-chip, e.g. in short distance data interconnects, requiring up to 100TB/s over a 10m to 100m long distance. The only viable technology for transmitting this level of information is using optical interconnects. Besides a huge data rate, optical interconnects also allow for additional flexibility through the use of wavelength division multiplexing. This additional flexibility may be employed for more intelligent interconnect systems, such as the optical network-on-chip system also investigated in this project.

OBJECTIVE

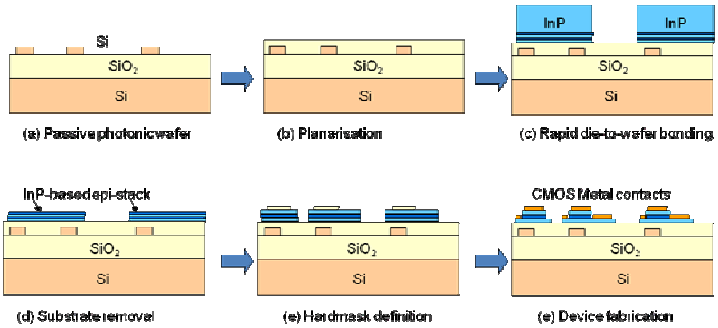
WADIMOS will build a complex photonic interconnect layer incorporating multi-channel microsources, microdetectors and different advanced wavelength routing functions directly integrated with electronic driver circuits and demonstrate the application of such electro-photonic ICs in two representative applications:



- *Optical Network on Chip for ST Microelectronics multi-processor chips*. Inter-processor communication rates will soon reach an aggregated bandwidth of several hundred GHz. Several new electrical interconnect architectures are currently under investigation but despite these efforts still the International Technology Roadmap for Semiconductors predicts that interconnects will become the bottleneck of integrated systems-on-chip. Therefore, WADIMOS works on the realization of an optical NoC. The photonic layer will include complex wavelength division multiplexing functionality both for increasing the data rate and for increasing the routing flexibility since there is a broad consensus that this is the only approach really bringing added value to the network-on-chip.
- *Terabit optical datalink for MAPPER.* Mapper lithography is a semiconductor equipment company focusing on the development and manufacturing of a new and highly competitive maskless lithography machine using thousands of electron beams for writing the desired patterns. The electron beams are controlled by shutters in a beam blanker ship, which are controlled by an optical signal. This requires a data-rate of over 100TB/s between the subfab, where the patterns are generated, and the actual lithography equipment. At this moment, each of the thousands ebeam gates requires a separate optical beam, delivered through a separate optical fiber for controlling it. We will investigate if optical wavelength multiplexing can be used to decrease the number of optical fibers required

TECHNOLOGY PLATFORM

Nowadays a technology platform, which can fulfill the requirements of the applications described above, does not exist and until recently it also did not seem realistic to believe this level of photonic circuit integration would even be possible. However, the recent emergence of the new research domain that is now commonly called "Silicon Photonics" has completely changed this picture. The high refractive index of silicon in the near infrared allows for the fabrication of very compact photonic circuits. Moreover, these circuits can be fabricated using the advanced and very reliable processing tools also used for the fabrication of electronic circuits. In recent years, the different basic functions necessary for realizing complex photonic ICs were all demonstrated – among others by the partners of this consortium and we believe this technology now has reached the level whereby these individual functions can be combined into much more complex circuits and directed towards specific applications, such as on-chip optical networks and terabit optical links.

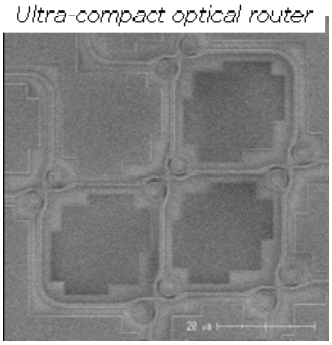


The basic technology was developed in the context of the FP6 project PICMOS. It is based on an optical layer consisting of silicon nanophotonic waveguides integrated with III-V micro-optoelectronic components. A waferscale compatible heterogeneous integration approach based on a rapid die-to-wafer bonding process was developed. WADIMOS will extend this technology platform considerably:

- In PICMOS only single point-to-point links were demonstrated. Within WADIMOS, we will demonstrate complex wavelength routing based functionality.
- In PICMOS, only part of the process was carried out in a CMOS pilot line. Within WADIMOS, we will develop the processes for fully processing the III-V optoelectronic components in a CMOS-pilot line
- Improved optoelectronic devices will be developed, including:
    - Faster and lower power consumption micro-sources
    - Detectors integrated in the same epitaxial layer as the micro-sources
    - Complex passive circuitry, including optical router and novel "scissor" devices
- In WADIMOS, two practical applications – optical network on-chip and terabit link for massive parallel ebeam writer – are studied in detail and functional demonstrators will be realized.

PROJECT TEAM

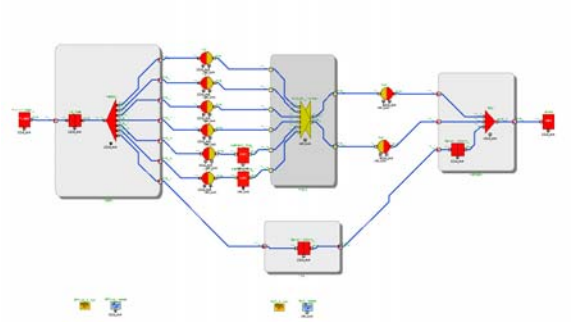
The project includes partners from industry (STM, MAPPER) as well as major research institutes and universities (IMEC, CEA-LETI, INL, UNITN). Both partners with a strong background in electronics as partners with an outstanding track record in photonics are part of the consortium. ST Microelectronics is one of the world leading suppliers of electronic IC's while IMEC and CEA-LETI are the largest European research institutes on microelectronics. Mapper Lithography, a Delft University spin-off is developing a massively parallel ebeam writing system for future electronic circuit fabrication. On the other hand, UNITN, INL and the IMEC photonics research group are part of the world's leading research groups on optics and photonics.


Ultra-compact optical router

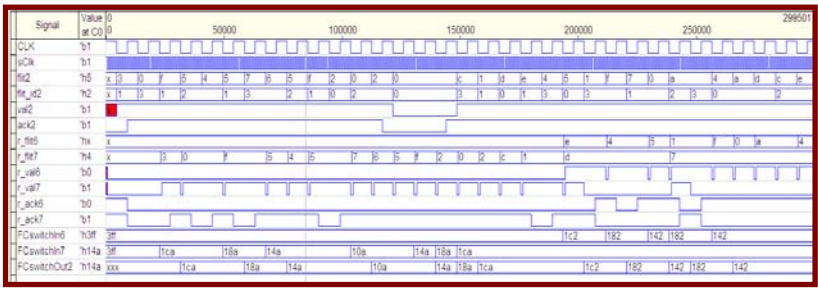
IMEC coordinates the project and designs ultra-compact SOI waveguide circuits for routing and demultiplexing. IMEC also contributes to the fabrication of the μsources and their integration with the waveguides. **ST Microelectronics** is investigating the viability of optical networks-on-chip and designs the required CMOS-circuits. **CEA-LETI** develops the integration process and fabricates the photonic layer in a standard CMOS pilot line, including the III-V based microsources. **INL** is involved in the design and fabrication of the microsource arrays, contributes to the optoNoC system studies and is responsible for the design of the optical routers. **UNITN** is designing innovative optical WDM circuits based on coupled ring resonators. **MAPPER** is responsible for the system studies related to the terabit optical link.

MAIN RESULTS FOR YEAR 1

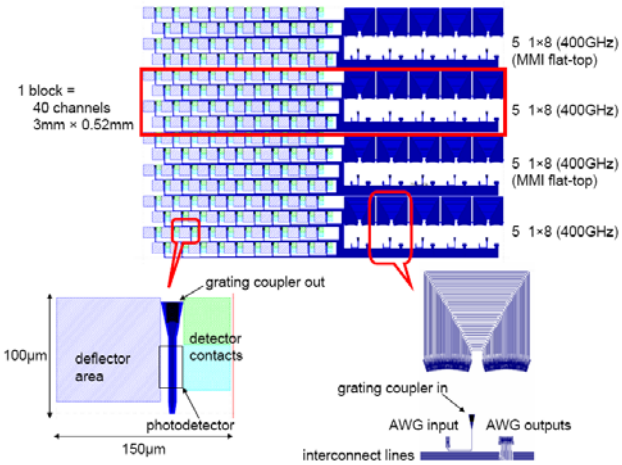
The main objectives for year 1 were to carry out an extensive system study for the two applications under study, to study in depth the basic components and processes required for the optical layer, to propose an integration scheme and to start processing of the first generation demonstrator. These objectives were largely reached.



The design study for the **optical network-on-chip** (ONoC)(WP1) has lead to a detailed *architectural description* (D1.1 and updated in D1.2) and to a set of *specifications for the subcomponents*, including the CMOS circuits (WP3), the passive router structure (WP4) and the active optoelectronic components. A demonstrator mapped on a typical application with 6 initatior IP blocks (e.g. computing blocks) and 2 target IP blocks (e.g. memory blocks) was proposed. Full bi-directional optical links between these blocks (6 to 2) will be provided. A *systemC* model for the electronic part of the demonstrator was developed in ST relying on the OCCS Genkit, an ST internal tool. At the same time, INL developed *system C models* for the optical parts. These models will be integrated in year 2 of the project.

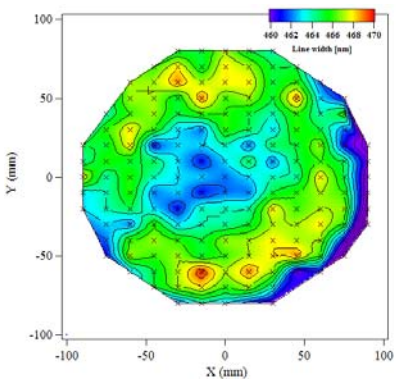


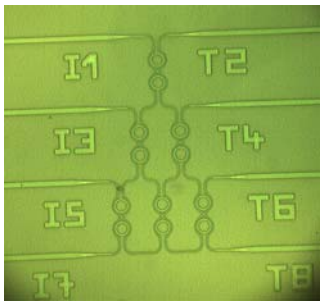
The system study for the **MAPPER** application (WP2) was focused on the possibility to integrate wavelength multiplexing functionality directly on the beam blanker chip. This requires integrating hundreds optical demultiplexers on the beam blanker chip, which has a size of only a few cm^2. Using currently commercially available devices this would be completely out of the question. Even a single such device would not fit on the surface of the chip. And although the ultracompact silicon photonic circuits investigated in this project allow reducing the size of the optical demultiplexer by several orders of magnitude, the requirements imposed by the application remain challenging. However, an extensive system study (D2.1) has shown that a demultiplexing rate of 16 should be feasible within the timeframe of the project. Based on this, an initial demonstrator chip was designed. Also approaches for extending the demultiplexing ratio further were proposed.



The component workpackages are focused on the CMOS circuits required for the demonstrators, the passive optical components and the active optical components. The **CMOS circuits** (WP3) include the circuits for the ONoC and receivers for the terabit link. In year one, both the digital and the analog parts of the CMOS for the ONoC were studied in detail. In year 2, this will be continued and the circuits will be realized. Also receiver circuits for the mapper beam blanker were designed.

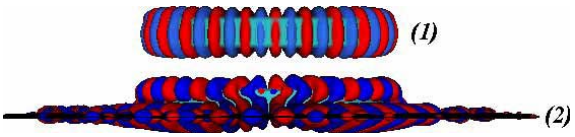
Also the **passive optical components** needed for routing and filtering the optical signals based on their wavelength are studied in a separate workpackage (WP4). For both applications the compactness of the devices is extremely important.





For the ONoC we studied a ring resonator based optical router, composed of individual building blocks, which allow switching a signal between two outputs based on its wavelength. By combining such blocks, a full wavelength router can be built. These basic blocks were fabricated and characterised in detail during year 1. The results will serve as input for the design of the router to be included in the final demonstrator. For the terabit link compact optical demultiplexer are required. Therefore we tested different AWG (arrayed waveguide grating) designs during year 1. Low loss was obtained for 8-channel devices with Gaussian passband and a size of only 250um x 300um. Flatband designs still need improvement and a second iteration of the latter is currently under fabrication. These are important for practical deployment: due to the high index contrast, silicon nanophotonic devices are extremely sensitive to small variations in the fabrication process. Having a flatband filter ensures some built-in tolerance for such deviations . However, in parallel, we are investigating how process variations can be avoided as much as possible. Therefore, during year 1, the existing fabrication process was characterized in detail and different possible causes for process variations were identified. Also in WP4, we're investigating how a novel type of devices, so called SCISSORS, can be used as an alternative for the ONoC.

The last component workpackage investigates **the active devices**, which are based on III-V microdisk devices, integrated on the silicon nanophotonic circuits. During the first year of the project we demonstrated for the first time direct modulation and multi-wavelength operation of such devices. We also developed an analytic model, which allows a fast design optimization. We also investigated different possibilities for tuning the emission wavelength of the devices, either based on directly changing the temperature of the microdisk or based on changing the properties of an external cavity integrated with the microdisk. Using these models, a first mask set was prepared and processing of a first generation of devices in a CMOS-pilot line was started. In parallel, also the specific processes needed were optimized, including the epitaxial layers, the bonding process, the etching – in a CMOS compatible reactor - and the CMOS-compatible contacts.



The last workpackage is devoted to the **integration process** and the **demonstrators**. During the first year, a full process flow for the photonic layer was defined in detail and formed the basis of the first generation devices.

CONCLUSION

All year 1 deliverables and milestones were completed with no or minor delay. The project is on-track and no major obstacles are foreseen at the moment. The project already has led to more than 5 journal publications, a number of invitations at international conferences and several ideas are currently under review for patent application. In year 2, we expect the first worldwide demonstration of III-V-active devices fully fabricated in a CMOS pilot line.