WADIMOS

Wavelength Division Multiplexed Photonic Layer on CMOS

WADIMOS is a EU funded research project aiming at demonstrating a photonic interconnect layer on CMOS. WADIMOS has six partners and a total budget of 3.2MEuro. The project started on Jan. 1, 2008 and will run for three years.

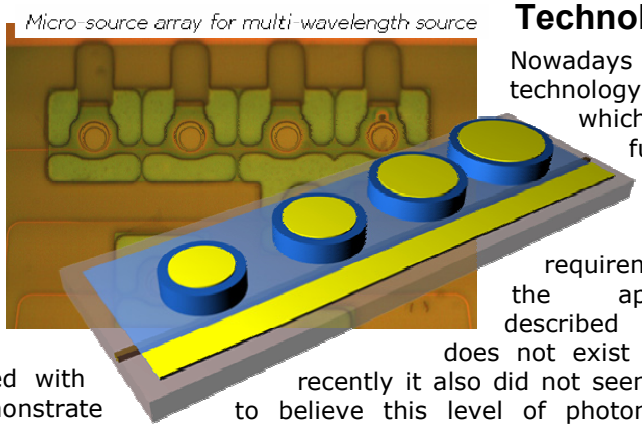
Background

The enormous computing power of multi-processor systems and manufacturing tools now on the drawing table will require data transfer rates of over 100Terabit/s. These data rates may be needed on-chip, e.g. in multicore processors, which are expected to need total on-chip data rates of up to 100TB/s by 2015, or off-chip, e.g. in short distance data interconnects, requiring up to 100TB/s over a 10m to 100m long distance. The only viable technology for transmitting this level of information is using optical interconnects. Besides a huge data rate, optical interconnects also allow for additional flexibility through the use of wavelength division multiplexing. This additional flexibility may be employed for more intelligent interconnect systems, such as the optical network-on-chip system also investigated in this project.

Objective

WADIMOS will build a complex photonic interconnect layer incorporating multi-channel microsources, microdetectors and different advanced wavelength routing functions directly integrated with electronic driver circuits and demonstrate the application of such electro-photonic ICs in two representative applications:

- *Optical Network on Chip for ST Microelectronics multi-processor chips*. Inter-processor communication rates will soon reach an aggregated bandwidth of several hundred GHz. Several new electrical interconnect architectures are currently under investigation but despite these efforts still the International Technology Roadmap for Semiconductors predicts that interconnects will become the bottleneck of integrated systems-on-chip. Therefore, WADIMOS works on the realization of an optical NoC. The photonic layer will include complex wavelength division multiplexing functionality both for increasing the data rate and for increasing the routing flexibility since there is a broad consensus that this is the only approach really bringing added value to the network-on-chip.
- *Terabit optical datalink for MAPPER.* Mapper lithography is a semiconductor equipment company focusing on the development and manufacturing of a new and highly competitive maskless lithography machine using thousands of electron beams for writing the desired patterns. This requires a data-rate of over 100TB/s between the subfab, where the patterns are generated, and the actual lithography equipment.



Micro-source array for multi-wavelength source

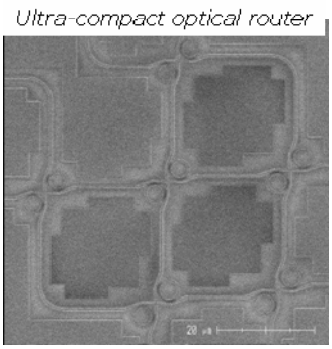
Technology

Nowadays a technology platform, which can fulfill the requirements of the applications described above, does not exist and until recently it also did not seem realistic to believe this level of photonic circuit integration would even be possible. However, the recent emergence of the new research domain that is now commonly called "Silicon Photonics" has completely changed this picture. The high refractive index of silicon in the near infrared allows for the fabrication of very compact photonic circuits. Moreover, these circuits can be fabricated using the advanced and very reliable processing tools also used for the fabrication of electronic circuits. In recent years, the different basic functions necessary for realizing complex photonic ICs were all demonstrated – among others by the partners of this consortium and we believe this technology now has reached the level

whereby these individual functions can be combined into much more complex circuits and directed towards specific applications, such as on-chip optical networks and terabit optical links.

Project team

The project includes partners from industry (STM, MAPPER) as well as major research institutes and universities (IMEC, CEA-LETI, INL, UNITN). Both partners with a strong background in electronics as partners with an outstanding track record in photonics are part of the consortium. ST Microelectronics is one of the world leading suppliers of electronic IC's while IMEC and CEA-LETI are the largest European research institutes on microelectronics. Mapper Lithography, a Delft University spin-off is developing a massively parallel ebeam writing system for future electronic circuit fabrication. On the other hand, UNITN, INL and the IMEC photonics research group are part of the world leading research groups on optics and photonics.


Ultra-compact optical router

IMEC coordinates the project and will design ultra-compact SOI waveguide circuits for routing and demultiplexing. IMEC will also contribute to the fabrication of the μsources and their integration with the waveguides. **ST Microelectronics** is investigating the viability of optical networks-on-chip and will design the required CMOS-circuits. **CEA-LETI** will develop the integration process and fabricate the photonic layer in a standard CMOS pilot line, including the III-V based microsources. **INL** is involved in the design and fabrication of the microsource arrays, will contribute to the optoNoC system studies and will be responsible for the design of the optical routers. **UNITN** will design innovative optical WDM circuits based on coupled ring resonators. **MAPPER** will be responsible for the system studies related to the terabit optical link.

Project Fact Sheet

Start Date: 01/01/2008 End Date: 31/12/2010
Project Duration: 36 Months
Project cost: 3.2k€ Funding: 2.3k€

Project coordinator & info:
Dries Van Thourhout - IMEC
dries.vanthourhout@imec.be
http://wadimos.intec.UGent.be

Partners

IMEC
- *Photonics Research Group, Ghent University, Ghent (B)*

http://www.photonics.intec.ugent.be

ST Microelectronics
- *OCCS group, Catania (It)*

http://www.st.com

CEA – LETI
- *Silicon photonics group, Grenoble (F)*

http://www-leti.cea.fr/

INL – Lyon Institute of Nanotechnology
- *Ecole Centrale de Lyon, Lyon (F)*
- *LPM group at INSA de Lyon, Lyon (F)*

http://inl.cnrs.fr/

UNITN - Trento University
- *Silicon photonics group, Trento (It)*

http://www.science.unitn.it/~semicon/

MAPPER Lithography
- *Maskless Lithography, Delft (NL)*

http://www.mapperlithography.com/