WADIMOS

Wavelength Division Multiplexed

Photonic Layer on CMOS

Collaborative Project

ICT – Information and Communication Technologies

FINAL PUBLISHABLE SUMMARY REPORT

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Project Coordinator : Dries Van Thourhout

Project Coordinator Organisation: IMEC

Grant Agreement: 216405

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EXECUTIVE SUMMARY

WADIMOS - WAVELENGTH DIVISION MULTIPLEXED PHOTONIC LAYER ON CMOS

The enormous computing power of multi-processor systems and manufacturing tools now on the drawing table will require data transfer rates of over 100Terabit/s. These data rates may be needed on-chip, e.g. in multicore processors, which are expected to need total on-chip data rates of up to 100TB/s by 2015-2020, or off-chip, e.g. in short distance data interconnects, requiring up to 100TB/s over a 10m to 100m long distance. The only viable technology for transmitting this level of information is using optical interconnects. Besides a huge data rate, optical interconnects also allow for additional flexibility through the use of wavelength division multiplexing. This additional flexibility may be employed for more intelligent interconnect systems, such as the optical network-on-chip system also investigated in this project.

In WADIMOS we have built a complex photonic interconnect layer incorporating multi-channel microsources, microdetectors and different advanced wavelength routing functions directly integrated with electronic driver circuits and demonstrate the application of such electro-photonic ICs in two representative applications:

- *Optical Network on Chip for ST Microelectronics multi-processor chips*. Inter-processor communication rates will soon reach an aggregated bandwidth of several hundred GHz. Several new electrical interconnect architectures are currently under investigation but despite these efforts still the International Technology Roadmap for Semiconductors predicts that interconnects will become the bottleneck of integrated systems-on-chip. Therefore, WADIMOS works on the realization of an optical NoC. The photonic layer will include complex wavelength division multiplexing functionality both for increasing the data rate and for increasing the routing flexibility since there is a broad consensus that this is the only approach really bringing added value to the network-on-chip.
- *Terabit optical datalink for MAPPER.* Mapper lithography is a semiconductor equipment company focusing on the development and manufacturing of a new and highly competitive maskless lithography machine using thousands of electron beams for writing the desired patterns. The electron beams are controlled by shutters in a beam blanker ship, which are controlled by an optical signal. This requires a data-rate of over 100TB/s between the subfab, where the patterns are generated, and the actual lithography equipment. At this moment, the data required to steer the individual electron beams is brought to the chip using thousands of optical fibers, each carrying an individual channel. We will investigate if optical wavelength multiplexing can be used to decrease the number of optical fibers required

Through several demonstrators we demonstrated the both the basic building blocks required for these applications and the possibility for integrating these building blocks. We also carried out higher level system studies. The project has resulted in 7 patent applications and over 30 peer-reviewed scientific publications. The results have been presented at the most important scientific conferences but also to a wider public, including industrial decision takers and the general public.

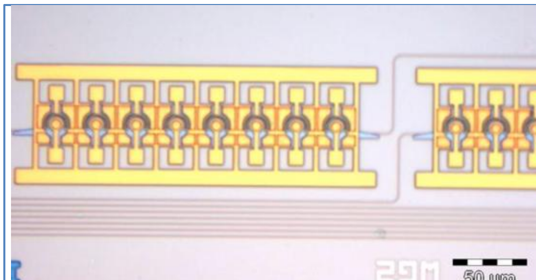
PROJECT CONTEXT AND OBJECTIVES

BACKGROUND

The enormous computing power of multi-processor systems and manufacturing tools now on the drawing table will require data transfer rates of over 100Terabit/s. These data rates may be needed on-chip, e.g. in multicore processors, which are expected to need total on-chip data rates of up to 100TB/s by 2015-2020, or off-chip, e.g. in short distance data interconnects, requiring up to 100TB/s over a 10m to 100m long distance. The only viable technology for transmitting this level of information is using optical interconnects. Besides a huge data rate, optical interconnects also allow for additional flexibility through the use of wavelength division multiplexing. This additional flexibility may be employed for more intelligent interconnect systems, such as the optical network-on-chip system also investigated in this project.

OBJECTIVE

The objective of WADIMOS was to build a complex photonic interconnect layer incorporating multi-channel microsources, microdetectors and different advanced wavelength routing functions directly integrated with electronic driver circuits and demonstrate the application of such electro-photonic ICs in two representative applications:



8-channel multi-wavelength source based on microdisk lasers (with built-in tuning), processed on 200mm CMOS line

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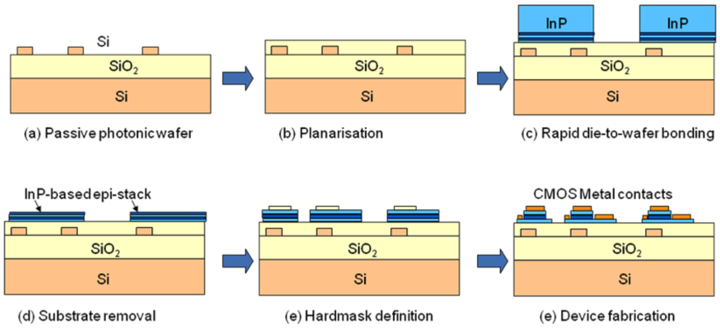
TECHNOLOGY PLATFORM

At the start of the the project a technology platform, which can fulfill the requirements of the applications described above, did not exist and until recently it also did not seem realistic to believe this level of photonic circuit integration would even be possible. However, the emergence of the new research domain that is now commonly called “Silicon Photonics” has completely changed this picture. The high refractive index of silicon in the near infrared allows for the fabrication of very compact photonic circuits. Moreover, these circuits can be fabricated using the advanced and very reliable processing tools also used for the fabrication of electronic circuits. In recent years, the different basic functions necessary for realizing complex photonic ICs were all demonstrated – among others by the



partners of this consortium and we believe this technology now has reached the level whereby these individual functions can be combined into much more complex circuits and directed towards specific applications, such as on-chip optical networks and terabit optical links.

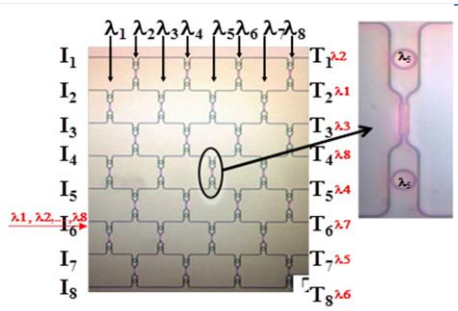
The basic technology was developed in the context of the FP6 project PICMOS. It is based on an optical layer consisting of silicon nanophotonic waveguides integrated with III-V micro-optoelectronic components. A waferscale compatible heterogeneous integration approach based on a rapid die-to-wafer bonding process was developed. The aim of WADIMOS was to extend this technology platform considerably:

- In PICMOS only single point-to-point links were demonstrated. Within WADIMOS, we aimed to demonstrate complex wavelength routing based functionality.
- In PICMOS, only part of the process was carried out in a CMOS pilot line. Within WADIMOS, we aimed to develop the processes for fully processing the III-V optoelectronic components in a CMOS-pilot line
- Improved optoelectronic devices needed to be developed, including:
    - Faster and lower power consumption micro-sources
    - Detectors integrated in the same epitaxial layer as the micro-sources
    - Complex passive circuitry, including optical router and novel "scissor" devices
- In WADIMOS, two practical applications – optical network on-chip and terabit link for massive parallel ebeam writer – are studied in detail and functional demonstrators were targeted.

PROJECT TEAM

The project included partners from industry (STM, MAPPER) as well as major research institutes and universities (IMEC, CEA-LETI, INL, UNITN). Both partners with a strong background in electronics as

partners with an outstanding track record in photonics are part of the consortium. ST Microelectronics is one of the world leading suppliers of electronic IC's while IMEC and CEA-LETI are the largest European research institutes on microelectronics. Mapper Lithography, a Delft University spin-off is developing a massively parallel ebeam writing system for future electronic circuit fabrication. On the other hand, UNITN, INL and the IMEC photonics research group are part of the world's leading research groups on optics and photonics.

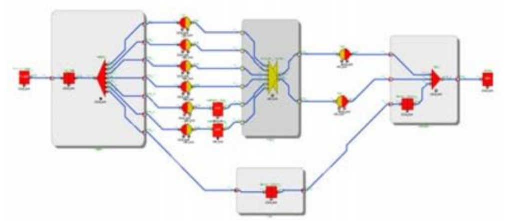


8x8 wavelength router based on ring resonators

IMEC coordinated the project and designed ultra-compact SOI waveguide circuits for routing and demultiplexing. IMEC also contributed to the fabrication of the μsources and their integration with the waveguides. **ST Microelectronics** investigated the viability of optical networks-on-chip and designed the required CMOS-circuits. **CEA-LETI** developed the integration process and fabricated the photonic layer in a standard CMOS pilot line, including the III-V based microsources. **INL** was involved in the design and fabrication of the microsource arrays, contributed to the optoNoC system studies and was responsible for the design of the optical routers. **UNITN** designed innovative optical WDM circuits based on coupled ring resonators. **MAPPER** was responsible for the system studies related to the terabit optical link.

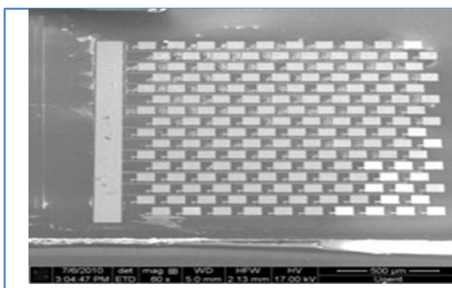
MAIN TECHNICAL PROJECT RESULTS

The project was divided in 6 work packages. Two of these (WP1 & 2) where dedicated to the system analysis of the applications under study. Three work packages were devoted to the different subcomponents: electronics (WP3), passive optical circuitry (WP4) and active optical circuitry (WP5). The final work package was devoted to the integration of all components (WP6). Below we describe the main results of each subtask.



Integration of optical router in ST OCCS GenKit

In WP1, ST and INL developed a system C model for the electronic and optical parts of the demonstrator respectively, relying on the OCCS Genkit, an ST internal tool and then integrated these. The proposed models have been integrated successfully inside an industrial development environment (ST OCCS GenKit) using an industrial standard (VSTNoC) protocol. Such an environment allows to define a system and its interconnect placing and connecting the ONoC, configuring it according to the specific application, simulating and characterizing the whole system (and in particular the interconnect) in terms of performance metrics (latency, throughput). A demonstrator mapped on a typical application with 6 initatior IP blocks (e.g. computing blocks) and 2 target IP blocks (e.g. memory blocks) with full bi-directional links between these blocks was implemented in this environment and evaluated.

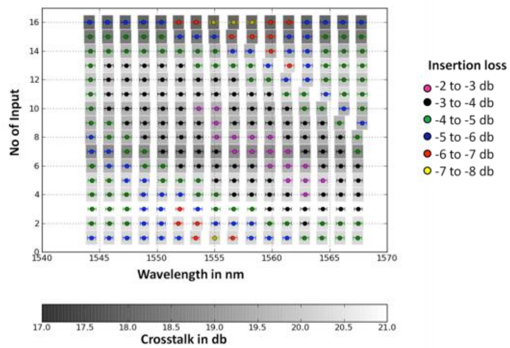


160-channel (20x8) parallel detector module for MAPPER datalink

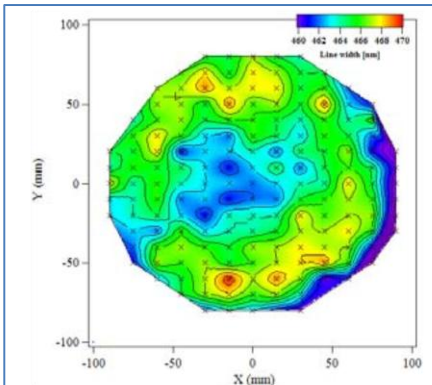
The system study for the MAPPER application (WP2) was focused on the possibility to integrate wavelength multiplexing functionality directly on the beam blanker chip. This requires integrating hundreds optical demultiplexers on the beam blanker chip, which has a size of only a few cm^2. Using currently commercially available devices this would be completely out of the question. And although the ultracompact silicon photonic circuits investigated in this project allow reducing the size of the optical demultiplexer by several orders of magnitude, the requirements imposed by the application remain challenging. In a first system study at the beginning of the project we concluded that with current state-of-the technology a demultiplexing rate of 16 should be achievable. Based on this study we defined the demonstrators to be realized in the project. In a follow-up system study at the end of the project MAPPER investigated in more detail the practical implementation of a traditional optical access system while imec studied the scalability of the WDM option. We proposed a new dense multiplexer design allowing for 64-512 channels with a limited sensitivity to process variations.

In WP3, we are developing the **CMOS circuits** needed to drive the ONoC demonstrator (ST 65nm process). Starting from the global CMOS chip architecture and definition we carried out the front-end design and simulation of both the analog and digital components. The analog part includes the laser and receiver drivers and is running up to 4GHz. The digital part includes both the components needed for the actual ONoC (serializers, buffers …) and the components needed for testing the circuits in different configurations. A dedicated 4GHz PLL (phase locked loop) to clock the analog parts was designed and validated. VHDL models were developed for the analog drivers and the optoelectronic components and integrated with the digital models. In this way the top level operation of the whole chip could be simulated. These results where then used as the entry point for the back-end flow, leading to the CMOS chip layout after place and route process. Functional equivalence between the layout and the front-end netlist has been proven through the LVS (Layout Versus Schematic) tool of the physical design platform. CMOS chip layout timing has been verified through the timing analyzer of the physical design platform. The CMOS chip GDS-II data base has then been delivered to CMP for manufacturing. This work resulted in 6 patent applications.

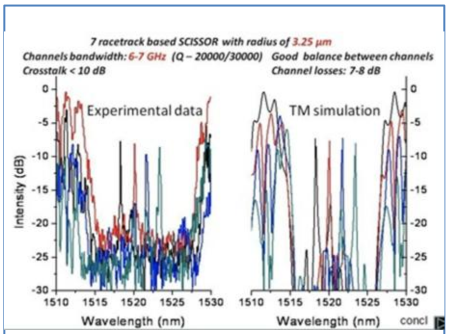
In WP4 we focused on the passive devices needed for the demonstrators, their scalability and their manufacturability. We investigated both ring resonator based devices and AWG-based devices. Ring resonator based routers are in principle more compact and should exhibit a lower fundamental loss but are more sensitive to process variations. In the project INL designed and tested optical λ-routers with up to 8-channels. A new approach to reduce the loss of the unavoidable waveguide crossings was developed – using MMI-splitters. Full transmission between every input and every output port was measured. The imbalance between the 8 channels was lower than 2 dB. In general the crosstalk was better than -10dB. The total footprint of the device is about 240 x 360 µm². AWG-based devices are larger but much more tolerant to fabrication issues. IMEC designed and characterized large channel count routers (16x16channels) and demultiplexers (1x32 channels). These devices show record low losses and acceptable crosstalk levels (-18dB). We also demonstrated flat-passband devices, which are more tolerant to wavelength shifts. The main remaining challenge for all these devices lies in precisely characterizing the group index, for correcting the channel spacing to the desired grid. In parallel, UNITN investigated possible applications of a two new types of optical routers, based on the SCISSOR concept (Side coupled sequences of resonators). Depending on the network they can be arranged to provide band or narrow channel routing. The overall advantage for both the proposed schemes over more standard single ring architectures is mainly on the coherent feedback provided by the ring sequences which allows to realize device which show larger insensitivity to fabrication errors. This turns out to be critical for complex optical networks where many routing/switching nodes are required. Finally we investigated in detail the fabrication uniformity of our processes over a single die, over a full wafer and from wafer to wafer. Due to the high index contrast, the devices are extremely sensitive to small variations in e.g. the linewidth or thickness of the waveguides. As a consequence, although reaching a manufacturing variation of less then 0.1nm on small range, and less then 3nm over a wafer – much better than what is typically required for an electronics process – we still see the influence of these variations in the optical measurements. The origins of these variations were thoroughly studied and improvements in the process were implemented. We made a proposal for uniformity improvement based on exposure dose compensation and fabricated integrated micro-heaters to allow tuning or trimming of wavelength selective circuits.

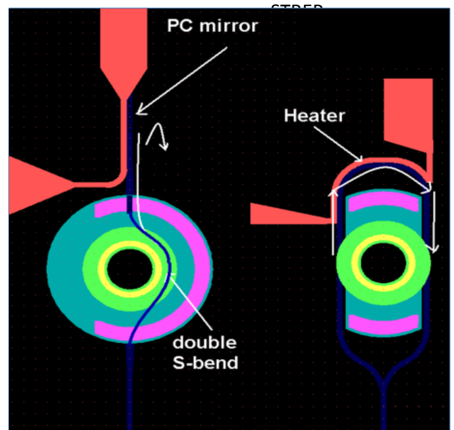


Characterisation results of 16 x 16 AWG based wavelength router



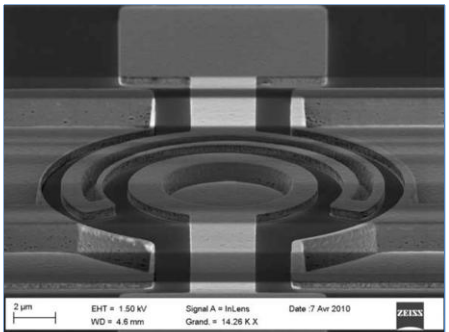
Uniformity of etch processes over 200mm wafer





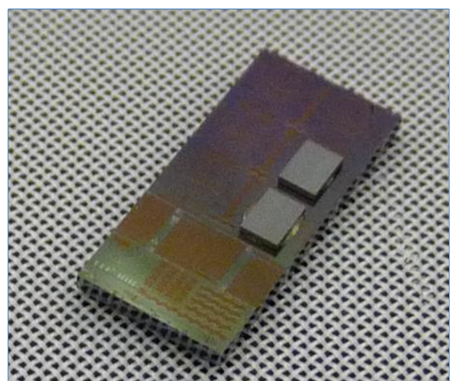
Layout of novel microdisk sources with external cavity controlling wavelength and directionality

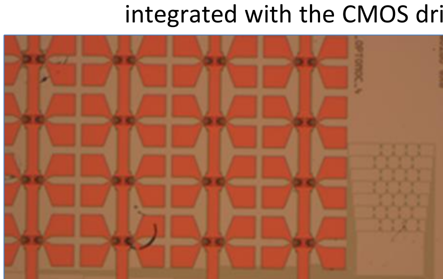
In WP5 the individual active devices where optimized and characterized. We demonstrated devices with substantially improved output power (under CW operating conditions) and lower threshold current, fabricated on small samples. This was made possible by an improved epitaxial layer design and growth, improved etching and better heat sinking. We reached the WADIMOS target of a 150µA threshold current and showed a small signal modulation bandwidth of 6GHz, compatible with 9GBit/s data transmission. The results of these initial experiments where then transferred to the 200mm processing line and we demonstrated for the first time operational III-V microdisk devices fully processed in a CMOS-compatible line, on a 200mm wafer. Using a specifically designed epitaxial stack, we managed to integrate for the first time also detectors with the microsources, allowing for a full optical link. The detectors had a responsivity better than 0.7A/W and bandwidth better than 10GHz. We also proposed and demonstrated several innovative approaches for controlling and tuning the output wavelength of the microdisk lasers. The simplest approach, developed by imec, consists of integrating a heater in the same III-V stack. This does not require additional processing and high tuning efficiency was reached. INL proposed two advanced cavity concepts, which allow tuning the wavelength through phase modulation of an external cavity. These approaches have the advantage that they also fix the lasing direction and suppress nearby azimuthal modes, improving the side-mode-suppression ratio.



Microdisk laser with CMOS compatible top-contact

WP6 was devoted to the **integration process** and coordination of the **demonstrator** fabrication. One of the first results was the definition of the detailed process sequence needed to realize the full optical layer with detectors, waveguides, tunable filters and tunable sources. This process was then used to fabricate the different demonstrators. For the mapper demonstrator we built the different subcomponents of a parallel datalink. We showed a WDM detector module with 160 channels (20 x 8) and different wafer-scale approaches for integrating the optical layer with CMOS-circuitry. The optical network demonstrator consisted of two parts: an 8 x 8 network, consisting of 8 8-channel transceivers connected through passive 8x8 optical routers, and a 2 x 2 network integrated with the CMOS driver circuitry developed in WP3. The full integration process could be completed and as already discussed above all blocks were demonstrated separately. Unfortunately however, the yield of the overall process was still too low to get the full demonstrator to work. As a consequence we could not demonstrate the fully integrate module. Further investment in dedicated equipment for this integration process seems to be required.


Optical ONoC integrated with CMOS driver circuitry


Wavelength router (right) integrated with optical microsources and detectors to form an 8x8 optical network

The project has resulted in 7 patent applications and over 30 peer-reviewed scientific publications. The results have been presented at the most important scientific conferences but also to a wider public, including industrial decision takers and the general public.

IMPACT AND DISSEMINATION

The project has resulted in 7 patent applications and over 30 peer-reviewed scientific publications. The results have been presented at the most important scientific conferences but also to a wider public, including industrial decision takers and the general public. Some of the results, e.g. on the passive optical circuits, are already used by the project partners in their commercial or semi-commercial offerings, e.g. through the shared wafer service ePIXfab run by imec and CEA-LETI. Other results, such as those on the microdisk lasers clearly need follow up research and will be the subject of further collaborations and projects.

Below we include a list of the journal papers published over the course of the project. These provide all necessary background information on the technical results.

#	Authors	Title	Reference	Lead Partner	Year
1	P. Bettotti,* M. Mancinelli, R. Guider, M. Masi, M. Rao Vanacharla, and L. Pavesi	Robust design of an optical router based on a tapered side-coupled integrated spaced sequence of optical resonators	April 15, 2011 / Vol. 36, No. 8 / OPTICS LETTERS	UNITN	11
2	Mattia Mancinelli, Romain Guider, Marco Masi, Paolo Bettotti, Manga Rao Vanacharla, Jean-Marc Fedeli, and Lorenzo Pavesi	Optical characterization of a SCISSOR device	4 July 2011 / Vol. 19, No. 14 / OPTICS EXPRESS 13664	UNITN	11
3	Mattia Mancinelli, Romain Guider, Paolo Bettotti, Marco, Masi Manga, Rao Vanacharla, Jean-Marc Fedeli, Dries Van Thourhout, Lorenzo Pavesi	Optical characterization of silicon-on-insulator-based single and coupled racetrack resonators	Journal of Nanophotonics, 051705-1 , Vol. 5, 2011	UNITN	11
4	Marco Masi, Mattia Mancinelli, Alberto Battarelli, Romain Guider, Manga Rao Vanacharla, Paolo Bettotti, Jean-Marc Fedeli, and Lorenzo Pavesi	A Silicon Photonic Interferometric Router Device Based on SCISSOR Concept	JOURNAL OF LIGHTWAVE TECHNOLOGY, VOL. 29, NO. 18, SEPTEMBER 15, 2011	UNITN	11
5	M. Mancinelli,* R. Guider, P. Bettotti, M. Masi, M. R. Vanacharla, and L. Pavesi	Coupled-resonator-induced-transparency concept for wavelength routing applications	20 June 2011 / Vol. 19, No. 13 / OPTICS EXPRESS 12227	UNITN	11
6	F. Mandorlo, P. Rojo Romeo, N. Olivier, L. Ferrier, R. Orobtchouk, X. Letartre, J-M. Fedeli, P. Viktorovitch	Controlled multi-wavelength emission in full CMOS compatible microdisk LASERs for on chip interconnexions	JLT (submitted)	CNRS	11

7	F. Mandorlo, P. Rojo Romeo, J-M. Fedeli, H. MD Sohrab, R. Orobtchouk	Mode Density Reduction and Coupling in Microdisk LASERs Processed on a 200 mm CMOS Pilot Line	PTL (accepted)	CNRS	11
8	S. Selvaraja, W. Bogaerts, D. Van Thourhout, M. Schaekers	Thermal trimming and tuning of hydrogenated amorphous silicon nano-photonic devices	Applied Physics Letters, 97 (7), (2010)	IMEC	10
9	L. Liu, T. Spuesens, G. Roelkens, D. Van Thourhout, P. Regreny, P. Rojo-Romeo	A thermally tunable microdisk laser built on a III-V/Silicon-on-insulator heterogeneous integration platform	Photonics Technology Letters, 22, p.1270 (2010)	IMEC	10
10	M. Masi, R. Orobtchouk, G. F. Fan, L. Pavesi	Towards a Realistic Modelling of Ultra-Compact Racetrack Resonators	Journ. of Light. Techn., Vol. 28, pp. 3233-3242, 2010	UNITN	10
11	F. Mandorlo, P. Rojo-Romeo, X. Letartre, R. Orobtchouk and P. Viktorovitch	Compact modulated and tunable microdisk laser using vertical coupling and a feedback loop	Opt. Express, Vol.18, pp. 19612-19625, 2010	CNRS	10
12	D. Van Thourhout, T. Spuesens, S. Selvaraja, L. Liu, G. Roelkens, R. Kumar, G. Morthier, Rojo-Romeo, Pedro, Mandorlo, Fabien, Raz, Oded, Kopp, Christophe, Grenouillet, Laurent	Nanophotonic Devices for Optical Interconnect	IEEE JSTQE (invited), 16(5), p.1363-1375 (2010)(invited)	IMEC	10
13	L. Liu, R. Kumar, K. Huybrechts, T. Spuesens, G. Roelkens, E.-J. Geluk, T. de Vries, P. Regreny, D. Van Thourhout, R. Baets, G. Morthier	An ultra-small, low-power, all-optical flip-flop memory on a silicon chip	Nature Photonics, 4(3), p.182-187 (2010)	IMEC	10
14	L. Liu, G. Roelkens, J. Van Campenhout, J. Brouckaert, D. Van Thourhout, R. Baets	III-V/silicon-on-insulator nanophotonic cavities for optical network-on-chip	Journal of Nanoscience and Nanotechnology (invited), 10, p.1461-1472 (2010)	IMEC	10
15	G. Roelkens, L. Liu, D. Liang, R. Jones, A. Fang, B. Koch, J. Bowers	III-V/silicon photonics for on-chip and inter-chip optical interconnects	Laser & Photonics reviews (invited), p.DOI: 10.1002/lpor.200900033 (2010)	IMEC	10
16	W. Bogaerts, S. Selvaraja, P. Dumon, J. Brouckaert, K. De Vos, D. Van Thourhout, R. Baets	Silicon-on-Insulator Spectral Filters Fabricated with CMOS Technology	(invited) publication in J. Sel. Top. Quantum Electron.,	IMEC	10
17	Shankar Kumar Selvaraja, Patrick Jaenen, Wim Bogaerts,Dries Van Thourhout,	Achieving sub-nanometer linewidth uniformity in silicon nano-photonic devices using	Journal of Selected Topics in Quantum Electronics : Silicon photonics special issue (Jan	IMEC	10

	Pieter Dumon, Roel Baets,	CMOS fabrication technology	2010)		
18	Shankar Kumar Selvaraja, Patrick Jaenen, Wim Bogaerts,Dries Van Thourhout, Pieter Dumon, Roel Baets,	Fabrication of Photonic Wire and Crystal Circuits in Silicon-on-Insulator Using193-nm Optical Lithography	Journal of Lightwave Technology, 27(18), p.4076-4083 (2009)	IMEC	9
19	F. Mandorlo, P. Rojo Romeo, X. Letartre, P. Viktorovitch	A simple perturbative analysis for fast design of an electrically pumped micro-disk laser	Optics Express, Vol. 17, Issue 1, pp. 70-79 doi:10.1364/OE.17.000070	CNRS	9
20	Z. Gaburro	Photonic energy lifters and event horizons with time-dependent microcavities	Journal of nanophotonics	UNITN	9
21	L. Liu, J. Van Campenhout, G. Roelkens, Richard A. Soref, D. Van Thourhout, Pedro Rojo-Romeo, Philippe Regreny, Christian Seassal, Jean-Marc Fedeli, R. Baets	Carrier-injection-based electro-optic modulator on silicon-on-insulator with a heterogeneously integrated III-V microdisk cavity	Optics Letters, 33(21), p.2518 (2008	IMEC	8
22	J. Van Campenhout, L. Liu, Pedro Rojo Romeo, D. Van Thourhout, Christian Seassal, Philippe Regreny, Lea Di Cioccio, Jean-Marc Fedeli, R. Baets	A Compact SOI-Integrated Multiwavelength Laser Source Based on Cascaded InP Microdisks	IEEE PHOTONICS TECHNOLOGY LETTERS, 20(16), p.1345-1347 (2008)	IMEC	8
23	Liu Liu, Joris Van Campenhout, Günther Roelkens, Dries Van Thourhout, Pedro Rojo Romeo, Philippe Regreny, Christian Seassal, Jean-Marc Fedeli, Roel Baets	Ultra-low-power all-optical wavelength conversion in a silicon-on-insulator waveguide based on a heterogeneously integrated III-V micro-disk laser	Applied Physics Letters, 93(6), p.061107 (2008)	IMEC	8

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Further information on the project can be found on the website: www.wadimos.eu

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