FABULOUS NEWSLETTER

FDMA Access By Using Low-cost Optical Network Units in Silicon photonics

Number 3

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European Commission

STREP Contract 318704

Objective ICT-2011-3.5: Core and disruptive photonic technologies

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FABULOUS at a glance:

Start date: 1st October 2012
Duration: 36months
Total project cost: 4,2M€
EU financing: 2,9M€

Welcome to the third issue of the FABULOUS newsletter

The FABULOUS project is entering its "full maturity stage", since we are now in the middle of the third and last year of the project. Most of the activities for Workpackage WP-SYST on system level experiments are coming close to their conclusion, while the work in WP-COMP on the realization optoelectronic components is now starting to give its first results. I thus would like to summarize in this Introduction to our Newsletter our main achievements so far.

For what concerns system level activities, we run an extensive set of laboratory experiments using discrete off-the-shelf optoelectronic components. Among our best results, we assemble over a realistic PON (37km of metropolitan installed fiber, up to 31 dB of possible ODN loss) five complete ONUs transmitting in upstream according to the FABULOUS architecture, and we demonstrate on this setup five concurrent FDMA streams running each ONU at 1 Gbps net data traffic (carried over a 16-QAM modulation). By setting the frequency allocation to a worst-case situation, we emulated the equivalent of 32 ONUs. Similar results were also obtained for the downstream transmission so that, in conclusion, we demonstrated the feasibility of 32x1 Gbps transmission per wavelength over up to 31 dB ODN loss. In addition, in order to maximize the exploitation potential, some other application that PON for FTTH are being investigated, as reported in page 3 of this issue.

For what concerns the components-related activities, we have now in our "FABULOUS portfolio" the realization of a III-V SOA integrated on a silicon photonic platform, that was also fully packaged and used in some system demonstration, showing good physical layer performances. The first realization of the reflective Mach-Zehender modulator on Silicon Photonics have now reach the lab, and are today in the test phase. Several prototyping run came out from the fab, and were integrated with the properly designed driver with distributed electrodes and then packaged. Some delay is occurring with respect to the original workplan, to that a project extension might be possible, however the preliminary results on the building blocks allow us to be optimistic on the results that the fully integrated component will achive in this generation, as well as in the next generation that currently is in fab.

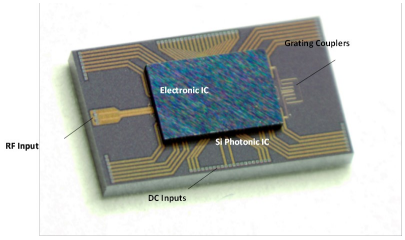
We have also carried out a techno-economic study on the cost and power consumption of a full "FABULOUS" ONU: the photonic chip cost has been evaluated around 7US$/unit and packaging 40US$/unit in 1M units volumes. The RF driver chip is evaluated to cost 2US$/unit. A TEC is necessary, with added cost estimated at 15US$. The electrical front end cost can be inferred from the UWB radio transceiver cost as the one used in the OLT cost assessment, that is 20US$ today and so 14US$ in the long term. This leads to a total ONU cost about 78US$ in the long term and in 1M units per year volumes. The resulting power consumption was estimated to be just under 6W.

In the next newsletter, we hope to give you the first actual demonstration and measurement on this full ONU realization.

Roberto Gaudino
Politecnico di Torino

Silvio Abrate
ISMB

First mock-up assembly of integrated R-MZM



Flip-chip stacking of the driver die on the Photonic Circuit

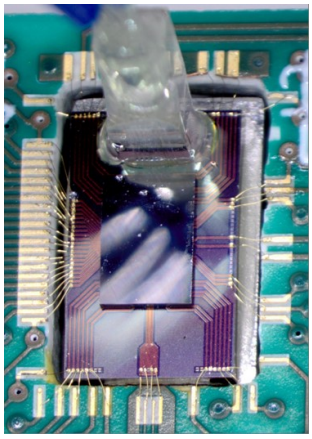
One of the main goals of the FABULOUS project is to demonstrate the integration of the ONU circuit into a low-cost compact module, using Silicon Photonics and co-integration with the driver using copper micropillars. This has been made possible during the last quarter of 2014 by merging the know-how of ST in terms of *Electronic IC* (EIC) design & manufacturing, CEA-LETI for *Photonic Integrated Circuit* (PIC) design & manufacturing and crucially Tyndall National Institute for EIC on PIC flip-chip assembly, optical pig-tailing and testboard assembly.

The copper micropillar compatible driver uses the same 65nm CMOS technology as the standalone version that was presented in the previous newsletter. 50µm pitch micropillars have been grown in order to allow a flip-chip stacking of the die onto the Photonic Circuit. This includes related metallized pads referred to as *Under Bump Metallization* (UBM). Several couple of dies have been flip-chip assembled, allowing to assess the stacking process. The first mock-ups have been particularly useful in order to assess the thermal and the DC electrical behavior of the module.

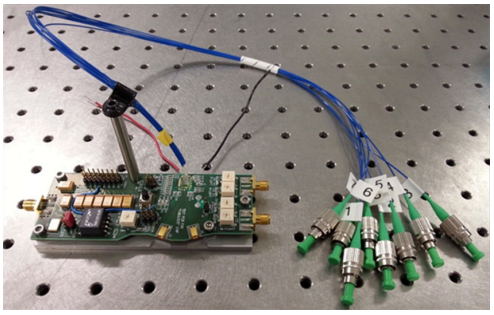
Other assemblies have been fully assembled in "Chip-On-Board" modules. This includes the design and fabrication of a dedicated board required to control the driver and the modulator biases in addition performing RF and system level tests of the whole device. At least, one 8-fiber ribbon is actively aligned and epoxy fixed onto the module in order to connect the device to the optical network. One of the fibers is used for optical I/O, whereas some other are used to facilitate alignment or for optical diagnostics.

Two modules have been fully packaged and are now used to prepare the system level test and also to optimize the PIC fabrication process of the next generation.

Stéphane Bernabé
CEA-Leti



Detail view of the first mock-up (with the fiber ribbon fixed on the circuit)



Full module assembly including test board and fiber pigtail

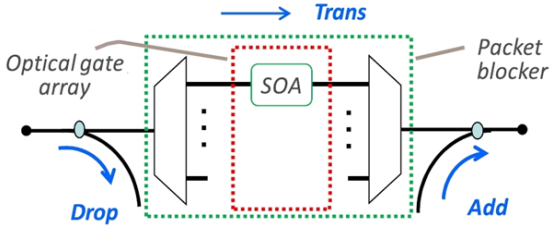
Light amplification on silicon

There is currently a strong trend in the communication market towards using silicon photonics in order to make compact, cost-effective, and power-efficient optical network equipment. And since there is no silicon-based light source to feed the silicon photonics circuits, a lot of effort is currently made to build hybrid lasers, in particular lasers made from III-V semiconductor materials, such as InP. These materials can amplify light, when a current runs through them, and when they are combined with silicon, an integrated light source can be achieved for silicon photonics.

The laser is an important component for photonic integrated circuits (PIC), but light amplification can be interesting in many other ways. The larger a PIC gets, the more important it becomes to compensate losses that arise from the propagation through waveguides and from the insertion into components such as filters, couplers, splitters, or modulators. In the FABULOUS project, we are working on an integrated reflective modulator ONU, which reaches a complexity that requires the use of integrated semiconductor optical amplifiers (SOA) as intermediate loss compensators. Another example of interest for light amplification is the use of an SOA as an optical gate in a packet switching node, such as the one show in the figure. When the SOA is turned on, a packet of information can go through, when it is turned off, the packet will be blocked. There are many other possible functions of optical amplifiers (remote modulator on colorless ONU, broadband light source, wavelength conversion, etc.), and we believe that with increasing maturity of silicon photonics, we will encounter more and more of them on a regular basis.

Peter Kaspar
III-V Lab

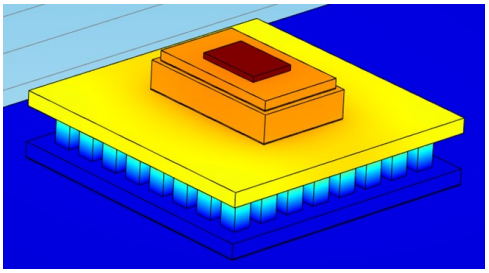
> **"The laser is an important component for photonic integrated circuits, but light amplification can be interesting in many other ways. "**



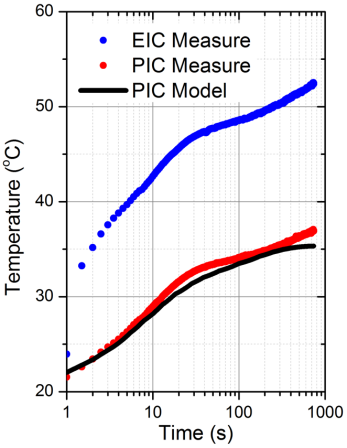
Use of SOA as optical gate

Thermal characterisation of the FABULOUS module

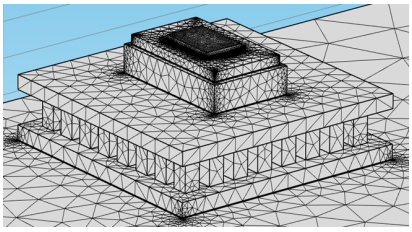
Tyndall is working to provide a comprehensive thermal characterisation of a the fully-packaged and assembled FABULOUS module. A good working knowledge of the thermal behaviour of the module is important, not only because the performance of certain photonic elements (like the micro-ring resonators and the semiconductor amplifier) are very temperature sensitive, but also because it helps us chose the appropriate thermal management solution,and dictates the overall power-budget of the device.



Heat spreading from the EIC, into the PIC, sinked below the Peltier-cooler.



Temperature of the uncooled PIC and EIC after power-up



Temperature of the uncooled PIC and EIC after power-up

By automatically measuring the temperature of the photonic integrated circuit (PIC) and the electronic-IC, over the course of several hours, and plotting the results on a logarithmic-scale, we gain an intuitive insight into how heat energy flows from the driver circuit, into the Si-PIC, through the Peltier-cooler, and into the Aluminium base-plate. The results of the temperature measurements are well reproduced by finite-element COMSOL simulations, based on a high-fidelity structural model of the module, allowing for further "virtual" optimisation of the module design.

Without cooling, the PIC temperature increases by less than 20C in the steady-state, while the electronic-IC increases by less than 30C. Such moderate temperature increases are easy to manage using a thermo-electric cooler (TEC). When temperature-controlled by the TEC, the measured Si-PIC temperature quickly stabilises to within a fraction of a degree at 20C, ensuring stable operation of all the photonic elements. Furthermore, after simulating a "power failure" condition in the module, our measurements show that the TEC re-stabilises the PIC temperature in less than 10s, demonstrating an excellent reboot time in the FABULOUS module.

Juns Su Lee, Lee Carroll
Tyndall National Institute, University College Cork

The vertical-PON scenario

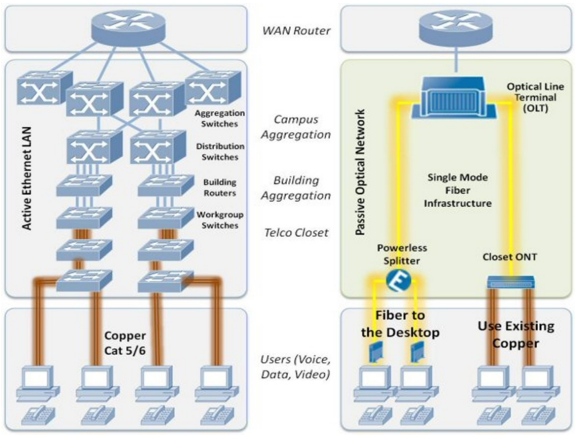
Although FABULOUS is conceived around the Passive Optical Network paradigm for optical access, the so-called Fiber-To-The-Home (FTTH), such paradigm is starting gaining attention for applications for local area networking (LAN) as well. In order then to maximize the exploitation potential of FABULOUS, it is reasonable to investigate whether our research is reasonable for this application scenario or not.

With respect to the PON scenario, the main differences reside in the optical part of the system: no optical amplifiers are to be used at the OLT side, the fiber link is definitely shorter (we considered 1 Km of fiber instead of a fiber testbed of 37 Km,) the fiber launch power has to be lower and we limited it to P_f=0 dBm. In addition, we think that a standard FEC with a threshold of $2.17 \cdot 10^{-3}$ is more suitable for a LAN scenario. Aiming at delivering 100 Mb/s per user, the 16-QAM modulation format that we adopted for the PON scenario at 1 Gb/s is not feasible for phase noise limitations, even with such a short fiber link, we then used QPSK modulation, yielding a per-channel bandwidth of 60.5 MHz (considering 10% of overhead for FEC and signaling), and then the modulator bandwidth limits the number of users to 128 (in order to stick with powers of 2, 256 would be the next step but not feasible). The total bandwidth requested to the modulator is well below 8 GHz, and we then believe that this lower requirement, with respect an high-performance PON scenario, makes LAN application a promising opportunity for the FABULOUS silicon-photonics ONU, still in its development phase.)

The experimental results achieved with such parameters have shown that the maximum achievable power budget for the LAN scenario is in the order of 31 dB, well above the 21 dB requested by the 1 : 128 optical power splitter; we then believe that this constitutes a potentially attractive application for the FABULOUS architecture and ONU.

Silvio Abrate
ISMB

"Vertical PON constitutes a potentially attractive application for the FABULOUS architecture and ONU"



The Vertical PON concept

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A flexible architecture, compatible with current infrastructures, and low cost components and network units based on silicon photonics: the keys for mass Fiber-To-The-Home deployment.

The FABULOUS Project has been conceived and is being carried out by a balanced mix of *universities, research centers, industries and operators*; such a consortium is very heterogeneous, in order to cover all the many different technological aspects required by the work-plan. In particular, two main different category of aspects can be identified in the project structure:

- **System aspects**, main duty of Istituto Superiore Mario Boella, Politecnico di Torino and France Telecom
- **Optoelectronic, silicon photonics and packaging aspects**, main duty of CEA-LETI, II-V Labs, University of Pavia, Tyndall National Institute, STMicroelectronics.

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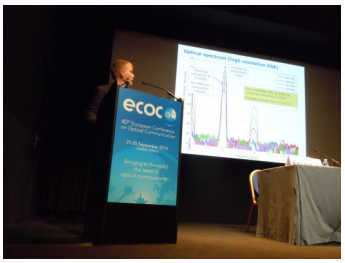

Oral presentation by Roberto Gaudino at ECOC 2014

EVENTS and DISSEMINATION

The partners of the FABULOUS consortium have been really active from the point of view of scientific dissemination. We count more that 20 peer-reviewed papers, and more are expected when the integrated component will be available.

Recently, ECOC conference held in Nice in September has been an important showcase for FABULOUS, with a few oral presentations and the presence of a booth, run by Orange, with the demonstration of the FABULOUS architecture with discrete components. Other important events that have seen the partecipation of the consortium are the International Conference on Group IV Photonics, OFC, EUCNC, ICTON and Fotonica.

In addition, papers have appeared on the issue of January 2015 on Photonics Technology Letters and the IEEE Journal of Lightwave Technology.

Where to see FABULOUS next? Invited presentations will be given at OFC 2015, held in March in Los Angeles, OECC 2015, held in Shangai in June, and ICTON 2015, held in Budapest in July. Moreover, regular papers are expected at the IEEE International Conference on Communications, that will be held in London in June, and Fotonica 2015, that will be held in Turin in May.

Wide dissemination is then expected for FABULOUS in 2015, the International Year of Light.

FABULOUS demonstration by Benoit Charbonnier at ECOC 2014