PROJECT PERIODIC REPORT

Grant Agreement number: 248613

Project acronym: DIAMOND

Project title: Diagnosis, Error Modelling and Correction for Reliable Systems Design

Funding Scheme: collaborative research project

Funding Scheme: Collaborative project

Date of latest version of Annex I against which the assessment will be made:

Periodic report: **1st** ☐ **2nd** ☐ **3rd** X **4th** ☐

Period covered: **from 01.01.2012 to 31.12.2012**

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Declaration by the scientific representative of the project coordinator

I, as scientific representative of the coordinator of this project and in line with the obligations as stated in Article II.2.3 of the Grant Agreement declare that:

- The attached periodic report represents an accurate description of the work carried out in this project for this reporting period;
- The project (tick as appropriate) [1]:
  - ☑ has fully achieved its objectives and technical goals for the period;
  - ☐ has achieved most of its objectives and technical goals for the period with relatively minor deviations.
  - ☐ has failed to achieve critical objectives and/or is not at all on schedule.
- The public website, if applicable
  - ☑ is up to date
  - ☐ is not up to date
- To my best knowledge, the financial statements which are being submitted as part of this report are in line with the actual work carried out and are consistent with the report on the resources used for the project (section 3.4) and if applicable with the certificate on financial statement.
- All beneficiaries, in particular non-profit public bodies, secondary and higher education establishments, research organisations and SMEs, have declared to have verified their legal status. Any changes have been reported under section 3.2.3 (Project Management) in accordance with Article II.3.f of the Grant Agreement.

Name of scientific representative of the Coordinator: Jaan Raik

Date: 15/ 02 / 2013

For most of the projects, the signature of this declaration could be done directly via the IT reporting to through an adapted IT mechanism and in that case, no signed paper form needs to be sent

[1] If either of these boxes below is ticked, the report should reflect these and any remedial actions taken.

1. Publishable summary

1.1 Project context and objectives

Increasing design costs are the main challenge facing the nanoelectronics community. Assuring the correctness of the design contributes to the major part of the problem. However, while diagnosis and correction of errors are more time-consuming compared to error detection, they have received far less attention, both, in terms of research works and industrial tools introduced.

Another, orthogonal threat to the development is the rapidly growing rate of soft-errors in the emerging nanometer technologies. According to roadmaps, soft-errors in sequential logic are becoming a more severe issue than in memories. However, the design community is not ready for this challenge because existing soft-error escape identification methods for sequential logic are inadequate.

The aim of DIAMOND was improving the productivity and reliability of semiconductor and electronic system design in Europe by providing a systematic methodology and an integrated environment for the diagnosis and correction of errors. DIAMOND developed:

- A unified, holistic diagnostic model for design and soft errors;

- Automated localisation and correction techniques based on the unified model, both pre- and post-silicon;

- Implementation of a reasoning framework for localisation and correction, encompassing word-level techniques, formal, semi-formal, and dynamic techniques;

- Integration of automated correction with the diagnosis methods.

DIAMOND reached beyond the state-of-the-art by proposing an integrated approach to localisation and correction of specification, implementation, and soft errors. In addition, it considered faults on all abstraction levels, from specification through implementation down to the silicon layout. Handling this full chain of levels allowed DIAMOND take advantage of hierarchical diagnosis and correction capabilities incorporating a wide range of error sources.

The partners of the project included Tallinn University of Technology (TUT), Linköping University (LIU), The University of Bremen (UNIB), Technical University of Graz (TUG), TransEDA (TEDA), Testonica Lab (TL), Ericsson and IBM Israel.

1.2 Description of work and results achieved during the project

The general picture of the DIAMOND project work flow is presented in Figure 1. As the starting point, requirements and end-user needs have been defined by the industrial partners of the project. Based on these requirements a holistic diagnostic model for design and soft errors has been developed and appropriate reasoning engines have been prepared. The core of DIAMOND is the design error diagnosis and correction and soft error analysis methods developed at the transaction and implementation levels, as well as post-silicon in situ diagnosis and repair methods. Finally, the project results have been evaluated on the benchmark designs constituting the DIAMOND platform. In the following, the results achieved during the project are summarised.

Requirement analysis and benchmarking
During the first project year we conducted a study of the requirements and expectations of the end-users. This study was based on the industrial partners' inputs. In addition, a number of individual diagnosis and repair benchmarks were made available within the consortium in order to allow evaluation of DIAMOND tools.

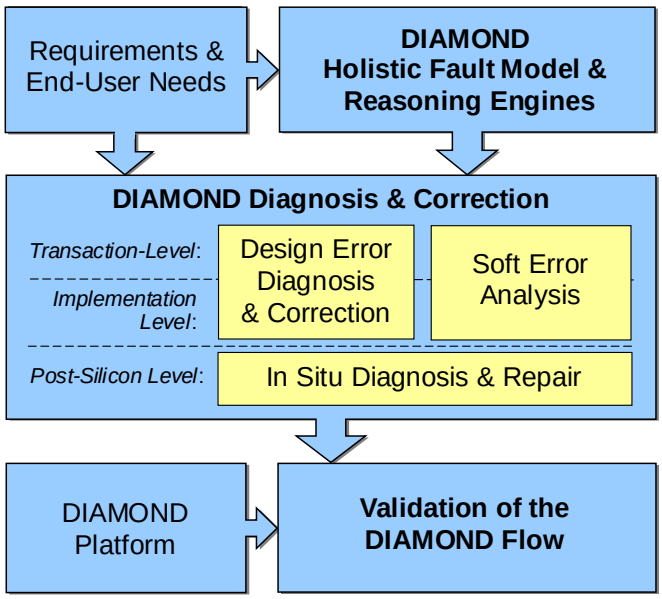

Figure 1. The DIAMOND Flow

Holistic diagnostic model

By the end of the second project year, the holistic diagnostic model, which can be considered the "backbone" of the DIAMOND infrastructure, has been developed. DIAMOND considers different application domains – diagnosis and correction – at different levels in the design flow – transaction, implementation and post-silicon. The aim of the diagnostic model is to integrate those different views as much as possible, to capture the individual requirements by the different applications. We devised use cases spanning all applications for the different abstraction levels considered within DIAMOND. From these use cases the requirements and the diagnostic model were derived.

Reasoning engines for diagnosis and correction

Formal, semi-formal, and dynamic reasoning engines are the core of the diagnosis, correction, and analysis approaches developed within DIAMOND. Different types of engines are required to trade reasoning power for resource requirements. Moreover, fine-tuning of the reasoning engines for particular types of applications is necessary to achieve the required efficiency and the expected quality of results.

Formal reasoning engines include an engine for debugging specifications using model-based diagnosis, engine for diagnostic test pattern generation, an engine particularly adopted for determining latency values for circuits (in order to identify for how many time cycles the computation of a sequential circuit may be influenced by erroneous values on certain signals), and tuning the formal reasoning engines for evaluating the vulnerability of latches with respect to soft errors.

Semi-formal reasoning engines contain a symbolic and concolic execution engine for localization and correction at the transaction level, a semiformal engine for latency analysis mentioned above and semiformal engines for the analysis of soft errors along with mechanisms to handle soft errors.

Dynamic engines are an approach to analyse very large systems based on simulation. Additionally, dynamic engines are applied to further utilise results returned from other, more powerful engines. The engines developed within DIAMOND include the simulation engine based on HLDDs, a dynamic engine for latency analysis which is complementary to the formal and semi-formal engines mentioned above, and more general frameworks for pre-silicon and post-silicon/in-situ diagnosis.

Diagnosis methods and tools

Various techniques for **error localisation and correction at the transaction-level** have been developed. This includes techniques to diagnose over-constrained formal specifications, to diagnose inconsistencies between hardware descriptions and their transaction-level specification, techniques

based on symbolic execution, and techniques using statistical design error ranking in combination with mutation-based correction. A new tool FoREnSiC implementing the transaction-level localisation and correction techniques has been released by the DIAMOND partners TUG, UNIB and TUT.

At the **implementation-level** (i.e. register-transfer and logic level), several methods and tools have been developed by UNIB, TUG, IBM, TEDA and TUT. These include a latency analysis tool for identifying the time a sequential circuit may be influenced by erroneous values, a model-based diagnosis tool, a dual model framework to increase the throughput of a soft errors injection framework by identifying error vanish time and a critical fault list generation to limit the number of soft errors to be simulated. In addition TUT has developed statistical design error localisation capabilities into an open source framework zamiaCAD. The tool is highly scalable and has been evaluated by IBM on large designs.

The **post-silicon and in situ diagnosis and correction** tools have been developed by Ericsson, LIU and TL. These include a method for efficient embedding of deterministic test data to enable flexibility in the type of commands that can be issued while keeping the memory requirements for storing deterministic test data low and the fault management approach containing techniques for error classification and for parallel scheduling of tests with synchronisation. In addition, a fault management architecture for on-line diagnosis has been developed.

Regarding the **tool integration** within DIAMOND, TEDA has focused on the integration of the toolsets and has engineered a new platform that allows TEDA to compete in the emerging cloud EDA market. Each toolset of partners in DIAMOND is configured and maintained on a dedicated virtual machine allowing for flavours of operating system and programming language. As a result of DIAMOND, several tools have been integrated into Assertain environment. TUT's APRICOT verification engine was integrated as a pilot project in December 2010. By the end of the project also FoREnSiC and zamiaCAD have been integrated to Assertain. The respective tools can be launched by the environment and debug reports are visualized in a uniform manner.

Dissemination

The web site for the DIAMOND, URL: http://fp7-diamond.eu, has been developed listing all the relevant information concerning the project. A promotional 2 minute video of DIAMOND has been produced and is accessible from the DIAMOND web site. In addition, a large number of press releases have been published worldwide, altogether in 10 different languages, including local TV, radio interviews and articles in items like EETimes, CNN, USA Today, Processor, IT Jungle, Design&Reuse, PR Newswire and several others. By the end of the project, 82 scientific papers related to the topics of DIAMOND have been published by the consortium.

The project was presented at several top-level European events including European Nanoelectronics Forum 2012, ACM/IEEE Design Automation and Test in Europe (DATE) 2010, 2011 and 2012, HiPEAC Computing Systems Week 2012 and European Test Symposium 2012. In addition, two dissemination workshops presenting the results of DIAMOND were held.

1.3 The final result achieved

The result of the project is a **scalable and robust environment for handling faults in semiconductor designs.** This development environment provides diagnostic information needed for the correction of faults, be they design faults, implementation faults, or soft errors. The diagnostic information is either at the source-level, the logic-level, or the gate-level, depending on the level of abstraction at which the design is provided. Such information may consist of the location of a fault or a soft error vulnerability. The environment also suggests measures for correction of the fault or vulnerability wherever possible, where the type of the correction is suitable to the level of abstraction in which it is needed. The environment significantly reduces the time spent on error analysis and design modification, hence increasing the designers' productivity.

1.4 Estimated impact and project exploitation

Electronics and information systems play an ever-increasing role in the worldwide economy, representing already today nearly 10% of Gross Domestic Product (GDP). The embedded systems technologies are deployed in all market sectors – automotive, aerospace, medical, environment, communications, entertainment, textiles, transport, logistics, printing and chemicals, food & drink, timber and materials, possessing therefore a tremendous economic potential for European companies and significant impact on the everyday life of European citizens.

The leading technology roadmap ITRS lists increasing design costs as the main threat to the growth of electronics development. Localisation and correction in ICs constitute 2/3 of the total time spent on verification, which in turn represents the main reason for the excessive costs. At the same time, due to entering the deep-submicron era (below 45nm), the semiconductor industry is faced with rapidly growing rates of soft errors.

DIAMOND predicted **50% reduction in time spent on fault localisation and correction**. The actual improvement provided by the project solutions has been estimated at two levels: transaction-level and implementation-level. At the transaction-level the FoREnSiC environment was applied, considered both formal and simulation-based cases. In formal design error correction, FoREnSiC's symbolic back-end was compared to a formal tool Sketch. The comparison showed that FoREnSiC offered a significant advantage in terms of better scalability. Hence much larger designs can be handled. In the field of simulation-based design error correction DIAMOND's mutation-based design error correction implemented within FoREnSiC was compared to a recent method based on the Tarantula software. The method developed within DIAMOND was able to increase the ratio of successful design error corrections for more than three times, from 16% to 50%. As a result the automated debug time was reduced by 67%, which is more than was initially predicted.

At the implementation level there is no reference tool to compare to. Hence, a case study on a real processor design ROBSY with 7 documented bug cases was carried out. The DIAMOND's automated fault localisation methods were integrated into the zamiaCAD system. In order to evaluate the improvement of debugging speed, zamiaCAD results were compared to the manual debug time provided in the bug reports. zamiaCAD was capable of locating all the 7 bugs with run times ranging from 2 to 12 minutes. The manual debug times were between 1 and 5 hours. Hence the speed-up measured on this case study was well above the 50% target.

In addition, DIAMOND predicted **25% reduction of soft-error simulation time** and **30% increase in the number of identified unprotected soft errors**. To that end, a method estimating robustness of design using interpolation-based model checking was developed in cooperation by IBM and UNIB. The results showed that, depending on the design, up to 60% of latches may be excluded from soft error simulation hence increasing the simulation speed by the same proportion. Also, a latch coverage engine which has been an enabler for automated identification of unprotected latches was developed in DIAMOND. Hence the time-consuming and error-prone work of validating unprotected latches has been replaced by an automated approach consuming only few seconds of run-time.

The two SMEs of DIAMOND, TEDA and TL, will bring DIAMOND innovations to market as new CAD tools. In addition, IBM and Ericsson are applying DIAMOND results in their development processes and university partners exploit the results in research and education. Two patents by IBM and a patent by TL have been filed related to DIAMOND project developments. The outcome of DIAMOND is expected to be applied not only by the consortium members but by a wider nanoelectronics community.