Publishable summary

Project context and objectives

Increasing design costs are the main challenge facing the nanoelectronics community. Assuring the correctness of the design contributes to the major part of the problem. However, while diagnosis and correction of errors are more time-consuming compared to error detection, they have received far less attention, both, in terms of research works and industrial tools introduced.

Another, orthogonal threat to the development is the rapidly growing rate of soft-errors in the emerging nanometer technologies. According to roadmaps, soft-errors in sequential logic are becoming a more severe issue than in memories. However, the design community is not ready for this challenge because existing soft-error escape identification methods for sequential logic are inadequate.

The aim of DIAMOND is improving the productivity and reliability of semiconductor and electronic system design in Europe by providing a systematic methodology and an integrated environment for the diagnosis and correction of errors. DIAMOND will develop:

- A unified, holistic diagnostic model for design and soft errors;

- Automated localisation and correction techniques based on the unified model, both pre-silicon and post-silicon;

- Implementation of a reasoning framework for localisation and correction, encompassing word-level techniques, formal, semi-formal, and dynamic techniques;

- Integration of automated correction with the diagnosis methods.

DIAMOND reaches beyond the state-of-the-art by proposing an integrated approach to localisation and correction of specification, implementation, and soft errors. In addition, it considers faults on all abstraction levels, from specification through implementation down to the silicon layout. Handling this full chain of levels allows DIAMOND to take advantage of hierarchical diagnosis and correction capabilities incorporating a wide range of error sources.

The partners of the project include Tallinn University of Technology (TUT), Linköping University (LIU), The University of Bremen (UNIB), Technical University of Graz (TUG), TransEDA (TEDA), Testonica Lab (TL), Ericsson and IBM Israel.

Description of work and results achieved by the 2nd year

The general picture of the DIAMOND project work flow is presented in Figure 1. As the starting point, requirements and end-user needs have been defined by the industrial partners of the project. Based on these requirements a holistic diagnostic model for design and soft errors have been developed and appropriate reasoning engines have been prepared. The core of DIAMOND is the design error diagnosis and correction and soft error analysis methods developed at the transaction and implementation levels, as well as post-silicon in situ diagnosis and repair methods. Finally, the project results will be evaluated on the benchmark designs constituting the DIAMOND platform. This evaluation will take place during the third year of the project. In the following, the results achieved by the second project year are summarised.

Requirement analysis and benchmarking

During the first project year we conducted a study of the requirements and expectations of the end-users. This study was based on the industrial partners' inputs. In addition, a number of individual

diagnosis and repair benchmarks were made available within the consortium in order to allow evaluation of DIAMOND tools. The industrial partners—IBM and Ericsson—chose benchmarks from their current activities. In addition the consortium selected 5 open source designs. Altogether, these benchmarks cover a wide range of designs and architectures, of sufficient size and complexity to provide challenges for diagnosis and repair of faults on different levels and the tools supporting it. During the second year the benchmark set was extended to include internationally recognized Siemens benchmarks in order to evaluate DIAMOND diagnosis and correction methods with respect to the state-of-the-art. In addition, Ericsson developed a new evaluation platform for in-situ diagnosis and repair tools.

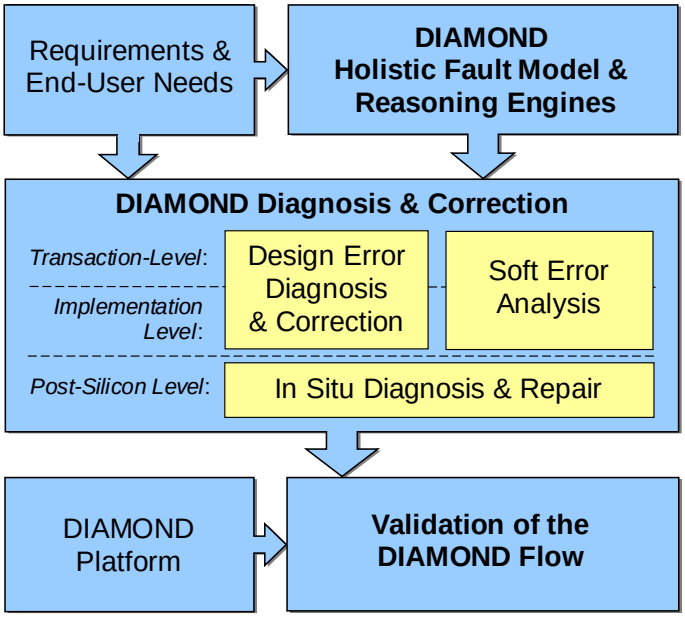

Figure 1. The DIAMOND Flow

Holistic diagnostic model

By the end of the second project year, the holistic diagnostic model, which can be considered the "backbone" of the DIAMOND infrastructure, has been developed. DIAMOND considers different application domains – diagnosis and correction – at different levels in the design flow – transaction, implementation and post-silicon. The aim of the diagnostic model is to integrate those different views as much as possible, to capture the individual requirements by the different applications. We devised use cases for the different abstraction levels considered within DIAMOND. For each abstraction level the use cases span all applications. From these use cases the requirements and the diagnostic model were derived.

Reasoning engines for diagnosis and correction

Formal, semi-formal, and dynamic reasoning engines are the core of the diagnosis, correction, and analysis approaches developed within DIAMOND. Different types of engines are required to trade reasoning power for resource requirements. Moreover, fine-tuning of the reasoning engines for particular types of applications is necessary to achieve the required efficiency and the expected quality of results.

Formal reasoning engines include an engine for debugging specifications using model-based diagnosis, engine for diagnostic test pattern generation, an engine particularly adopted for determining latency values for circuits (in order to identify for how many time cycles the

computation of a sequential circuit may be influenced by erroneous values on certain signals), and tuning the formal reasoning engines for evaluating the vulnerability of latches with respect to soft errors. The development of these engines was mainly driven by IBM, TUG, TUT, and UNIB.

Semi-formal reasoning engines contain a symbolic and concolic execution engine for localization and correction at the transaction level, a semiformal engine for latency analysis mentioned above and semiformal
engines for the analysis of soft errors along with mechanisms to handle soft errors. These engines were developed by IBM, TUG, TUT, and UNIB.

Dynamic engines are a powerful approach to analyze very large systems. Additionally, dynamic engines are applied to further utilize results returned from other, more powerful engines. The engines developed within DIAMOND include the simulation engine based on HLDDs, a dynamic engine for latency analysis which is complementary to the formal and semi-formal engines mentioned above, and more general frameworks for pre-silicon and post-silicon/in-situ diagnosis. The dynamic engines and reasoning frameworks were designed and implemented by TEDA, TL, TUT and UNIB.

Diagnosis methods and tools

Various formal, semi-formal and dynamic techniques for error localization on the transaction-level have been developed. This includes techniques to diagnose overconstrained formal specifications, to diagnose inconsistencies between hardware descriptions and their transaction-level specification, techniques based on symbolic execution, and techniques using program slicing. A new tool FoREnSiC implementing the transaction-level diagnosis and correction techniques has been released by the DIAMOND consortium partners TUG, UNIB and TUT. Moreover, a fault-management infrastructure for multi-processor system-on-chip architectures has been created.

At the implementation-level (i.e. register-transfer and logic level) several methods and tools have been developed. This includes a design error localisation method based on HLDD backtrace, the latency analysis tool for identifying the time a sequential circuit may be influenced by erroneous values, a model-based diagnosis tool, a dual model framework to increase the throughput of a soft errors injection framework by identifying error vanish time and a critical fault list generation to limit the number of soft errors to be simulated. The implementation level tools have been developed mainly by UNIB, TUG, IBM, TEDA and TUT.

The post-silicon and in situ diagnosis and correction tools have been mainly developed by Ericsson, LIU and TL. These include a method for efficient embedding of deterministic test data to enable flexibility in the type of commands that can be issued while keeping the memory requirements for storing deterministic test data low and the fault management approach containing techniques for error classification and for parallel scheduling of tests with synchronisation. In addition, a fault management architecture for on-line diagnosis is being developed.

Regarding the tool integration within DIAMOND, TEDA is building a verification Portal that will make use of techniques developed. The Portal will accommodate each of the partner's tools running on their discrete machines connected by a common network. A common set of design cores, the DIAMOND platform, will be used so that each participant's engine can be tested against the same designs. Metrics will be developed to show the effectiveness of each partners' algorithms. Initial integration of the first tools into the TEDA workflow engine has taken place.

Dissemination
The web site for the DIAMOND project was created under the URL: http://fp7-diamond.eu/ and a large number of press releases have been published worldwide, altogether in 10 different languages, including local TV, radio interviews, articles in items like EETimes, CNN, USA Today, Processor, IT Jungle, Design&Reuse, PR Newswire and several others.

The project was exhibited at the European Project Booth of the Design Automation and Test in Europe (DATE) Conference and Exhibition in March 8-12, 2010, Dresden, Germany.

On March 17, 2011, Grenoble, France the DIAMOND dissemination workshop titled "Handling the challenges of debugging and reliability" held in conjunction with the ACM/IEEE Design Automation and Test in Europe (DATE 2011) conference presented the latest research results on design error debug and reliable computing. The workshop was presented in form of a tutorial and it attracted 27 participants.

By the end of the second project year 46 scientific papers related to the topics of DIAMOND have been published by the consortium.

The expected final results

The result of the project will be a **scalable and robust environment for handling faults in semiconductor design.** This development environment will provide diagnostic information needed for the correction of faults, be they design faults, implementation faults, or soft errors. The diagnostic information will be either on the source-level, the logic level, or the gate level, depending on the level of abstraction on which the design is provided. Such information may consist of the location of a fault or a soft error vulnerability. The environment will also suggest measures for correction of the fault or vulnerability wherever possible, where the type of the correction will be suitable to the level of abstraction in which it is needed. The environment will significantly reduce the time spent on error analysis and design modification, hence increasing the designers' productivity.

Potential impact and use

Electronics and information systems play an ever-increasing role in the worldwide economy, representing already today nearly 10% of Gross Domestic Product (GDP). The embedded systems technologies are deployed in all market sectors – automotive, aerospace, medical, environment, communications, entertainment, textiles, transport, logistics, printing and chemicals, food & drink, timber and materials, possessing therefore a **tremendous economic potential for European companies and significant impact on the everyday life of European citizens**.

While the US has led the world in the domain of desk-top PCs and the associated networks, Europe has quietly led the revolution in Embedded Systems. In electronics in general, Europe has a stronger position in design than in manufacturing, with market shares of 27% and 20% respectively. **Embedded Systems know-how underpins the competitiveness of key European industries such as automobile, consumer electronics, medical systems, and energy control.** The situation is similar in other sectors as more and more embedded electronic systems are used to make products and processes more intelligent. The strong and increasing penetration of embedded systems in products and services creates new business opportunities for enterprises, but also imposes to deal with relevant and strategic research issues.

Nonetheless, due to broader range of applications and hence **versatility of user needs**, systems designers and manufacturers are on daily basis faced with **increasing complexity** of their work, which can result in **growing number of system errors**. Identifying, localising and correcting the faults is a **time-consuming** process, which is a significant **financial loss** for businesses involved

and can cause **malfunctioning applications** for everyday users. Latter is not only reflected in useless electronics, but also in **gambling with lives** of drivers (automobile industry), patients (medical systems) etc. In summary, to **guarantee** on one hand **the safety and satisfaction of consumers** and on the other hand to **increase the design competence and productivity of enterprises, miniaturised systems need to be designed more efficiently, first-time right**. They should be **free of design errors** as well as **tolerant to errors originating from the operating environment.**

Fault localisation and correction in ICs constitute 2/3 of the total time spent on verification and debug. Verification and debug (i.e. assuring the correctness of the design) or in other terms the time spent on it, in turn **represent the main reason of excessive costs**. At the same time, due to entering the deep-submicron era (below 45nm), the semiconductor industry is faced with rapidly **growing rates of soft errors**. **We estimate that DIAMOND design flow would bring about**

- **50 % reduction in time spent on fault localisation and correction**
- **25 % reduction of the time to identify a given number of soft error escapes**
- **30 % increase in the number of identified unprotected soft errors**

Note, that the provided improvements take into account the design costs only and do not include costs required for chip manufacturing, such as e.g. mask costs.

The planned impact of DIAMOND will not be achieved during the project, but as a result of it.