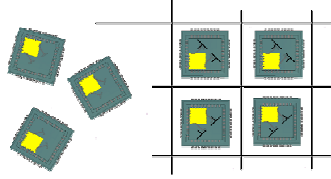# Silicon-based Ultra Compact Cost-efficient System Design for mmWave Sensors "SUCCESS"

Deliverable
D4.5

Mm-wave frontend ICs (v.2) test report v.2
(Confidential, results not published)

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Abstract
This document describes the test report of the redesign of 122 GHz analog-frontend (AFE). The original designs have been described in D4.3. The bugs have been fixed and some design parameters have been improved in this report. The first part is the report of the ZIF transceiver bug fixing, and the second part is the redesign of the hererodyne transceiver.

Keywords
mm-wave sensor, SoC, 122 GHz radar, single chip transceiver, build-in-self-test (BIST), design for test (DFT), SiGe BiCMOS

1. Introduction

This is the second report of the analog frontend (AFE) transceiver chipset. Both the ZIF and the heterodyne transceiver chipsets have been redesigned and tested again. The major results have been tested and reported in the first version of report v.1. In the redesigns, some parameters and performances have been improved and some bugs have been fixed. In the ZIF transceiver chipset, the voltage mismatch between the digital SPI register and the VCO digital tuning is fixed. The frequency measurement unit has been redesigned and it is working as expected. An extra digital pad is introduced to monitor and feed in the gating signal for the frequency measurement unit to have a better control and better insight to the interface between the digital and analog building blocks.

In the heterodyne transceiver, the only issue from the previous chipset is the frequency shifting up to somewhere 140 GHz. In the redesign, the VCO frequency has been tuned back to right 122 GHz band.

2. ZIF chipset redesign

Together with IHP in the SUCCESS-project, Silicon Radar submitted the redesign of radar transceivers which were fabricated in IHPs SG13 SiGe BiCMOS technology in the run T268.

After the measurements of the transceiver chips from testfield T252 the following improvements and corrections were implemented:
- implement control of the output power
- develop an amplifier for the DAC output signal
- add an extra pad for the gating signal of the Frequency Measurement Unit
- insert additional stage(s) to frequency divider in simple chip

 Error! Reference source not found. shows the circuit architecture of the two FMCW radar chips developed by Silicon Radar:
   a) Complex radar system with RX and TX and with digital control of all the circuits via SPI-bus
   b) Simple radar system w/o digital control

The complex radar system shown in **Error! Reference source not found.**a) consists of 120GHz push-push oscillator as a central part of the system. The RF-power generated there is directed to the TX-antenna via power amplifier. The power level can be measured by two power detectors placed between the power amplifier and TX-output. The RF-signal from oscillator is directed to RX-path via buffer circuits. The RX-signal is amplified by LNA and converted to baseband in two mixers with qadrature LO. The 120GHz oscillator has a digital 3-bit coarse tuning input and one analog fine tuning input. The analog fine tuning input can be used for CW radar operation with fixed frequency in PLL-mode by using the internal frequency divider (1/16) or for FMCW-radar with internal ramp-generation by using the integrated DA-converter. For smoothing the staircase voltage from the DA-converter, an external filter is provided. For calibration of oscillator frequency, a frequency measurement

unit is integrated. High-speed ramps can be generated with the internal memory (shift-register) with fast clocking. All the functionality is controlled by SPI-bus.

The second version is a more simple design. It is intended for CW radar system w/o all the digital and DA control to ensure functionality for the case that the complex radar system with the complicated interaction of RF, analog and digital parts will fail to work. The simple radar chip consists of oscillator, power amplifier, power detector, quadrature receiver and frequency divider for connection of external PLL-circuit. IF-amplifier and filter (marked in blue in **Error! Reference source not found.**) are not integrated in the test-structure of the first run.
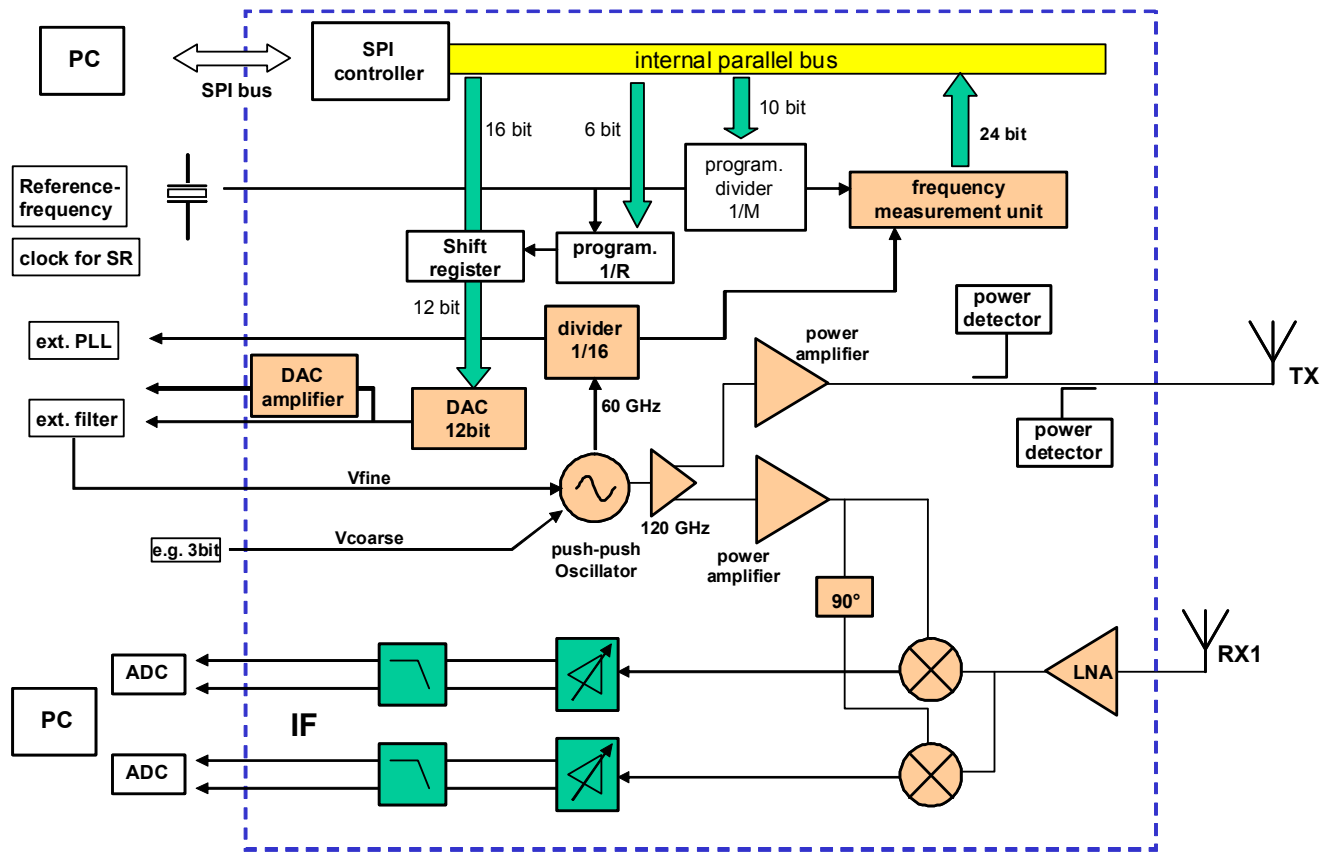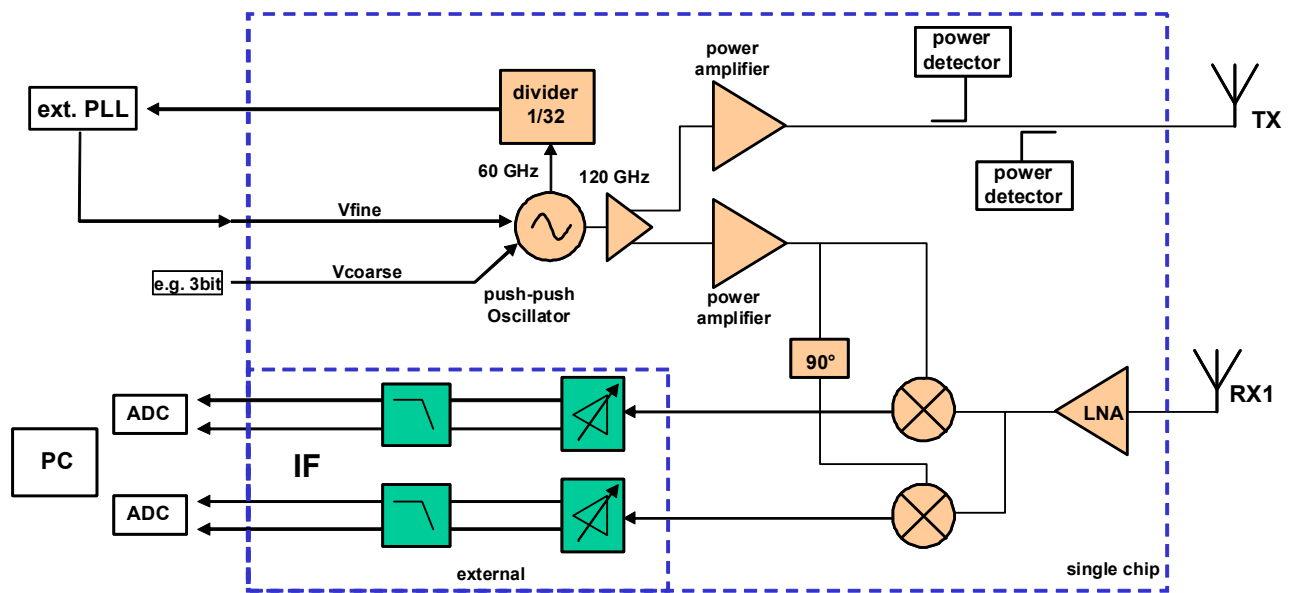
Figure 1 Block circuits of 122GHz Frontend a) complex radar system, b) simple radar system

2.1 Measurement Setup

Dedicated PCBs were developed for the measurement setup which is shown in Figure 2. The chips were mounted on small boards and then all the low-frequency interfaces were bonded. The 120 GHz transceiver input output were contacted using high frequency probes. The board with IC is attached to the so-called main-board equipped with all necessary connectors.
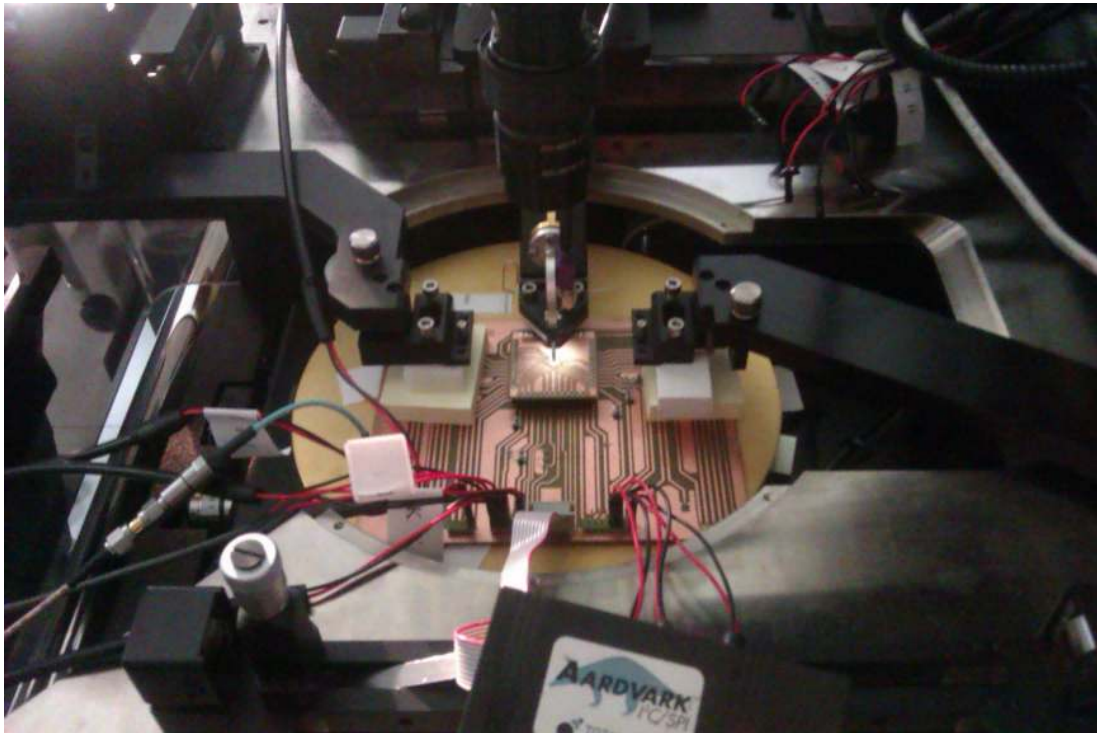
a)
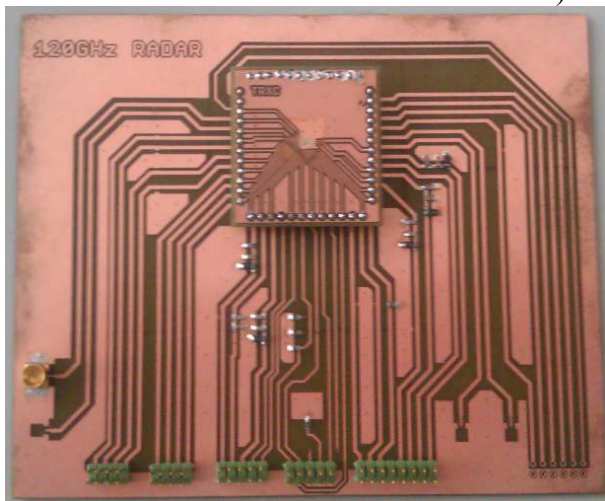
b)
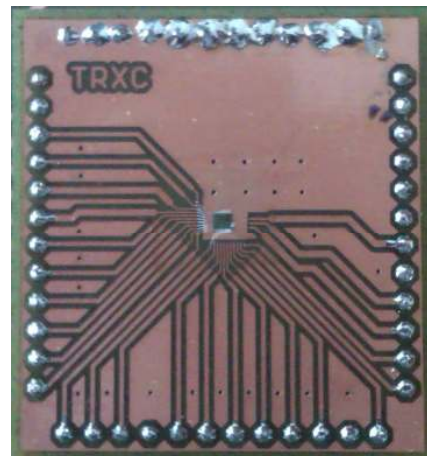
c)

Figure 2 Measurement Setup.

An Aardvark SPI host controller with appropriate software was used to access the digital control of the radar transceiver chip.

2.2 122 GHz Complex Radar System Measurement Results

2.2.1 RF frontend Measurements

The measured parameters of the radar chip are summarized in Table 1. It features moderate power consumption of about 380 mW. The receiver input is well matched to 50 Ohm as presented in Figure 3 a) and b). The conversion gain of the receiver reaches 25.5 dB and can be reduced to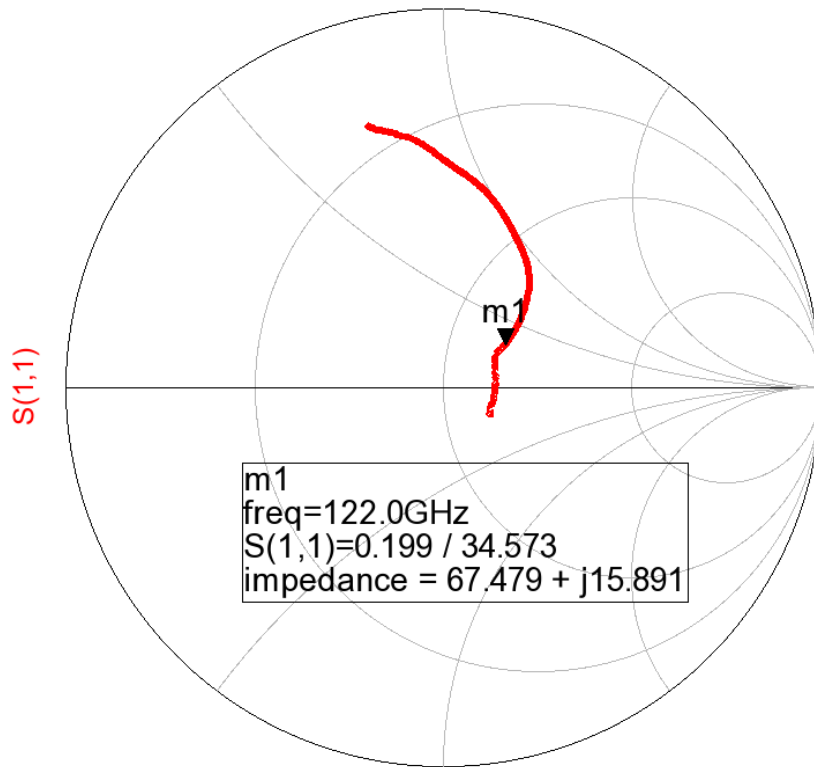 10 dB. The gain control is realized by digitally controlled VGAs. The receiver reaches 1 dB ICP at the input power of -25 dBm for the maximum gain as shown in Figure 4. Tuning characteristic of the VCO was measured at the divider output and then scaled by the division ratio (32). As shown in Figure 5, the overall tuning range of the VCO is 8.4 GHz divided in 8 sub-bands. The choice of the sub-band is done digitally by programming appropriate bits of the SPI register. The phase noise shown in Figure 6 is measured at the divider output as well. It was not corrected about the division ratio (extra 6 dBc per division by 2).

Table 1: Summary of measured parameters of the Complex Radar Transceiver

Parameter	Value
Supply voltage - analog	3.3 V
Supply voltage digital	1.2V
Current consumption ICC	114 mA
Gain	10-25.5 dB
Input Compression Point	-25 dBm
VCO tuning range	122.1 – 130.5 GHz
Output power	-0.5 – -7 dBm

S(1,1)

m1
freq=122.0GHz
S(1,1)=0.199 / 34.573
impedance = 67.479 + j15.891

freq (90.00GHz to 140.0GHz)

a)

S(2,2)

m2
freq=122.0GHz
S(2,2)=0.285 / 170.338
impedance = 27.940 + j2.913
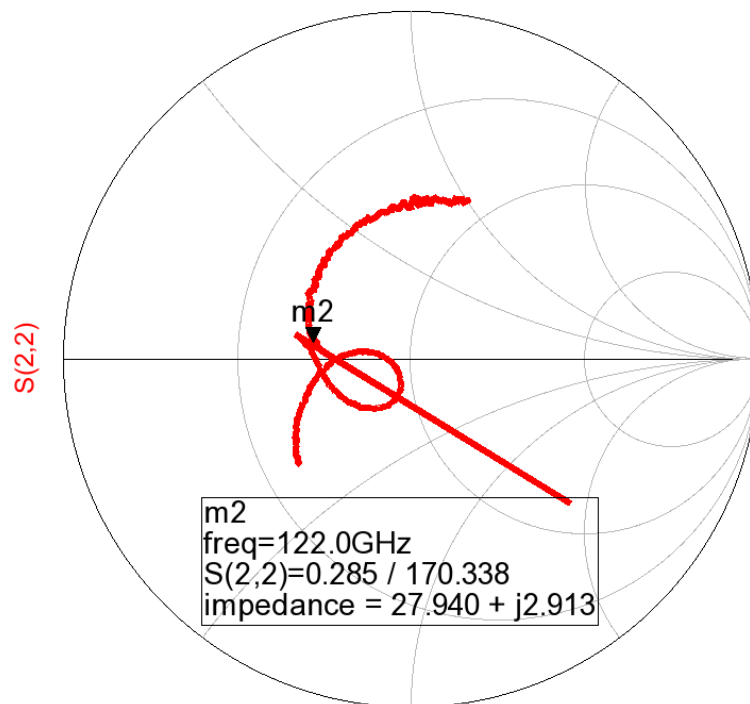
freq (90.00GHz to 140.0GHz)

b)

Figure 3 Measured a) S11 and b) S22 of the Transceiver.
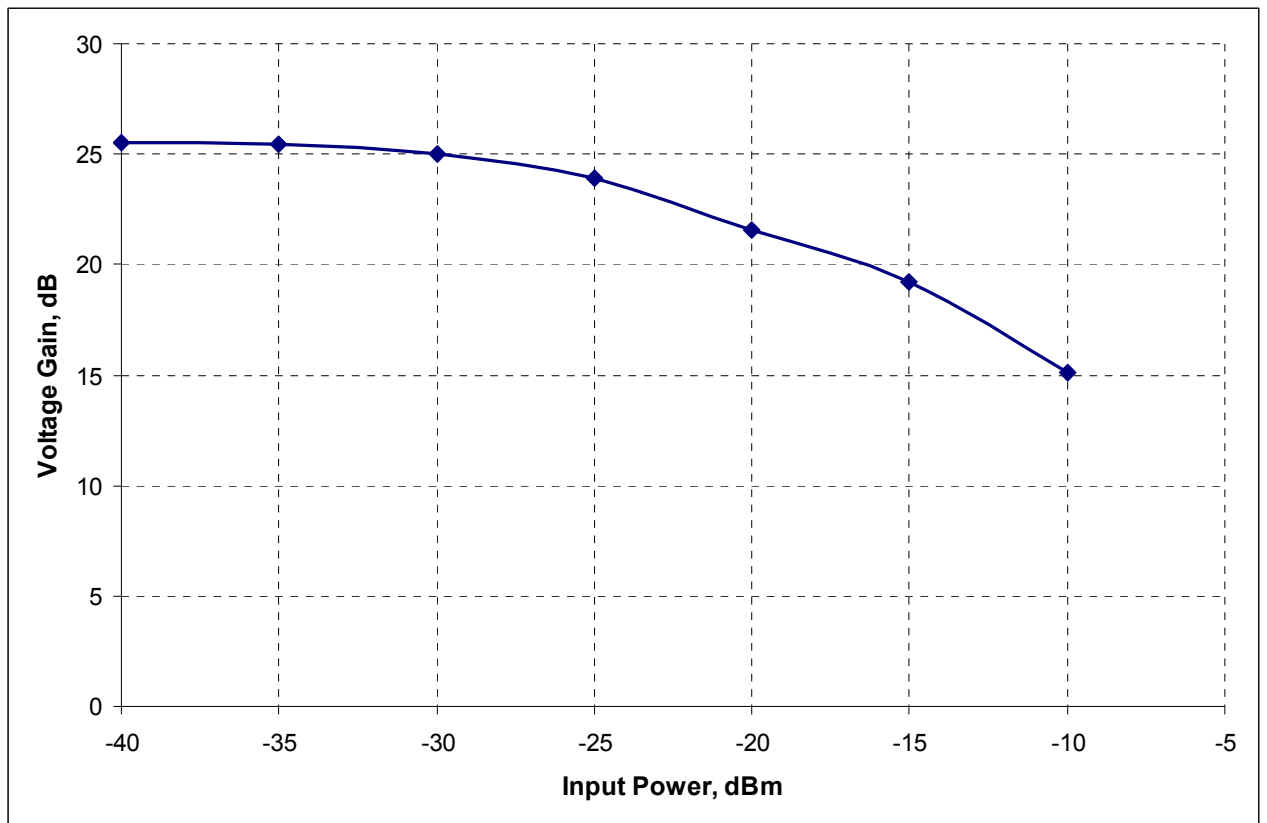
Figure 4 Measured Conversion Gain of the receiver.
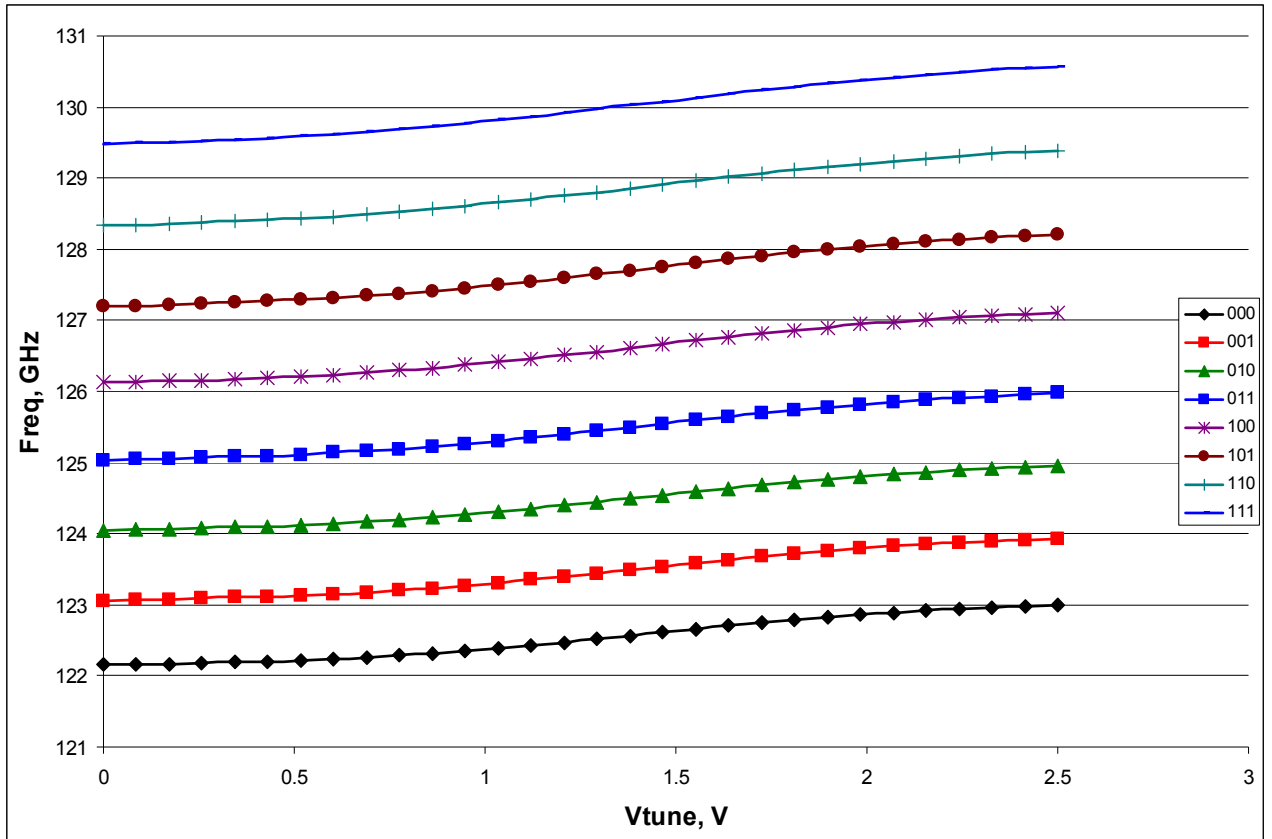
Figure 5 Measured tuning range of the VCO
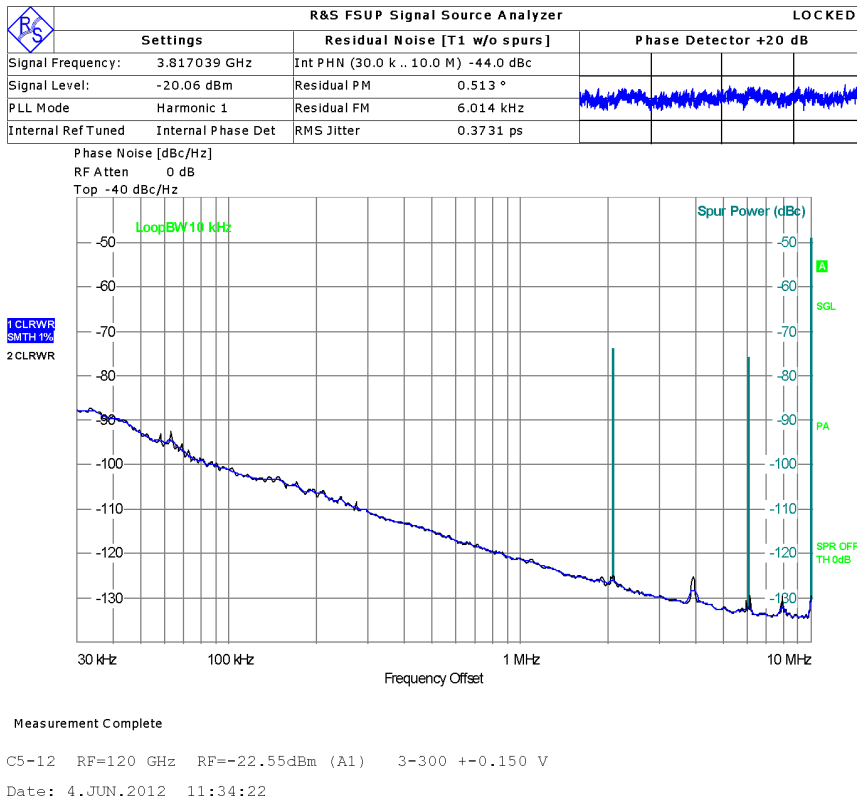
Figure 6 Phase Noise of the VCO measured at frequency divider output.

2.2.2 Digital Control

The top-level architecture of digital control design is shown in Figure 7, whereas the layout view is shown in Figure 8. The digital pads are located at the top side of the layout view.
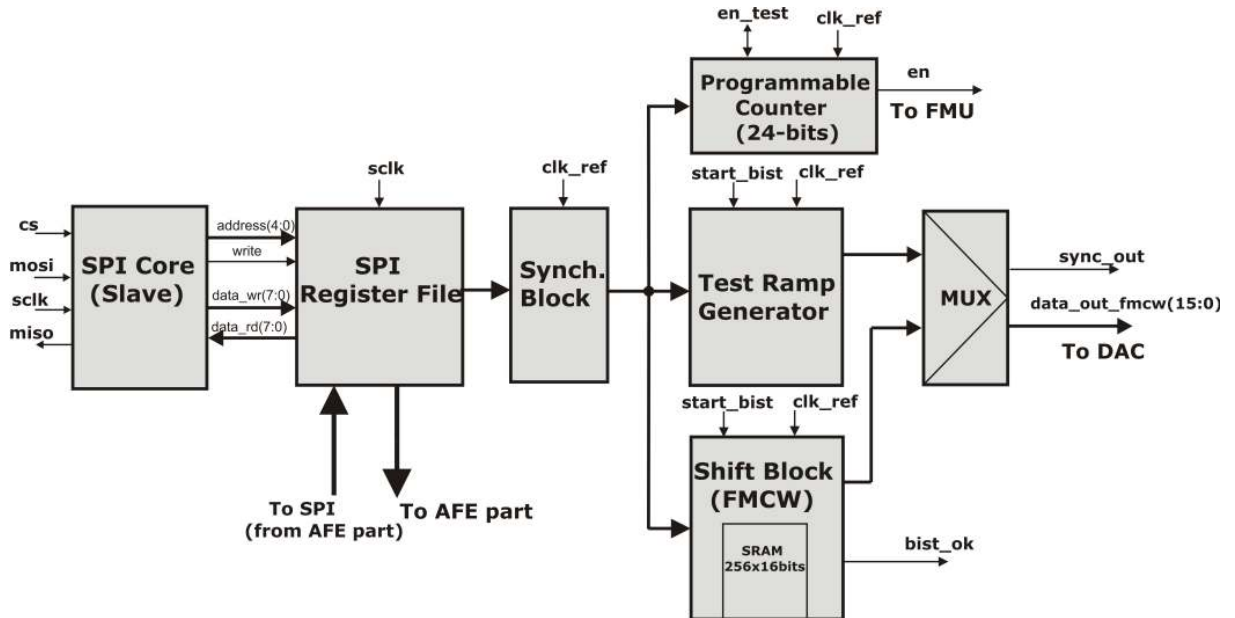
Figure 7 Block diagram of digital control block
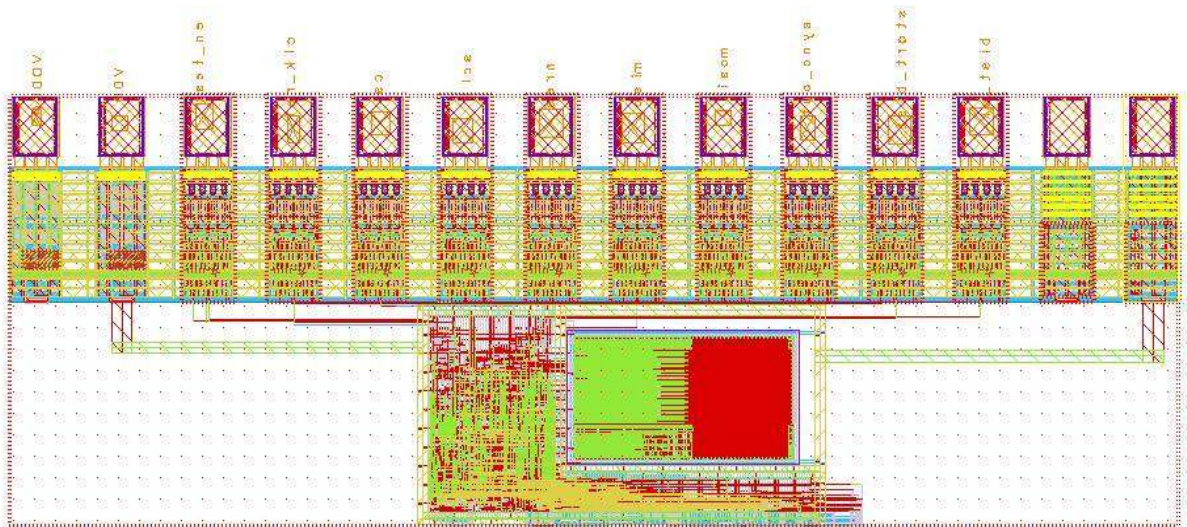
Figure 8 Layout view of digital control block

The digital control block is composed of the following subcomponents:
- **SPI Core**

  This subcomponent is responsible for communication between the BB processor and the RF Front-End. It always runs in a slave mode. The BB

processor contains the SPI master controller requesting communication and providing *SPI* clock and *CS* signal.

- **SPI Register File**

These registers are employed to store data transferred via SPI core. There are in total 26 registers with bit-width of 8 bits.

- **Synchronization Block**

This subcomponent is employed to cross over two clock domains (denoted by '*sclk*' and '*clk_ref*') without hazards.

- **Programmable Counter**

This subcomponent (timer) provides an enable signal for frequency measurement. The enable signal is active within time interval programmable via SPI interface.

- **Test Ramp Generator**

This subcomponent is able to generate a frequency ramp with three different time periods, but with pre-determined values of the frequency ramp. The purpose is to have an opportunity for the DAC testing without programming a RAM memory cell in the Shift Block.

- **Shift Block**

This subcomponent is used for storing frequency ramp values sent by the BB processor and transferred via SPI interface. For storing those values, a RAM memory cell with size 256x16 bits is employed.

The Table 2 summarizes the pin description of the digital control. In comparison to the previous version (tapeout March 2011), an additional digital pad ('*en_test*') has been introduced. The purpose of this pad is to test the timer as well as to have possibility to externally drive the FMU.

Table 2 Pin Signal Description of Digital Control

Name	Type	Polarity or Bus Size	Description
nres	In (Pad)	Low	Hardware reset input
clk_ref	In (Pad)	Rise	Reference clock, default value 50 MHz
sclk	In (Pad)	Rise and Fall	SPI clock (SPI interface)
cs	In (Pad)	Low	Chip Select (SPI interface)
mosi	In (Pad)	Level	Master-Output-Slave-Input (SPI interface)
miso	Out (Pad)	Level	Master-Input-Slave-Output (SPI interface)
start_bist	In (Pad)	High	Start signal of BIST SRAM memory
bist_ok	Out(Pad)	High	Pass/Fail signal of BIST SRAM memory

en	Out	High	Enable signal for frequency measurement unit (FMU)
en_out	InOut(Pad)	High	Out Mode : Enable signal for FMU generated by the timer; In Mode : Input external enable signal for FMU;
data0_fmu	In	8	Higher - (23:16) bits of frequency measured by FMU
data1_fmu	In	8	Middle - (15:8) bits of frequency measured by FMU
data2_fmu	In	8	Lower - (7:0) bits of frequency measured by FMU
data_out_fmcw	Out	16	Signal frequency value sent to DAC
sync_out	Out	High	Start of frequency ramp indicated by rising edge
vco_coarse	In	3	VCO coarse value
power_amp	Out	3	Power amplifier value
power_det1	Out	2	Power detector value 1
power_det2	Out	2	Power detector value 2
temp_sensor	Out	4	Temperature sensor value
vga_stage1	Out	8	VGA value 1
vga_stage2	Out	8	VGA value 2
vga_stage3	Out	8	VGA value 3
vga_stage4	Out	8	VGA value 4
data1_rd	In	8	General purpose inputs
data2_rd	In	8	General purpose inputs
data1_out	Out	8	General purpose outputs
data2_out	Out	8	General purpose outputs
data3_out	Out	8	General purpose outputs
data4_out	Out	8	General purpose outputs
data5_out	Out	8	General purpose outputs

The Table 3 presents the SPI register map. The bit-width of each register is 8 bits. The number of writable and readable registers is 18 and 8, respectively, which is in total 26 registers.

Table 3 SPI Register Map

Address(4:0)	Access	Description
0	Write	(7 : 2) – Higher (11 : 6) bits of programmable ratio R in FMCW mode; (1 : 0) - Higher (7 : 6) bits of number of frequency points in FMCW mode;
1	Write	FMCW mode: (7) – writing/reading mode bit; Logic '1' – writing mode; Logic '0' – reading mode; (6 : 1) bits Writing mode : lower (5:0) bits of number of frequency points; Reading mode : lower (5:0) bits of programmable clock ratio

		R; (0) – freeze bit ; In reset state, as long as FMCW mode bit is '0', freeze bit (low active) prevents reading unknown values from memory and delivering those unknown values to DAC;
2	Write	FMCW mode : Higher – (15:8) bits of a signal frequency;
3	Write	FMCW mode : Lower – (7:0) bits of a signal frequency
4	Write	Higher – (23:16) bits of programmable counter used for frequency measurement
5	Write	Middle – (15:8) bits of programmable counter used for FMU
6	Write	Lower – (7 :0) bits of programmable counter for FMU
7	Write	(7:5) bits – VCO coarse value (4:2) bits – Power amplifier value; (1:0) bits – selecting bits for frequency ramp duration in test mode; (0) bit – selecting whether 'en_test' pad is IN or OUT ; Default value is zero – OUT pad;
8	Write	VGA coarse gain control – c<0> - c<3>
9	Write	VGA fine gain control – vg2<0> - vg2<6>
10	Write	VGA stage current control – vb<0> … vb<7>
11	Write	VGA stage 4 value
12	Write	Memory address in test mode
13	Write	Bit 7 = mux_C1;Bit 6 = mux_C2;Bit 5 = mux_C3;Bit4 = mux_C4 Bit3 = divEN; Bit2 = buffEN; Bit1 = FC_RST;Bit0 = FC_PWR
14	Write	Data2_out value
15	Write	Data3_out value
16	Write	Data4_out value
17	Write	Data5_out value
18	Read	(7:6) bits – Power detector 1 value (5:4) bits – Power detector 2 value (3:0) bits – Temp. sensor value
19	Read	Higher – (23:16) bits of frequency measured by FMU
20	Read	Middle – (15:8) bits of frequency measured by FMU
21	Read	Lower – (7:0) bits of frequency measured by FMU
22	Read	Data1_rd value
23	Read	Data2_rd value
24	Read	Higher – (15 :8) bits of memory cell output in test mode
25	Read	Lower – (7:0) bits of memory cell output in test mode

2.3 SPI Host Adapter and PC application

For accessing the digital control of the Radar 122 GHz chip, we have used an Aardvark SPI host adapter (www.totalphase.com). That is a small box connected to an USB port of PC which provides a SPI host (or slave) and an I2C interface. The Aardvark software comprises a GUI for interactive access under Windows and Linux

and a programming library for C, Labview, etc. The communication between PC, Aardvark adapter and Radar chip is illustrated in Figure 9. In our testing environment, the Aardvark SPI adapter is always a host (master) SPI.

Figure 9 PC, Aardvark Adapter and Radar 122 GHz chip

We have used an C application developed for communication between the Aardvark SPI host adapter and the SPI slave implemented in the digital control of Radar chip. By using the C application, we are able to perform the operations summarized in Table 4, which will be explained in later in the text.

Table 4 The SPI operations supported by C application

1.	Read SPI register
2.	Write SPI register
3.	Configure SPI word
4.	Reset SPI slave
5.	Fast ramp programming: rising edge
6.	Fast ramp programming: rising + falling edge
7.	Fast ramp programming: rising edge + flat region + falling edge
8.	Automatic VCO tuning

2.3.1 Test procedures

2.3.1.1 INITIALIZATION (RESET)

After connection Aardvark SPI adapter and switching power-on, it is required to initialize (reset) the digital control before starting any programming of SPI registers. For this purpose we have used the operation "Reset SPI slave" (Table 3). Basically, that operation delivers a low-level signal for a short time at input 'nres' pin of the chip. Since the reset signal is synchronized with clock reference signal, it is required to have active clock reference signal during reset. The timing diagram is shown in Figure 10.
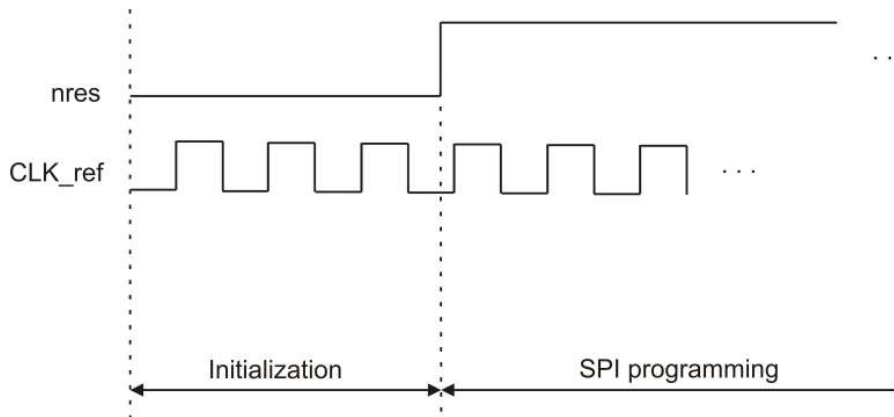
Figure 10 Initialization (reset)

In order to ensure correct operation of digital control, an initialization procedure shall be always done after switching power-on.

2.3.1.2 CONFIGURATION OF SPI WORD

Before programming of any SPI register, it is required to configure the SPI word. The size and composition of a data word, which must be transferred on the SPI bus in order to read or write registers in SPI slave, depends on the SPI slave configuration. It constitutes of: register address, read enable bit, data word and write enable bit. In our configuration, the read enable bit is not present. Configuration parameters of the SPI word in our chip are summarized in Table 4.

Table 5 Configuration parameters of the SPI word

Addressable Registers	Address Bits	Data Bits	Write Enable Bit	Read Enable Bit	Total SPI Word Bits
26	5	8	1	0	14

2.3.1.3 SPI PROGRAMMING

The SPI programming (writing and reading registers) is based on communication protocol shown in Table 6 and Table 7. Since the Aardvark adapter may send and receive only 8-bit (a byte) words over SPI interface, the communication protocol is based on exchanging two data bytes.

Table 6 Write to SPI register

SPI bit number	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SPI Input	SPI register address					written data								1	0	0
SPI register	the first write								the second write							

Table 7 Read from SPI register

SPI bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

number																
SPI input	SPI register address					0	0	0	0	0	0	0	0	0	0	0
SPI output	-					read data								-	-	-
SPI register	the first read					the second read										

The chosen SPI clock polarity (CPOL) and SPI clock phase (CPHA) values are CPOL = '1' and CPHA = '1'. Data transmission format for one byte of such configuration is shown in Figure 11. The SPI slave in digital control can support only this transmission format. The SPI master and slave need to agree about data transmission format. Therefore, it is required to configure the Aardvark adapter (SPI master) to support the same transmission data format as the SPI slave.
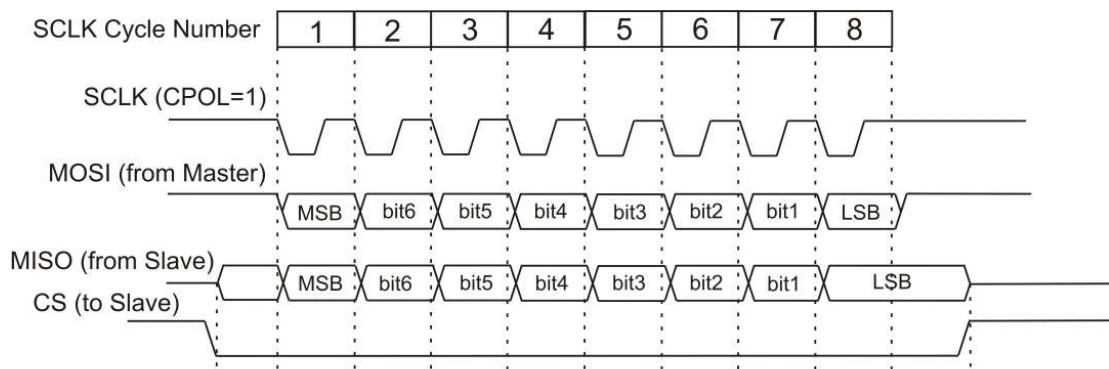
Figure 11 SPI Data Transmission Format

The functionality of the SPI slave itself can be checked by a simple write-read procedure. An arbitrary data can be written in to a SPI register and then read out that register to check whether the same value is read out.

Example:

To write data value "10100110" in register 8, the following bits shall be sent:

address(4:0)					data value (7 :0)								we	dummy	
0	1	0	0	0	1	0	1	0	0	1	1	0	1	0	0

After a write enable bit (we) the two dummy bits (zeros) shall be sent to fill the complete SPI word consisting of two bytes.

To read the register 8, the following bits shall be sent:

address(4:0)					data value (7 :0)								we	dummy	
0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Note that after the address bits, all remaining bits are zero bits.

2.3.2 Digital Ramp Generation

We have used the following procedure to generate the digital ramp:

1. Set the following parameters: writing mode of RAM cell, number of ramp points, and programmable ratio R (bits(11:6)). This is done by programming SPI register 0 and 1.

2. Fast ramp programming. In this step the values of ramp which will be generated are written into RAM cell. By using the current version of C application we are able to perform fast ramp programming with the three different ramp shape, see Table 4 and Figure 12. In principal, the shape of ramp is only an software issue which means that we are able to generate any shape of ramp by a software modification. Since we have implemented a 12-bit DAC in Radar chip, the maximum value of ramp is 4095.

3. Set the following parameters: reading mode of RAM cell and programmable clock ratio R (bits (5:0)). This is done by programming again register 1. Once this step is finished, the digital ramp is generated with period of :

$$T_{ramp} = \frac{(R+1)N}{f_{clk\_ref}}$$

where R is the programmable clock ratio, N is the number of ramp points and f_{clk_ref} is the reference clock frequency.

rising edge   rising && falling edge   rising edge && flat region && falling edge
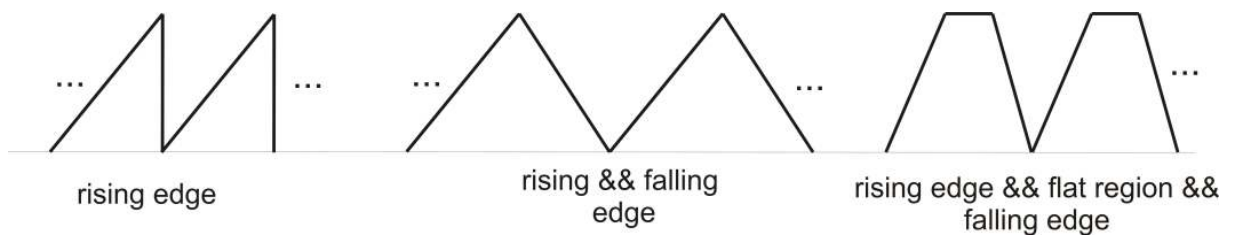
Figure 12 Shapes of digital ramp supported by SPI software (C application)

Example 1:

1. Programming of register 0 and 1:

Register 0: Write "00011111"; in hex format: 1F
Register 1: Write "11111111"; in hex format: FF

2. Fast ramp programming with rising edge:

num_ramp_points = 256; ramp_step = 16; start_value = 0;

3. Programming of register 1:

Register 1: Write "01100111"; in hex format 67

The period of the generated ramp is (f_{clk_ref} = 10 MHz):

$$T_{ramp} = \frac{(499+1)*256}{10MHz} = 12.8 \text{ ms}$$

The maximum digital value of the ramp is 255*16 = 4080 corresponding to the almost maximum voltage level at the DAC output (2.5 V).
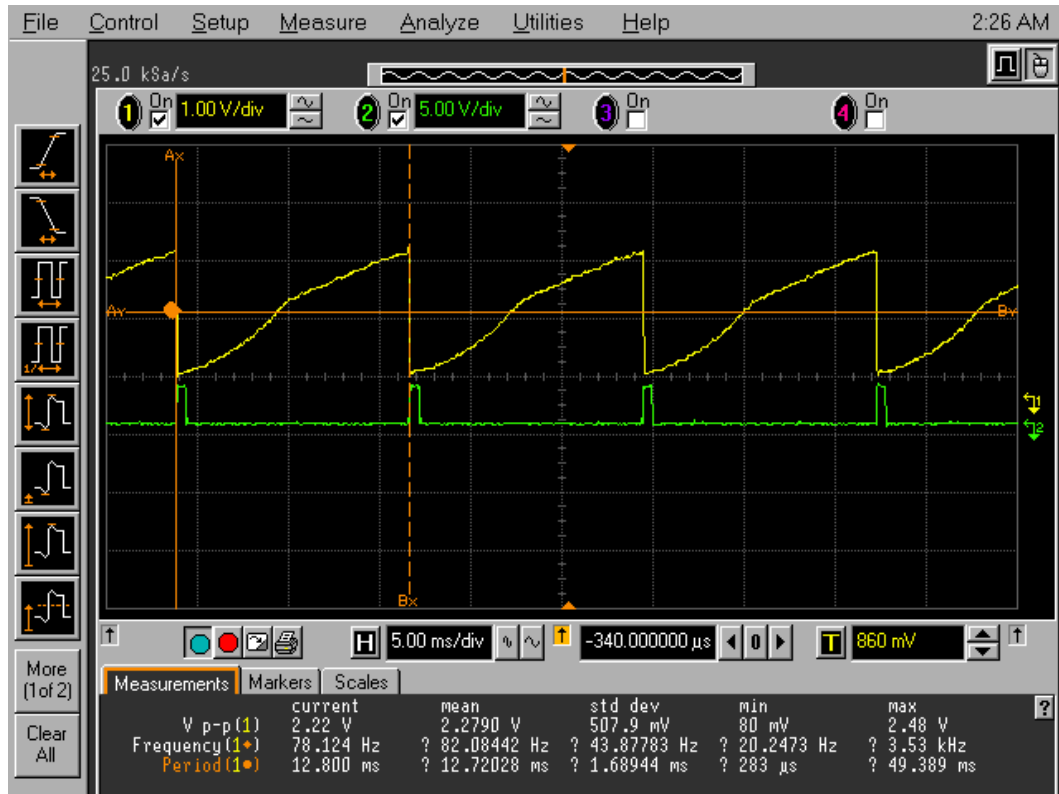

Figure 13 The rising edge ramp: the output signal of DAC (yellow) and 'sync_out' signal (green)

Example 2:

1. Programming of register 0 and 1:

Register 0: Write "00011111"; in hex format: 1F
Register 1: Write "11111111"; in hex format: FF

2. Fast ramp programming with rising and falling edge:

num_ramp_points = 256; ramp_step = 32; start_value = 0;

3. Programming of register 1:

Register 1: Write "01100111"; in hex format 67

The period of the generated ramp with symmetrical rising and falling edge is:

$$T_{ramp} = \frac{(499+1)*256}{10MHz} = 12.8 \text{ ms}$$
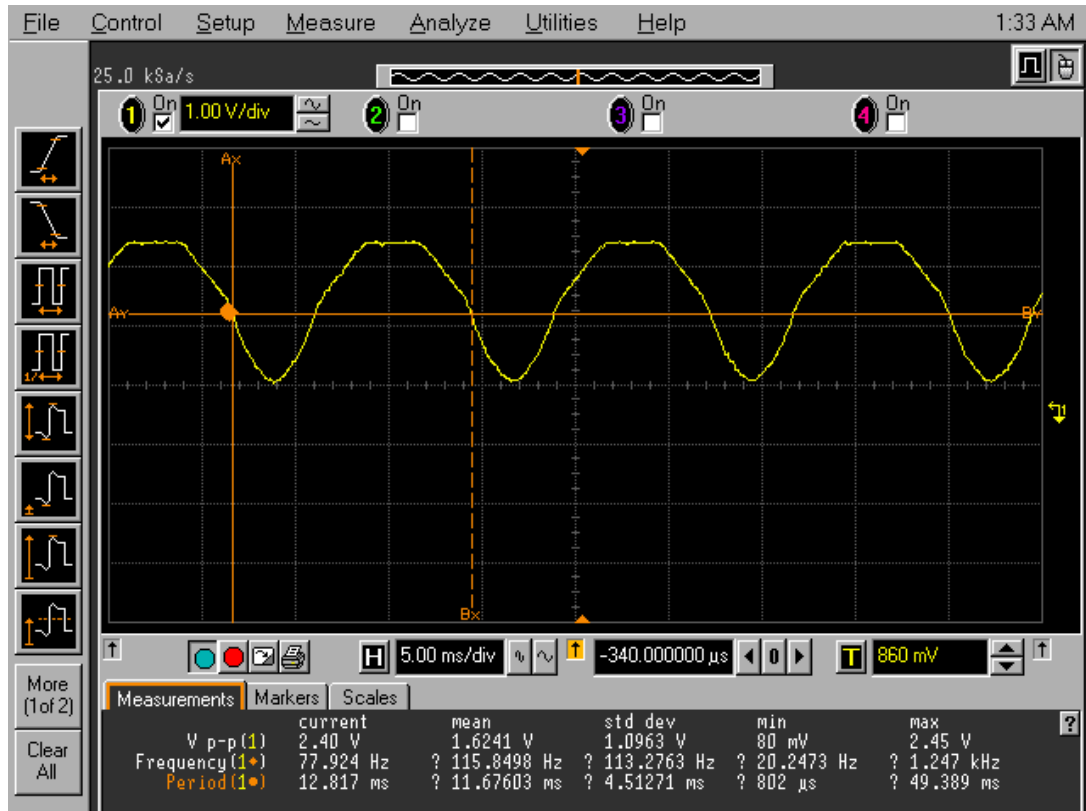
The maximum digital value of the ramp is 127*32 = 4064.
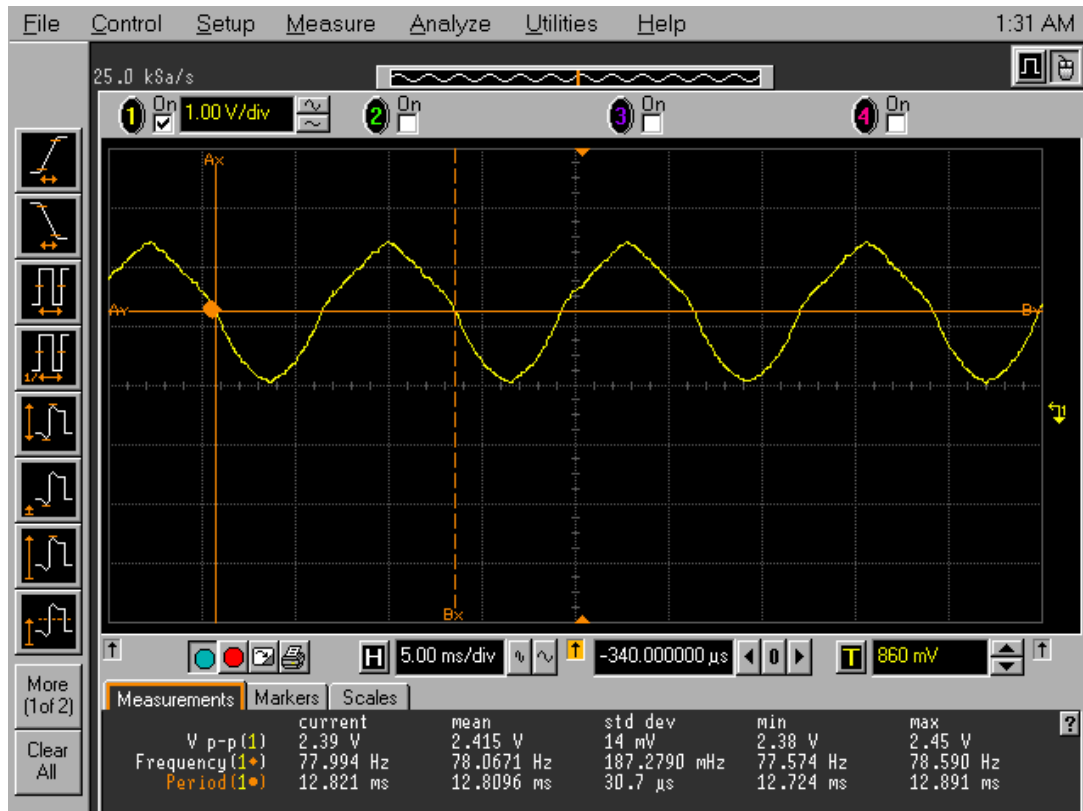
Figure 14 The ramp with rising and falling edge: the output signal of DAC

Example 3:

1. Programming of register 0 and 1:

Register 0: Write "00011111"; in hex format: 1F
Register 1: Write "11111111"; in hex format: FF

2. Fast ramp programming with rising edge, flat region and falling edge:

num_ramp_points = 256; num_ramp_points_flat_region = 56; ramp_step = 40; start_value = 0;

3. Programming of register 1:

Register 1: Write "01100111"; in hex format 67

The period of the generated ramp with flat region and symmetrical rising and falling edge:

$$T_{ramp} = \frac{(499+1)*256}{10MHz} = 12.8 \text{ ms}$$

The maximum digital value of the ramp is 100*40 = 4000.

Figure 15 The ramp with rising edge, flat region and falling edge: the output signal of DAC

Example 4:

1. Programming of register 0 and 1:

Register 0: Write "00000011"; in hex format: 03
Register 1: Write "11111111"; in hex format: FF

2. Fast ramp programming with rising edge:

num_ramp_points = 256; ramp_step = 16; start_value = 0;

3. Programming of register 1:

Register 1: Write "01100011"; in hex format 63

The period of the generated ramp is (f_{clk_ref} = 10 MHz):

$$T_{ramp} = \frac{(49+1)*256}{10MHz} = 12.8 \ \mu s$$
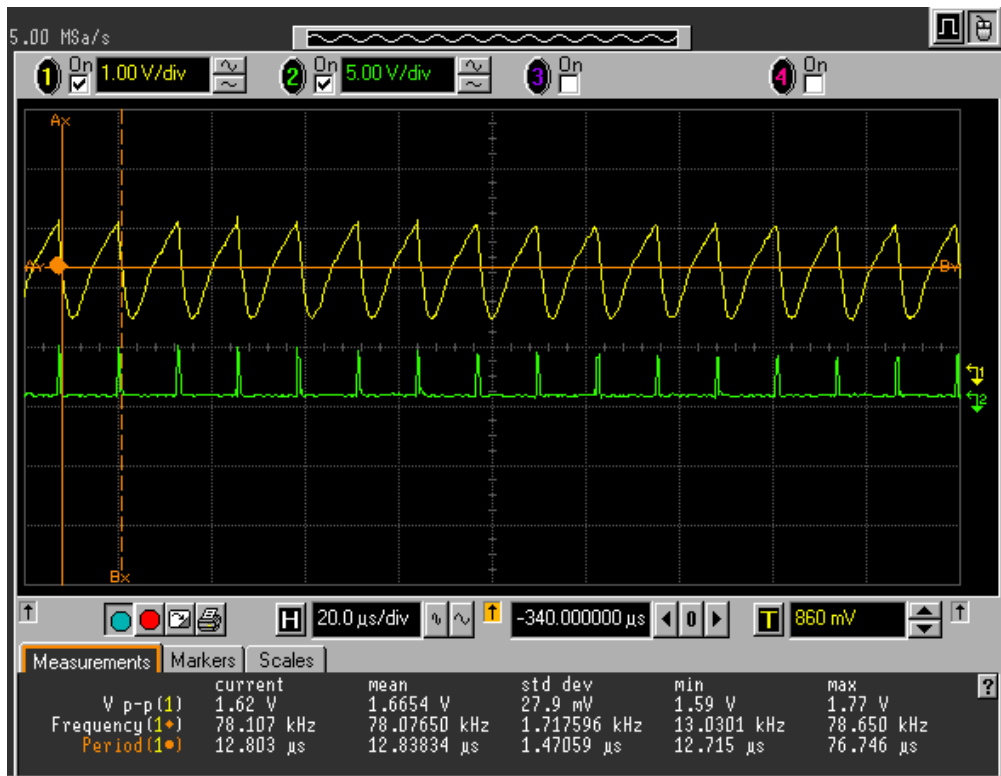
Figure 16 The fast ramp with period 12.8 µs: the output signal of DAC

2.3.3 Frequency Measurement

A timer implemented in the digital control provides an enable signal for frequency measurement. The enable signal is active within time interval programmable via SPI. In order to define that time interval, registers 4, 5, and 6 shall be programmed.

Example :

1. Programming of registers 4, 5 and 6:

Register 4: Write "00000000"; in hex format: 00
Register 5: Write "01001110"; in hex format: 4E
Register 6: Write "00100000"; in hex format: 20

The enable signal required for frequency measurement is active within the time interval of

$$T_{enable} = \frac{M}{f_{clk\_ref}}$$

where M is 24-bits value of registers 4, 5 and 6.

Therefore, T_{enable} is:

$$T_{enable} = \frac{20000}{10MHz} = 2 \text{ ms}$$

2.3.4 BIST Test

BIST test is used to check functionality of RAM cell itself. Additionally, DAC functionality can be also tested without programming RAM cell. The clock reference signal needs to be active with the default frequency of 50 MHz.

The BIST procedure for RAM cell is as follows:

1. Reset the digital control

2. Set high level at '*start_bist*' pin

3. Check a level at '*bist_ok*' pin. If the BIST is successful, the high level is set at '*bist_ok*' pin.

The BIST procedure for DAC testing is as follows:

1. Reset the digital control

2. Set high level at '*start_bist*' pin

3. Check the output the DAC ('*Out_da*') pin. If the BIST is successful, the DAC generates
the ramp with period of 2000 μs.

By programming two bits of register 7, the ramp with period 500 μs or 1000 μs can be generated.

The BIST procedure for DAC testing (the ramp with period of 500 μs or 1000 μs) is as follows:

1. Reset the digital control

2. Programming of register 7:
    Register 7: Write "00000000", in hex format "00" – for the 500 μs ramp
    Register 7: Write "00000001", in hex format "01" – for the 1000 μs ramp

3. Set high level at '*start_bist*' pin

4. Check the output the DAC ('*Out_da*') pin. If the BIST is successful, the DAC

generates the ramp with period of 500 µs or 1000 µs.

2.3.4.1 AUTOMATIC VCO TUNING

The flowchart of the automatic VCO tuning is shown in Figure 17 and can be briefly described as follows. The overall tuning range of the VCO is divided in 8 sub-bands. The choice of the sub-band is done digitally by programming appropriate bits of the SPI register (register 7). For every sub-band, a digital word (from 0 to 4095) is sent do the DAC. Then, by programming SPI registers 4, 5 and 6, the enable signal for the FMU is generated. The registers 19, 20 and 21 which contain the calculated value F are read out. The frequency value is calculated as:

$$Freq = \frac{F - F_{init}}{T_{enable}}$$

where F_{init} is the initial value of register 21 (the lower bits, see Table 2) after the FMU reset by programming register 13. The procedure illustrated in Figure 17 should be repeated 4096 times for each of the VCO sub-bands.

The required time measurement (for single VCO sub-band, 4096 DAC point and SPI master idle state of 10 ms) is approximately 43 sec. The VCO curves are shown in Figure 18.
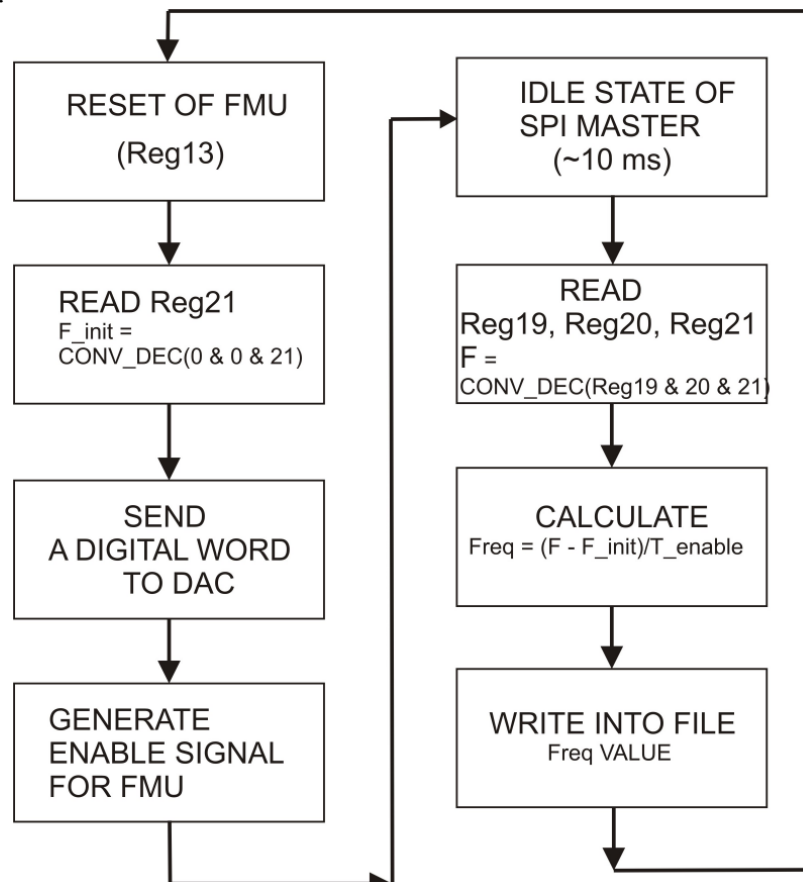
Figure 17 Flowchart of Automatic VCO tuning
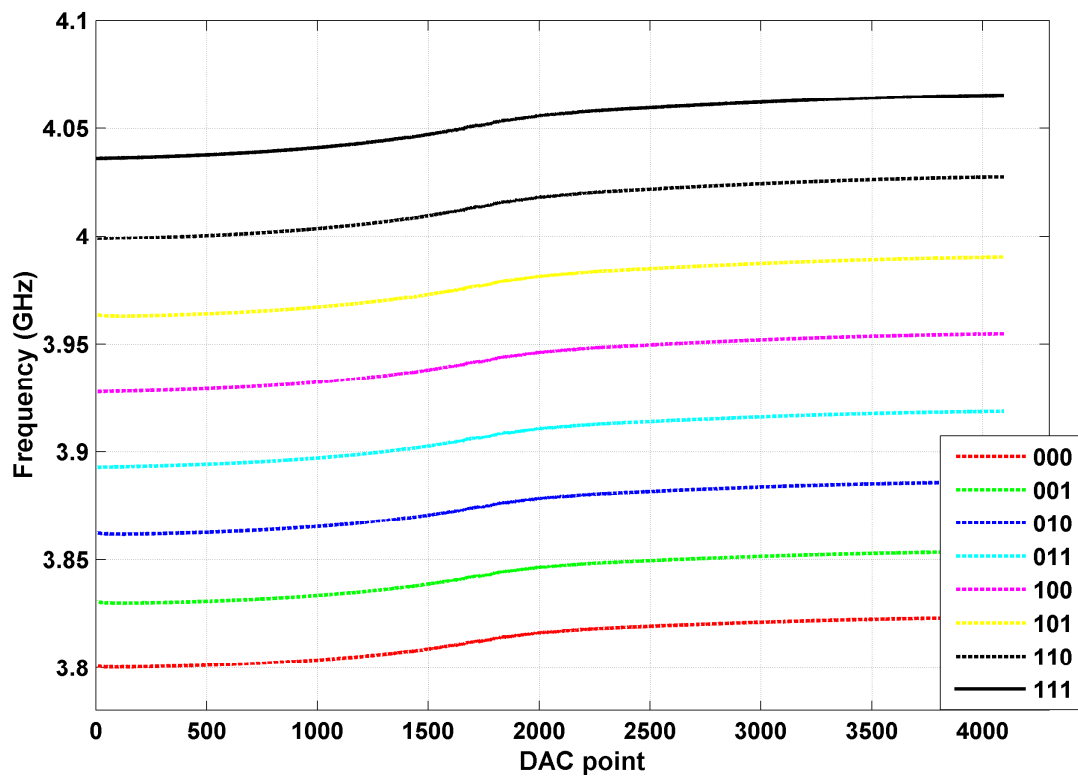
Figure 18 Tuning curves of VCO

2.3.4.2 TEST RESULTS

The Radar 122 GHz chip with the digital control has been taped out in December 2011. With respect to the digital control, all tests have passed successfully. The test results are summarized in Table 8.

Table 8 Test results of digital control

TEST	PASS/FAIL
SPI functionality	PASS
Memory BIST	PASS
DAC BIST	PASS
Ramp generation	PASS
Frequency measurement	PASS

2.4 122 GHz Simple Radar System Measurement Results

The measured parameters of the radar chip are summarized in Table 9. It features moderate power consumption of about 370 mW. The receiver input is well matched to 50 Ohm as presented in Figure 19 a) and b). The receiver features a conversion gain of 10 dB. The receiver reaches 1 dB ICP at the input power of -20 dBm. Tuning

characteristic of the VCO was measured at the divider output and then scaled by the division ratio (32). The overall tuning range of the VCO is 3.7 GHz divided in 8 sub-bands. The choice of the sub-band is defined by applying appropriate voltage level to tuning inputs VT (0 V or 2.5 V). The phase noise shown in Figure 20 is measured at the divider output, but it was not corrected about the division ratio (extra 6 dBc per division by 2).

Table 9: Summary of measured parameters of the Simple Radar Transceiver

Parameter	Value
Supply voltage - analog	3.3 V
Supply voltage digital	1.2V
Current consumption ICC	112 mA
Gain	10 dB
Input Compression Point	-20 dBm
VCO tuning range	121.3 – 128.8 GHz
Output power	-0.5 – -7 dBm

m1
freq=122.0GHz
S(1,1)=0.199 / 34.573
impedance = 67.479 + j15.891

freq (90.00GHz to 140.0GHz)

a)

S(2,2)

m2

m2
freq=122.0GHz
S(2,2)=0.285 / 170.338
impedance = 27.940 + j2.913

freq (90.00GHz to 140.0GHz)
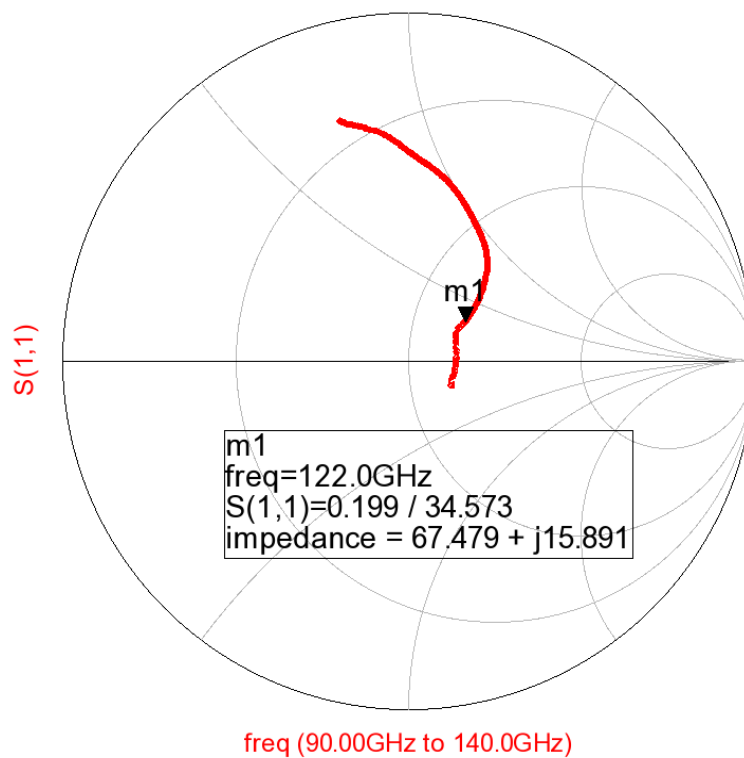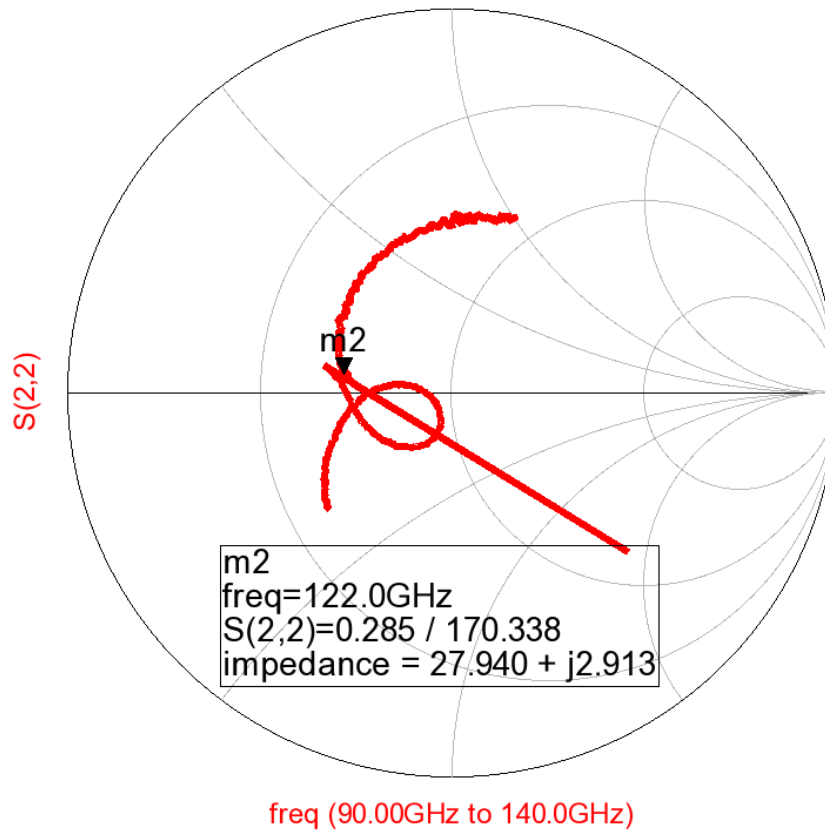
b)
Figure 19: Measured a) S11 and b) S22 of the transceiver.

R&S FSUP Signal Source Analyzer			LOCKED
Settings	Residual Noise [T1 w/o spurs]	Phase Detector +20 dB	
Signal Frequency: 1.893822 GHz	Int PHN (30.0 k .. 10.0 M) -50.2 dBc		
Signal Level: -13.39 dBm	Residual PM 0.251 °		
PLL Mode Harmonic 1	Residual FM 3.368 kHz		
Internal Ref Tuned Internal Phase Det	RMS Jitter 0.3680 ps		
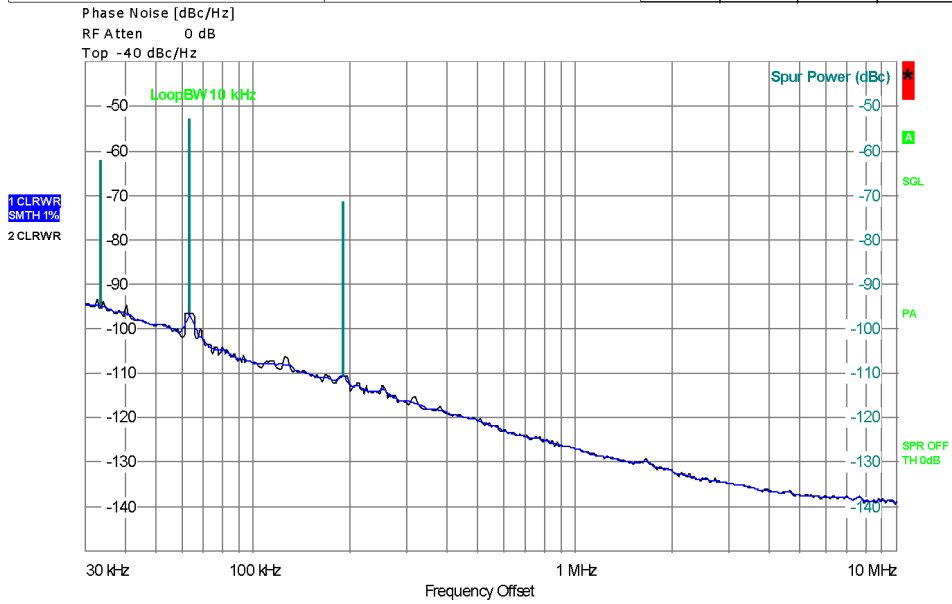
Measurement Aborted

```
C5-12  RF=120 GHz  RF=-22.55dBm (A1)   3-300 +-0.150 V
Date: 4.JUN.2012  12:25:32
```

Figure 20: Phase Noise of the VCO, measured at the divider output
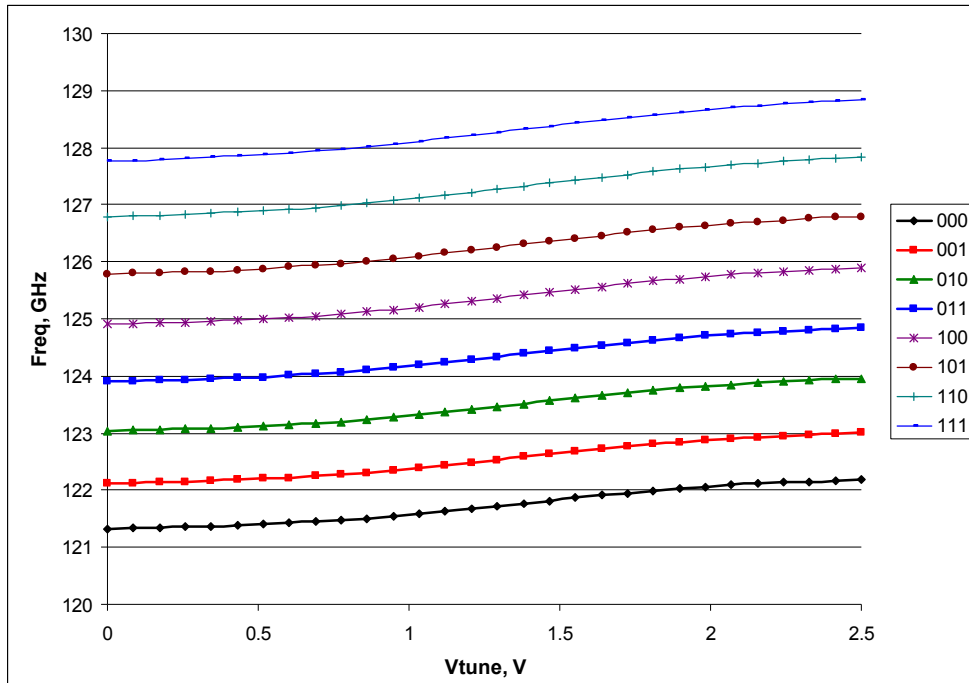
Figure 21 Tuning curves of the oscillator with combined analog and digital tuning (band switching)

2.5 Conclusions

The test results of the 120 GHz Radar Chip are summarized in Table 10.

Table 10: Test summary

Building Block	Parameter	Functionality
Analog Frontend	Gain Linearity Output Power Frequency Range	+ + + +
Power Detectors and Temperature sensor		+
IF Variable Gain Amplifier		+
DAC		+
Digital Control	SPI functionality Memory BIST DAC BIST Ramp generation Frequency measurement	Pass Pass Pass Pass Pass

The developed 120 GHz Radar Transceivers fulfil system specification. The functionality of all the building blocks is proven. The redesign of the first version of radar transceivers was successful and all the problems were solved.
120 GHz complex and simple transceivers developed within the project are ready to be implemented in short-range radar sensors for process control, low-cost consumer products and tools and instruments.

3. Heterodyne Transceiver Redesign

Two transceiver chips were designed and fabricated in two separate tapeouts, in April 2011 and in February 2012, respectively. The April 2011 chip experienced a frequency shift in the VCO frequency, which oscillated in the 141-152 GHz range. Apart from the frequency shift, the transceiver is fully operational and its functionality has been thoroughly verified.

A second version of the April 2011 chip was sent for fabrication at STMicroelectronics in February 2012 in order to retune the frequency of oscillation of the VCOs and center it at 122.5GHz. The dies were received in June 2012 and as will be presented in this report, the VCOs in the new version are correctly centered.

3.1 System Architecture

The system block diagram of the 122 GHz radar sensor is shown below:
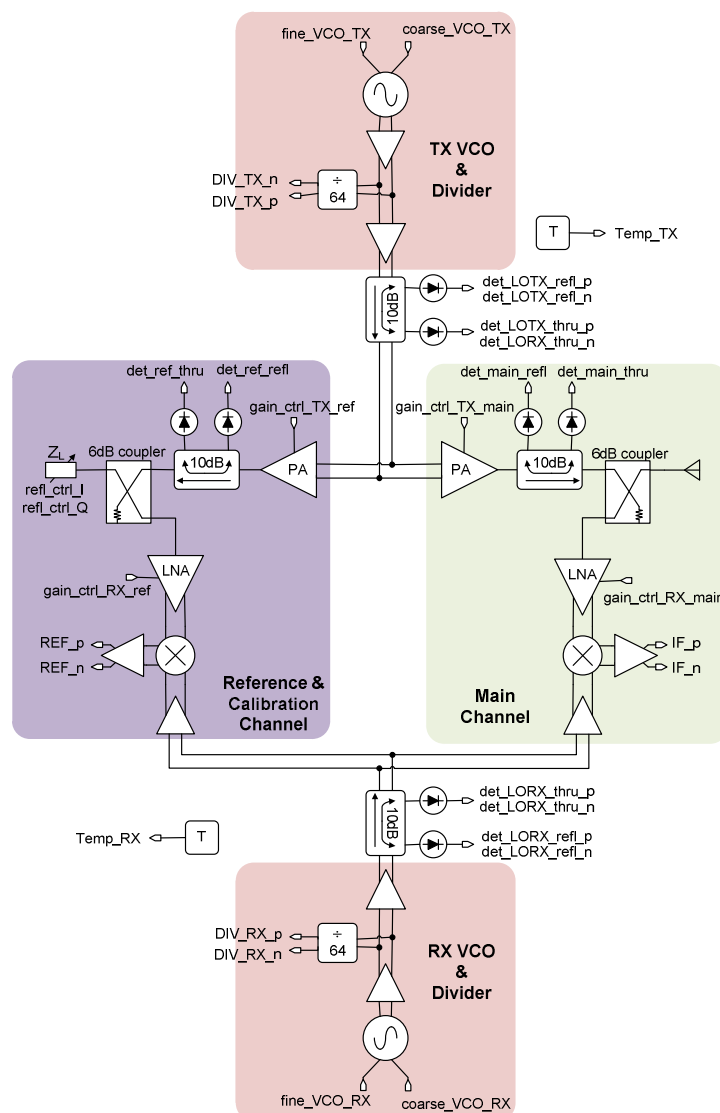
Figure 22: Radar Sensor Block Diagram

The system is based on a low-IF frequency plan achieved by using separate transmit (TX) and receive (RX) VCOs, which oscillate at frequencies f_{TX} and f_{RX} respectively. The signal generated by each oscillator is distributed to both the reference and the main channel using active power splitting. In both transceiver channels, the RX VCO signal drives the downconvert mixers while the TX VCO signal drives the power amplifiers.

In the main transceiver channel, the TX VCO signal is first transmitted by the antenna, reflected by a target whose distance is to be measured, and is received back by the same antenna. The 6dB coupler separates the transmitted from the reflected signal and steers the reflected signal to the receiver, which, in turn, downconverts it to the IF frequency $f_{IF} = f_{TX} - f_{RX}$. By comparing the IF outputs of the main and reference channels, any phase or frequency shifts between the transmitted and reflected signals can be resolved.

The reference channel is designed to be identical to the main channel that performs the actual measurement, but instead of being connected to an antenna, it is terminated on a variable impedance tuner. The equivalence between the main and reference channel minimizes any delay mismatch between the two, and thus capturing the round-trip delay to the target as accurately as possible. Furthermore, the impedance tuner can be used for self-testing and calibration as discussed below.

Several self-test features have been included in order to facilitate simple low-frequency, low-cost testing and thus minimize the use of D-band equipment:

1. Divide-by-64 divider chains have been introduced for both the TX and RX VCOs. Apart from allowing the VCOs to be locked by external PLLs, these dividers provide a low frequency (~2GHz) signal that can be used to independently verify the proper operation and tuning range of the VCOs.

2. Power detectors capable of monitoring both the forward and reflected power have been inserted between the RX LO distribution tree and the mixers, as well as between the TX LO distribution and the PAs. These detectors can verify whether adequate power is provided by the LO distribution networks and isolate potential problems in the mixers and PAs or in the VCOs. Furthermore, since the reflected power is monitored, the cause of potentially insufficient signal power can be traced back to improper matching or to inadequate VCO output power.

3. Power detectors were also placed at the PA outputs of both the main and reference channels. Apart from monitoring of the output power, the detector reading of the reflected power can be employed to estimate the reflection coefficient at the TX output and thus estimate how well the antenna is matched.

4. An impedance tuner was added at the output of the reference channel. This has been fabricated and characterized as a separate breakout and the values of its impedance states are known. By switching between different known impedance states, different amplitudes and phase shifts between the reference and IF outputs can be observed, thus verifying the proper operation of the reference channel. Furthermore, a one-port calibration using the known tuner

impedance states can be performed and the imperfections of the RF front-end (i.e. leakage, phase delays, etc.) can be estimated and calibrated out.

3.2 Circuit Design

This section provides the circuit schematics of the critical building blocks, designed in STMicorelectronics' production 0.13μm SiGeBiCMOS process (BiCMOS9MW). In cases where separate breakouts were fabricated and characterized separately using wafer probing, the corresponding measurement results are provided.

3.2.1 VCO

The schematic of the VCO is illustrated below:
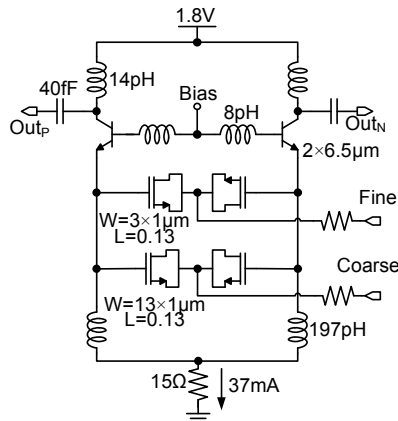
Figure 223: Schematic of the Colpitts VCO used in the April 2011 SUCCESS Sensor tapeout

The proposed Colpitts VCO consumes 40mA from 1.8V power supply. In order to achieve low voltage operation, as well as low phase noise, simple common emitter (as opposed to cascode) transistors are used to generate the negative resistance. The frequency is controlled by 0.13μm accumulation mode varactors which were preferred over p-n junctions due to their higher Q factor and lower control voltage.
A slightly different version of the VCO of figure 2 was previously manufactured and characterized both as a standalone breakout and as part of an earlier 122-GHz transceiver with a measured tuning range of 114.1 GHz – 123.7 GHz. In the April 2011 SUCCESS tapeout, some layout improvements and minor schematic modifications to the original VCO resulted in the shift of its tuning range to 143-152 GHz:
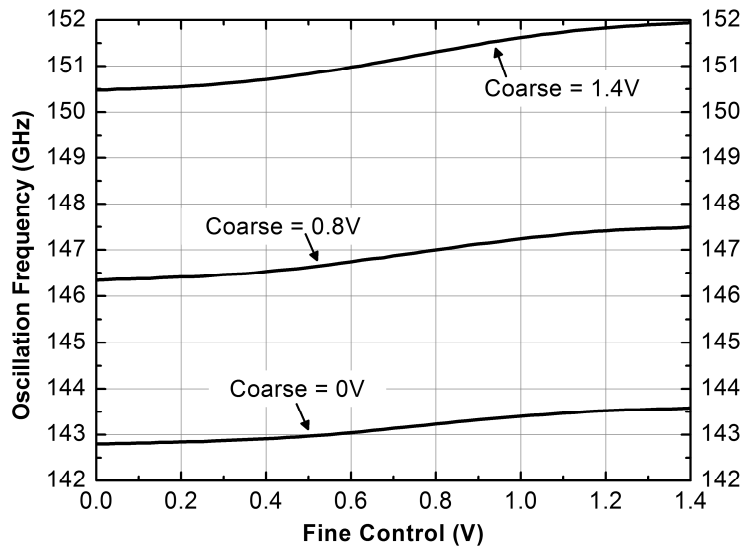
Figure 24: Tuning range of the April 2011 SUCCESS Sensor VCO

To circumvent this problem, the value of the tank inductance of the oscillator was increased appropriately and a new version of the radar sensor was taped-out on February 2012:
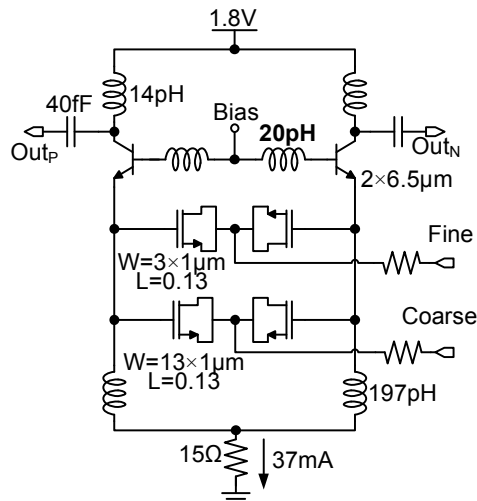
Figure 25: Schematic of the February 2012 version of the VCO.

After the fix, the VCO is centered in the appropriate 122.5GHz range:
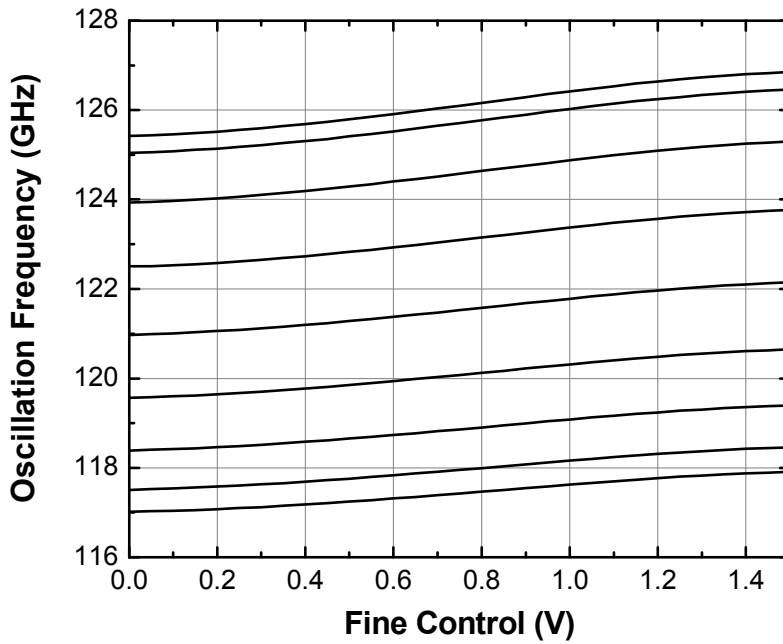
Figure 26: Measured tuning range of the February 2012 SUCCESS Sensor VCO

3.2.2 Divide-by-64 Divider Chain

The most criticalfirst stage of the divider chain employs a dynamic (Miller) divider architecture as illustrated below:
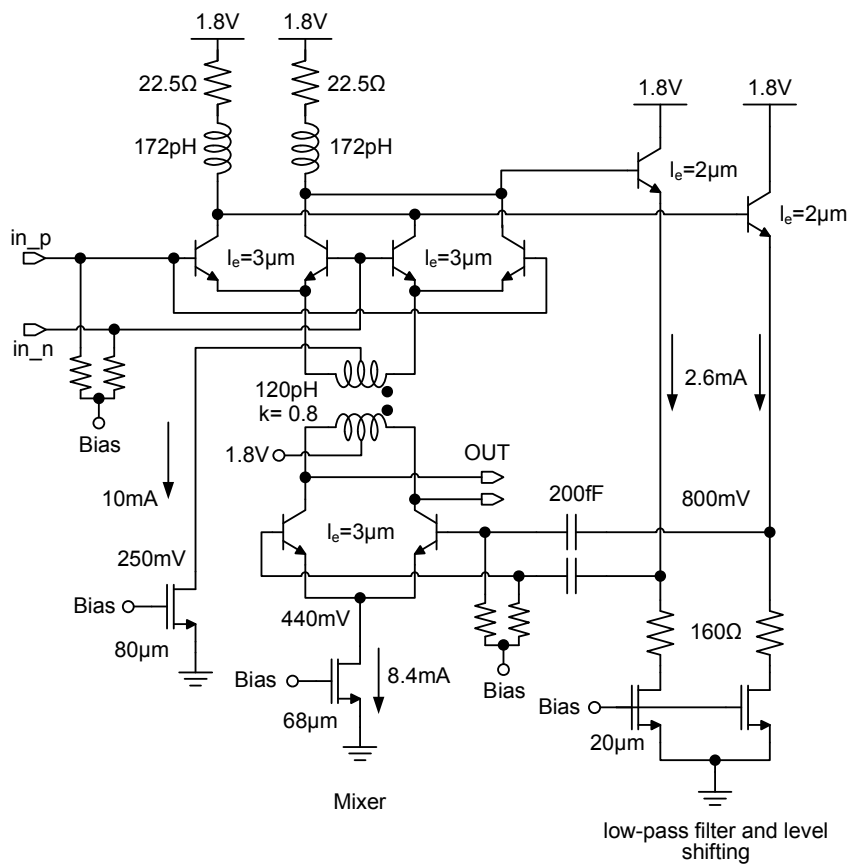
Figure 27: Schematic of the 120GHz Dynamic Divider

The divider mixer core is composed of a transformer-coupled Gilbert cell in order to maintain 1.8V operation. A pair of emitter followers, AC-coupled through capacitors to the mixer transconductors, provides low-pass filtering which is necessary in order to force the divider to generate half the input frequency at its output. The dynamic divider consumes 23mA from 1.8V power supply.

The remaining divider stages (from 60 GHz and below) are implemented using static dividers. The buffers which are necessary between the dynamic divider and the 60GHz static divider are implemented using CML inverters. The total power consumption of the divider chain is 120mW and it was fabricated and characterized as a standalone circuit, as well as part of the transceiver. When tested as a standalone breakout using a W-band (75GHz-110GHz) setup, the division range was found to be from 75GHz to 115 GHz (the maximum frequency the setup can support). In the transceiver, where the input was provided by the VCO and buffer chain, the divider chain was verified to divide properly up to 152 GHz.

3.3.3 Receiver

The 122-GHz receiver consists of a low noise amplifier followed by a double sideband Gilbert cell mixer and a 50-Ω IF buffer. The schematic of the 122-GHz receiver is illustrated below:
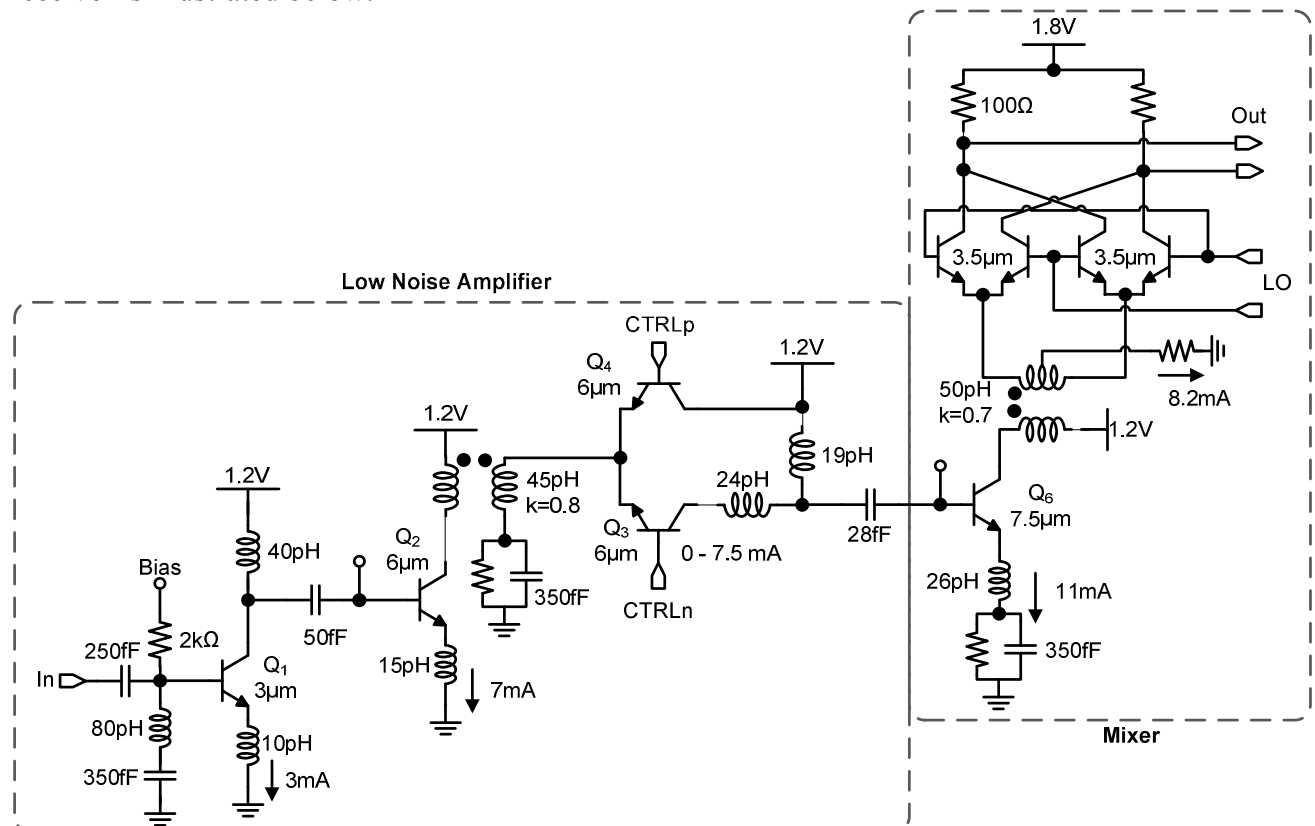
Figure 28: Receiver schematic

The 3-stage LNA provides low-noise matching to 50Ω as well as initial signal amplification. Gain control, necessary in order to ensure the overall linearity of the receiver, is achieved by steering current between the output common base transistor and a dummy, loadless, common base transistor.

The mixer employs an inductively degenerated transconductor which is transformer-coupled to the mixing quad. The transformer coupling is necessary in order to facilitate 1.8V operation, which would have been otherwise impossible due to lack of voltage headroom.

The simulated maximum downconversion gain, noise figure and IP1dB of the receiver are 15dB, 11dB and -21dBm respectively. The input compression power can be improved to -10dBmby taking advantage of the programmable gain feature of the LNA. This, however, results in approximately 4dB penalty in the noise figure of the receiver. The total power consumption of the receiver is 100 mW.

A breakout of the receiver was fabricated in the April 2011 run:
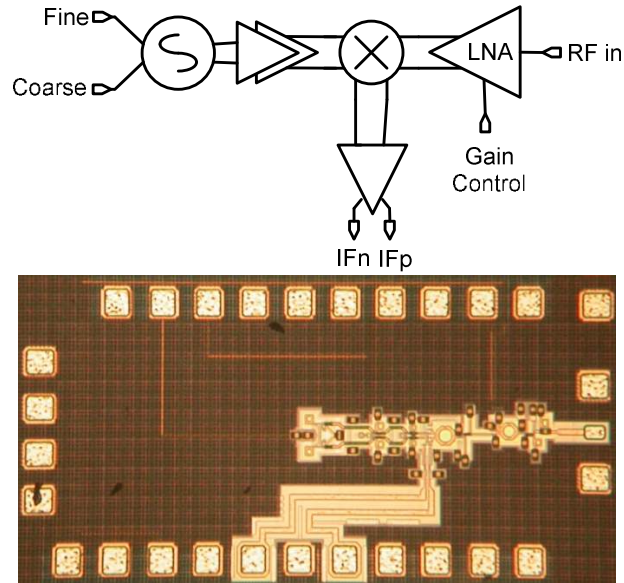
Figure 29: Receiver breakout block diagram and die photograph.

The gain and noise figure of the receiver were measured only in the 143 - 152 GHz range, limited by the tuning range of the VCO. The measurement results are reproduced in the figures below:
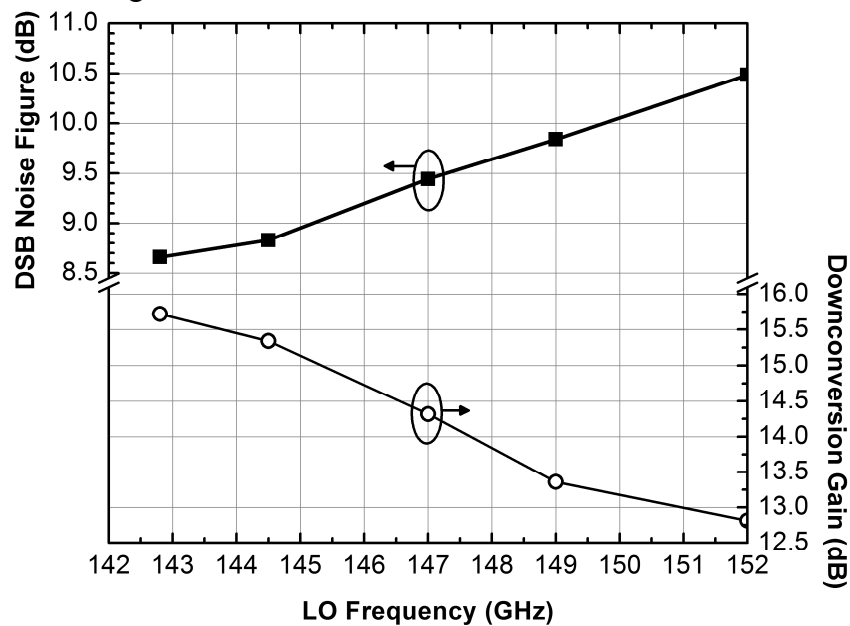
Figure 30: Gain and double sideband noise figure at a constant IF of 750 MHz versus LO frequency.
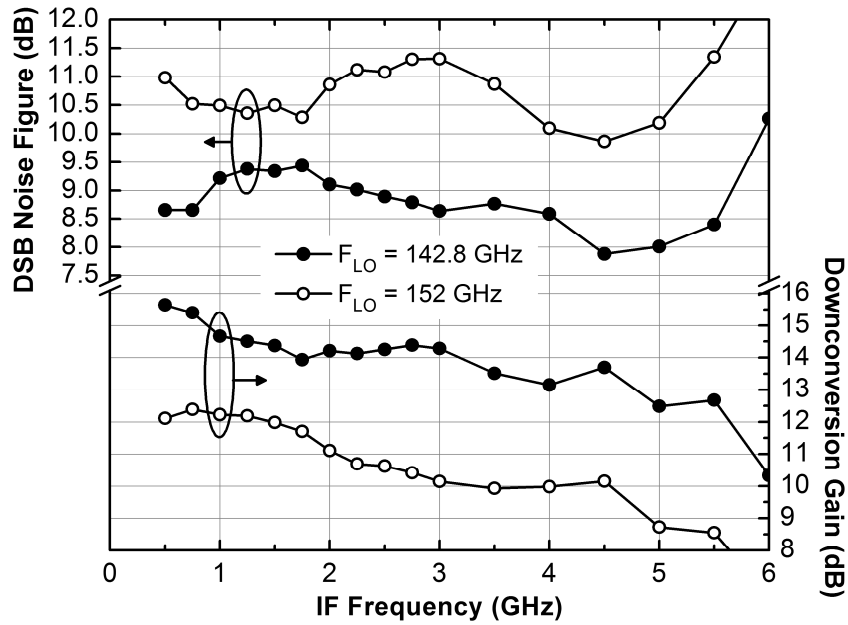
Figure 31: Gain and double sideband noise figure at constant LO frequency versus IF frequency. Deembedding of the mm-wave setup is performed at the LO frequency at and is increasingly inaccurate at higher IF frequencies

3.2.4 LO distribution

The figure below shows the LO distribution network:
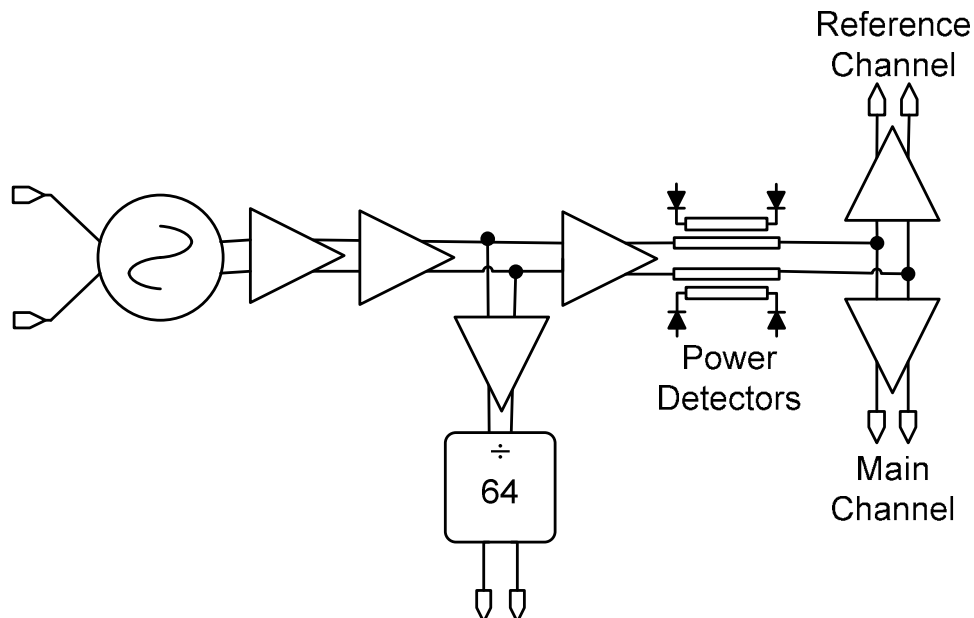
Figure 32: Schematic of the LO distribution network.

In order to provide adequate LO signal amplitude at the inputs of the two mixers and dividers, a chain of common-emitter buffers was inserted between the VCO and these blocks.

To ensure LO tree operation from 1.8V, and to avoid stability problems, common emitter buffers were preferred over cascode. Furthermore, bias stability, common

mode stability, and common mode rejection are ensured by inserting series R-L networks in the tail current sources of the differential amplifiers:
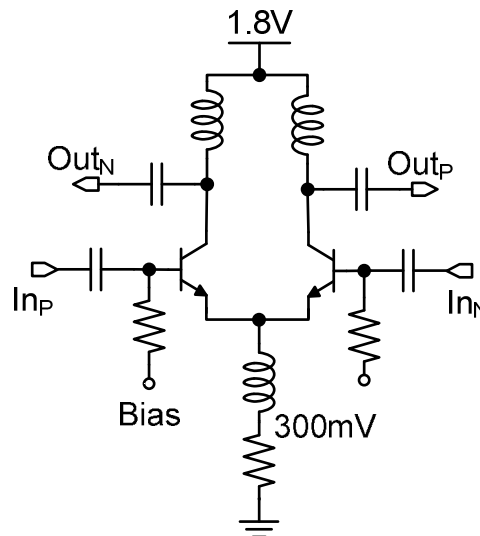
Figure 23: Schematic of the common emitter buffer used in the LO distribution network.

3.2.5 Power Detector

The schematic of the bidirectional power detector is illustrated below:
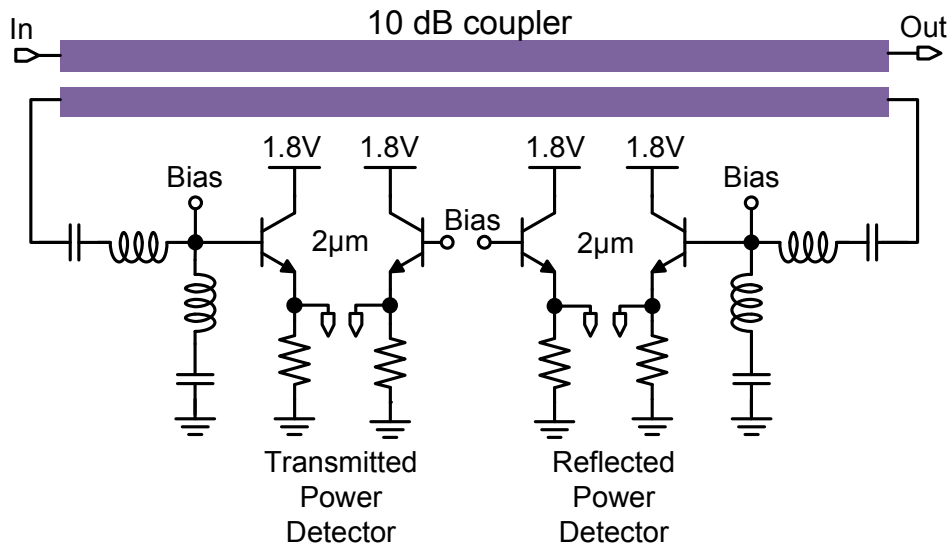
Figure 34: Schematic of the power detector

The power detector is based on a 10-dB coupled-line directional coupler whose coupled outputs are terminated on bipolar transistors that exhibit rectifying action in their base-emitter junctions. The coupled-line coupler was preferred to ring hybrids as it features wider bandwidth and more compact size. A coupling ratio of 10-dB was selected in order to minimize the loss that the power detector will introduce in the signal path. The bipolar transistors were biased at lower than peak-f_T current density that maximizes the responsivity.

A separate breakout of the bidirectional power detector was fabricated and characterized in order to assess its performance. The figure below shows a die microphotograph of the breakout along with the measured S-parameters:
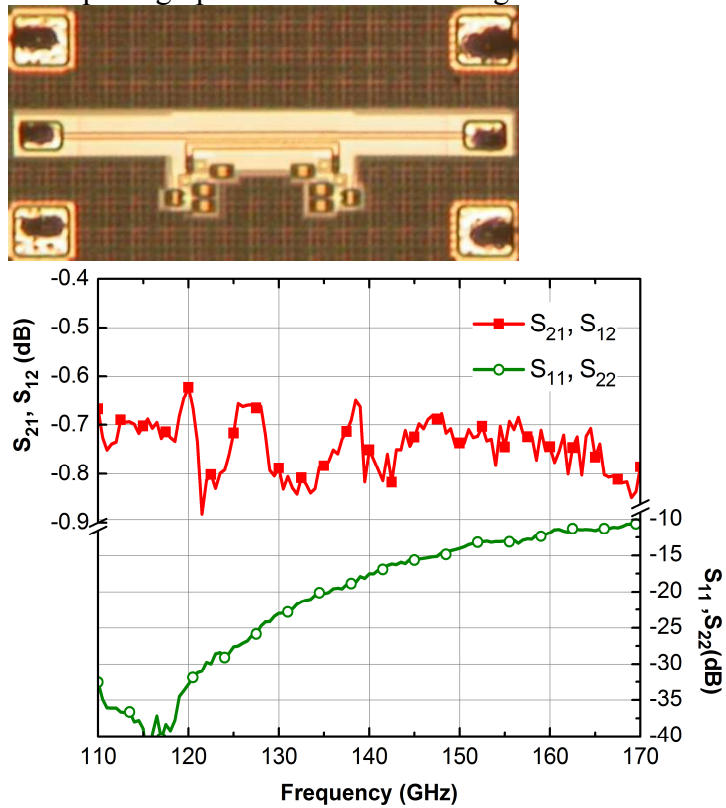
Figure 35: a) Die photograph of the directional couplers with detectors and b) Measured S-parameters.

The figures below reproduce the measured Vout-Pin behavior of the power detector at 122GHz and 145 GHz:
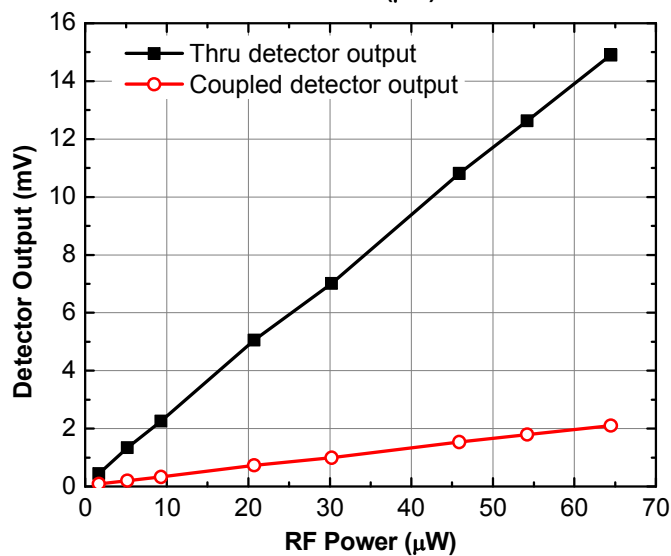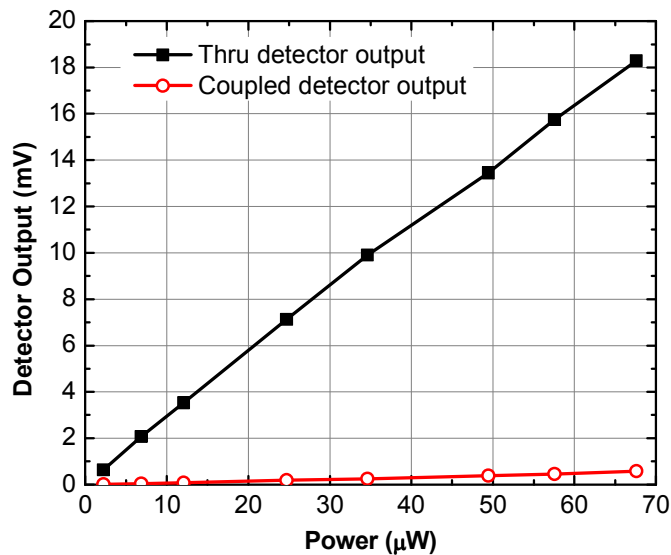
Figure 36: Vout-Pin characteristics at (a) 122GHz and (b) 145 GHz

3.2.6 Power Amplifier

Due to the relaxed output power requirements of the system (output power of 0dBm) no high power amplifier is required. Instead, the low noise amplifier is utilized as a medium power amplifier at the output of the two transmitters. The programmable gain feature of the LNA can be also utilized in the power amplifier for output power control.

3.2.7 Programmable load

An arbitrary, complex reflection coefficient around the center of the Smith Chart can be obtained using the following circuit:
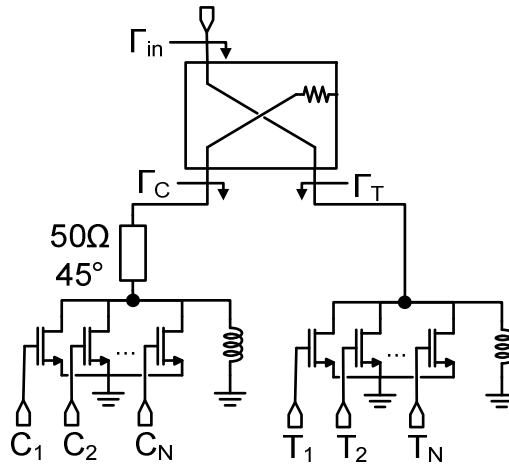
Figure 24: Realization of the programmable load with NFETs

The MOS transistors act as two state (on/off) resistors, since their parasitic capacitance is tuned out by the shunt inductor. The 45 degrees transmission line rotates Γ_C by 90 degrees, rendering it purely imaginary, as opposed to Γ_T which assumes only real values. As a result, the reflection coefficient at the input of the coupler becomes:

$$\Gamma_{in} = \Gamma_T + j\Gamma_C$$

which maps to a square whose center is the center of the Smith chart as Γ_C and Γ_T vary from 0 to 1.

An impedance tuner with 4 Γ_T and 4 Γ_C bits was designed and characterized as a separate breakout. The figure below reproduces the measured reflection coefficient Γ_{in} at 122 and 146 GHz for the different impedance states
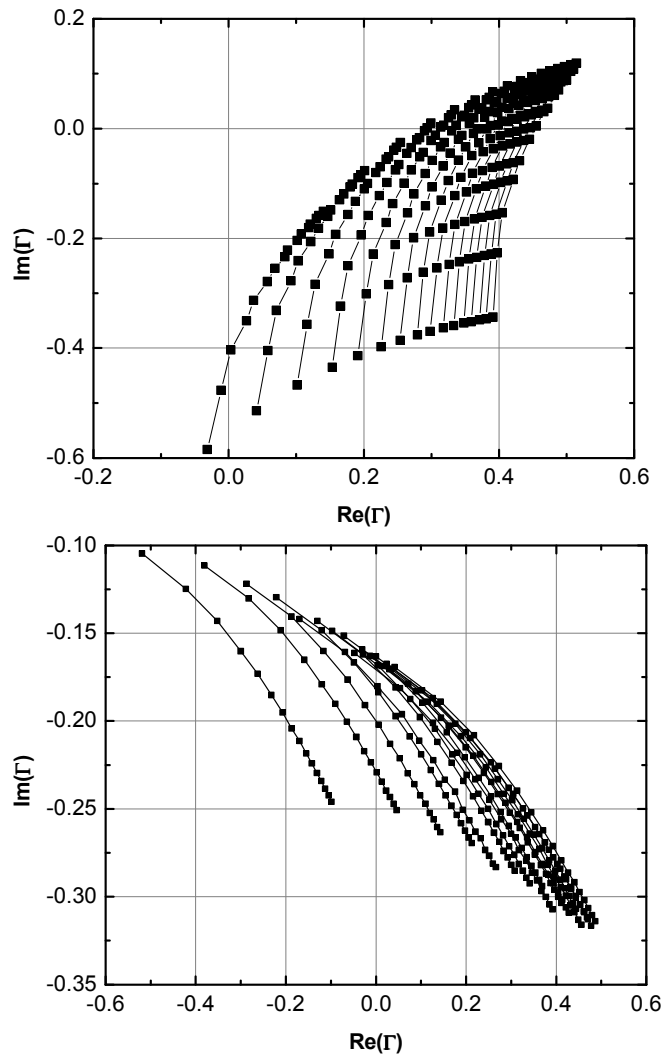
Figure 38: Measured Γ_{in} at (a) 122 GHz and (b) 146 GHz

3.2.8 Digital gain control

The programmable gain in the LNA and PA was realized in a digital fashion by using the control circuit illustrated below:
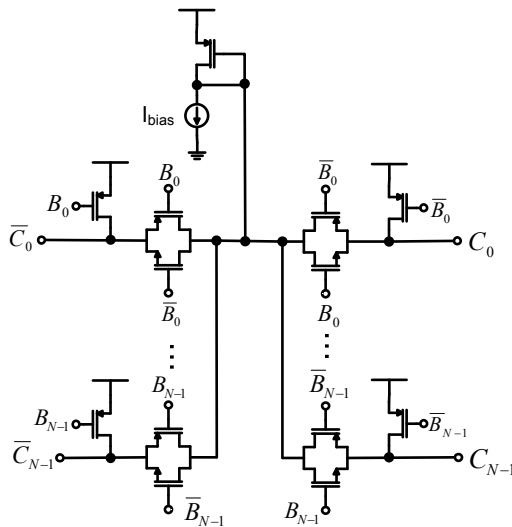
Figure 39: Schematic of the current source control circuits

The thermometer coded bits B_0, …, B_{N-1} control an array of transmission gates, which in turn, charge their output nodes C_0, …, C_{N-1} either to V_{bias}if B_N is a logic "1" or to 1.8V, if B_N is a logic "0".

Next, the signals C_0,…, C_{N-1} turn on or off the PMOS current sources in the circuit illustrated bellow:
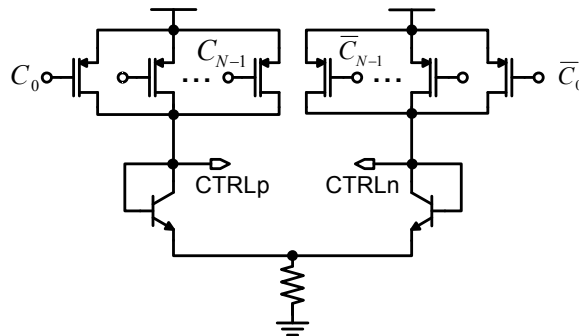
Figure 40: Schematic of the programmable current source

and as a result, controlling the total amount of current that flows though the corresponding bipolar current mirrors.

In order to read out the analog signals generated by the on-chip circuits (power detectors, temperature sensors etc.) and minimize the number of pads required for this process, the analog mux below was employed:
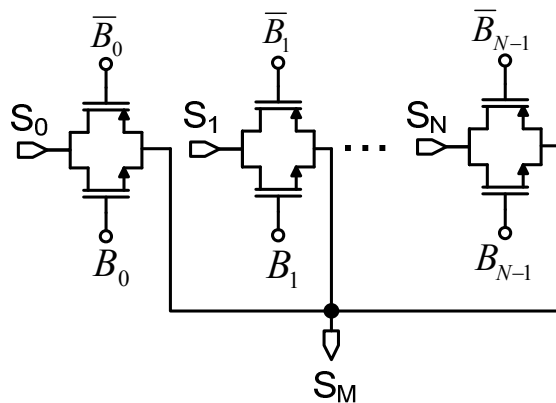

Figure 25: Analog MUX

The analog signals S_0, S_1, ... S_N are connected to the same output S_M through CMOS transmission gates. When S_N is to be read, the corresponding transmission gate bits B_N are set while the remaining gates are off. The correct toggling of only one transmission gate is assured by using a one-hot decoder to generate bits B_0, B_1, ... B_N. The analog mux allows all the analog signals to be read by off-chip equipment sequentially.

The control bits required by the above circuits are inserted in the chip thru a simple shift register that requires 3 control signals: Din, RESET, and Clock and an optional Dout signal.

3.3 Transceiver Characterization

The April 2011 transceiver chip was mounted on a QFN package and a PCB was designed by R. Bosch:
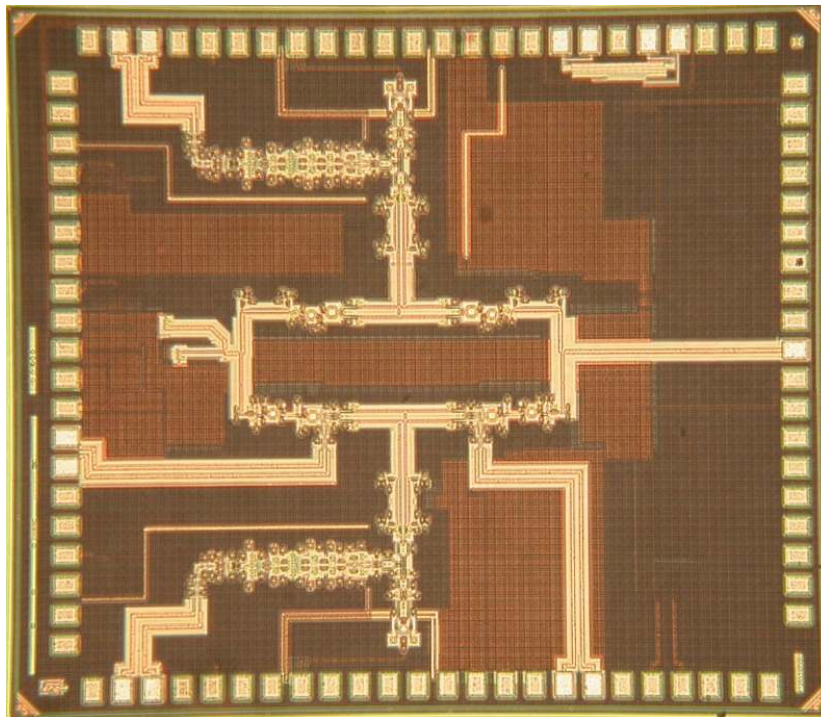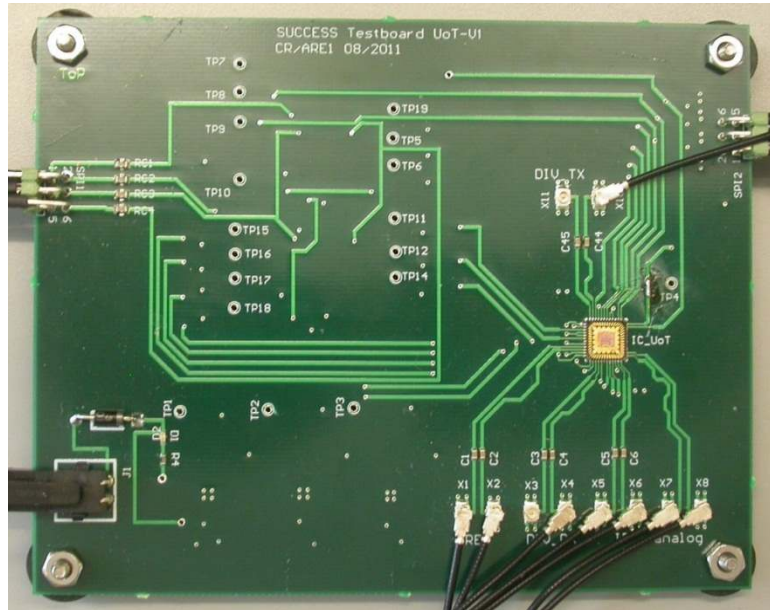

Figure 42: Die microphotograph

Figure 43: Transceiver QFN package and PCB

This method facilitates simple characterization and verification of the chip functionality using the Built-in Self-Test. The PCB was also fitted in a probe station and the antenna port of the transceiver was probed using D-band probes in order to further verify the operation of the chip.

The proper operation of the VCOs was first verified by checking the divider outputs. Subsequently, the LO tree power detectors were recorded and translated into power by using the measured Pin-Vout characteristics of the standalone detector:
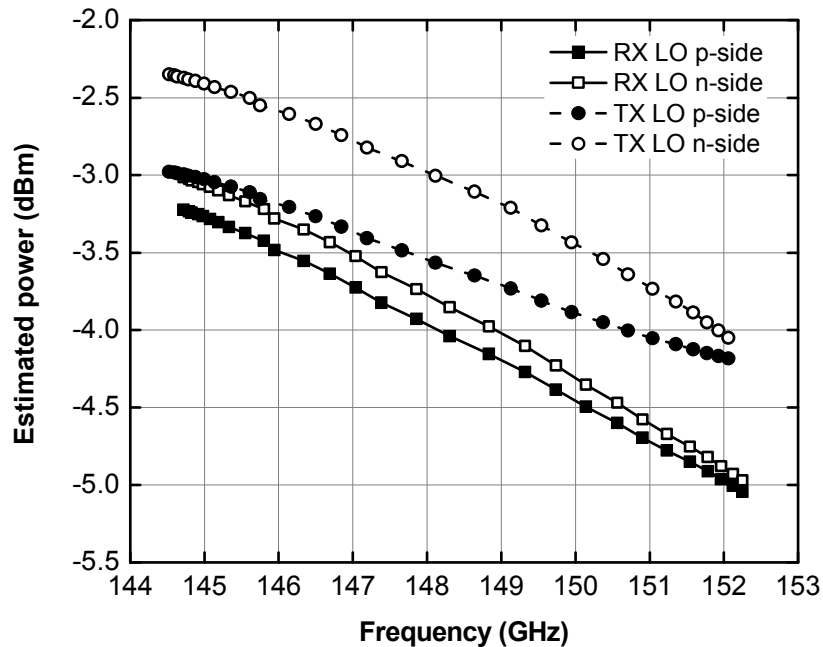

Figure 44: Power provided by the LO trees

The power levels of figure 26 indicate that the desired adequate power reaches the receiver mixers and transmitter power amplifiers to ensure their proper operation. Slight differential asymmetry of about 0.7dBwas detected from the TX detectors whose source has not been identified, but it is small enough not to impact the transmitter operation.

The output power of the chip was measured using both the on chip power detectors as well as by probing the antenna port of the chip and using an external ELVA-1 power sensor:
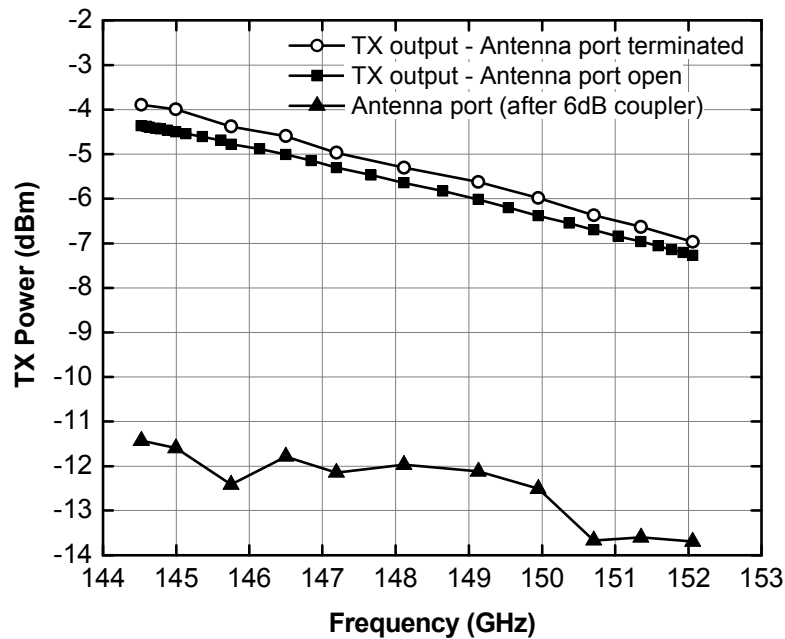

Figure 45: Measured Output Power

The measured power at the antenna port is consistent with the on-chip power sensor readings since 7-8dB loss between the PA output and the antenna pad are expected due the 6-dB coupler as well as the corresponding interconnect.

The capability to adjust the output power was verified using the on-chip power detectors as well as by monitoring the TX-to-RX leakage signal through the 6-dB antenna coupler:
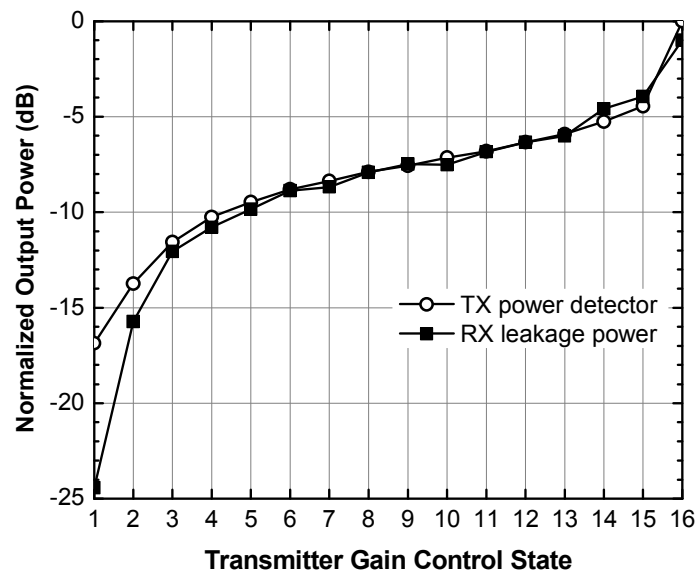

Figure 46: Transmitter output power control

The two measurements track each other and indicate that there is over 15 dB of output power control.

Similarly, the RX gain control steps were characterized by employing the TX-to-RX leakage and measuring the change in the received signal output power:
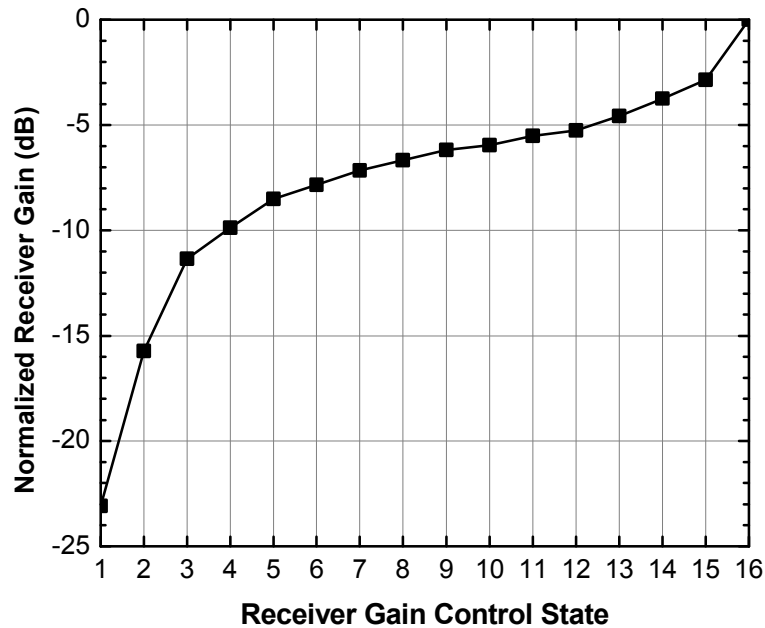

Figure 47: Receiver Gain Control

Finally, the on-chip tuner was used to verify that the transceiver is indeed sensitive to reflection coefficient variations. For this purpose, the main channel was used as the reference and the output of the reference channel was monitored for changes in amplitude and phase. The figure below illustrates the reflection coefficient of several tuner states, as measured by the chip, compared with the corresponding measured states of the standalone tuner. Furthermore, a one-port calibration with 4 error terms was applied using 3 states. After applying the corrections, the reflection coefficients measured by the chip are almost identical to those of the standalone tuner.
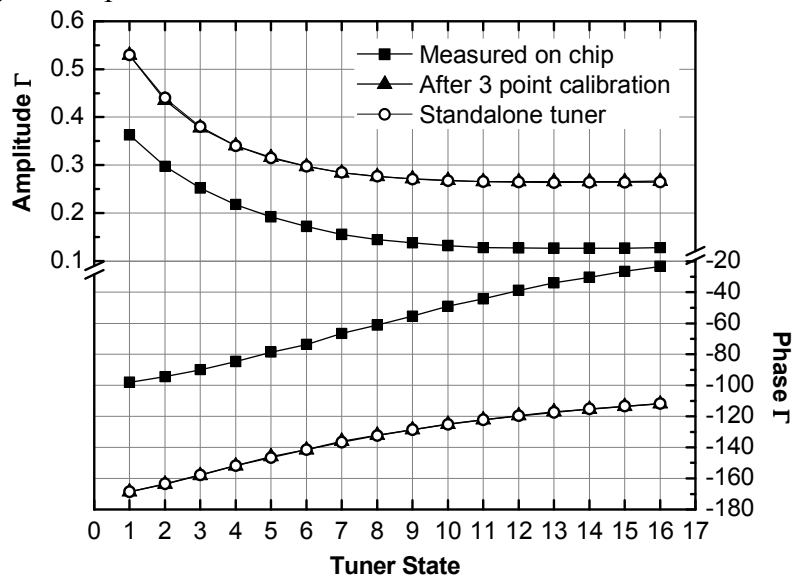

Figure 48: Raw and calibrated reflection coefficients.

3.4 Conclusions

Two transceiver chips were designed by the University of Toronto. The first one was taped out on April 2011 and operated in the 141-151 GHz frequency range. This chip has been mounted on a simple QFN package and its functionality has been verified. A second chip was taped-out on February 2012 and its frequency range of operation was measured to be 117 – 127 GHz.