Silicon-based Ultra Compact Cost-efficient System Design for mmWave Sensors “SUCCESS”

Deliverable
D4.3

Mm-wave SoC Front-end (V1) test report

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Abstract

This document describes the development of the first version frontend ICs and their building blocks. Three versions Front-end ICs have been designed and fabricated, direct-down transceivers with fundamental and sub-harmonic mixing, and a finite-IF transceiver.

Keywords
mm-wave sensor, SoC, 122 GHz radar, single chip transceiver, build-in-self-test (BIST), design for test (DFT), SiGe BiCMOS

1. Introduction

According to the system specification of D2.3, the transceiver architectures that can fulfill the specification have been reported in D4.1. Two transceiver frontend have been investigated in D4.1, one is a direct-down ZIF frontend and the other is a finite-IF transceiver frontend. This report will describe the finalized building block diagrams of the two frontends, and the designs of these building blocks and the measurement results.

For the ZIF frontend, two versions of chipsets have been designed and fabricated, one is fundamental frontend and the other is a sub-harmonic frontend. In sub-harmonic frontend, a 61 GHz push-push VCO is used and the VCO output is split into two paths to drive a passive sub-harmonic mixer and frequency doubler. The frequency doubler by itself can deliver enough power to antenna so that the 122GHz PA is omitted. In the fundamental mixing chipset, a 122 GHz push-push VCO is used. This signal is split into two paths to drive the 122 GHz PA and an active mixer. These ZIF transceiver chipsets also include a frequency ramping generation unit. The frequency ramping unit is a mixed signal design including digital cells and analog building blocks. Separate pads are used at the divider output and VCO input so that an external PLL can also be used in case of a different modulation scheme is required.

In the finite-IF chipset, the previous reported architecture is used. Mm-wave BIST and DFT circuit blocks have been added to the transceiver system.

2. ZIF transceiver frontend with sub-harmonic mixing scheme

2.1 Building blocks

The building block diagram of the subharmonic frontend is shown in the dashed box in figure 1. In includes 60GHz push-push VCO with divider, a 60GHz drive amplifier, a 122GHz frequency doubler, a two directional power detector, an 122GHz LNA, a 122GHz passive 90 degree couple, two passive sub-harmonic mixers, two IF VGAs and a frequency measurement unit.

The building blocks have been designed, fabricated and measured before integrating into a single chip.

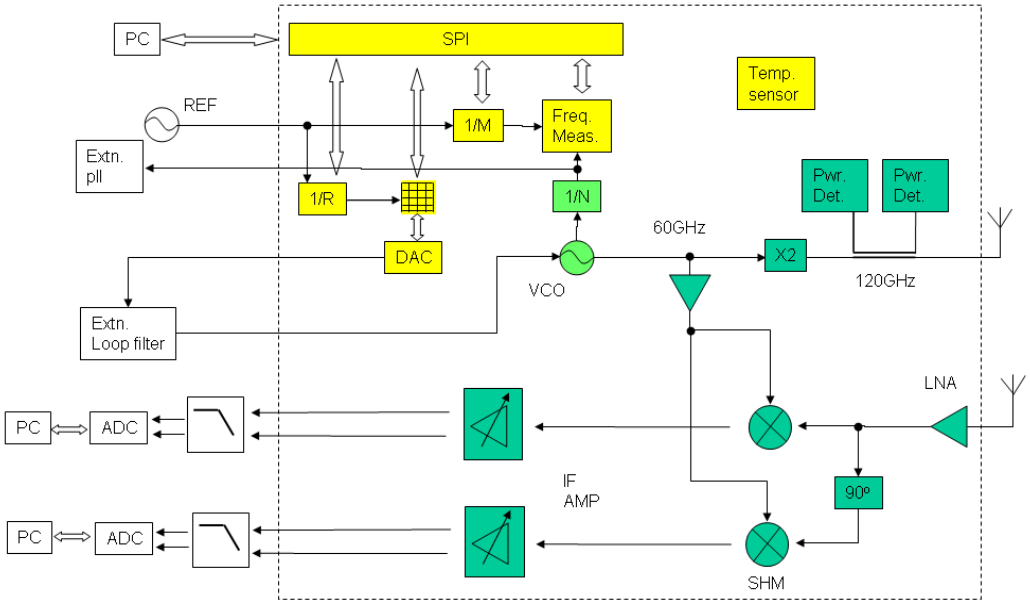


Figure 1. ZIF 122 GHz Transceiver architecture with harmonic mixing scheme.

2.1.1 122 GHz frequency doubler

The simplifed schematic of the 122 GHz frequency doubler is shown in figure 2. A 2nd order generator is realized by a pair of HBTs connected at their collectors and emitters. A common base stage is connected on top of the 2nd order generator to amplify the 122 GHz signal. Its input is matched to 61GHz through a passive transformer and its output is matched to 122GHz to drive the transmitter antenna. The chip photo is shown in Figure 3. It occupies a chip area of 0.45 mm^2 with pond-pads and 0.18 mm^2 without bond-pads.

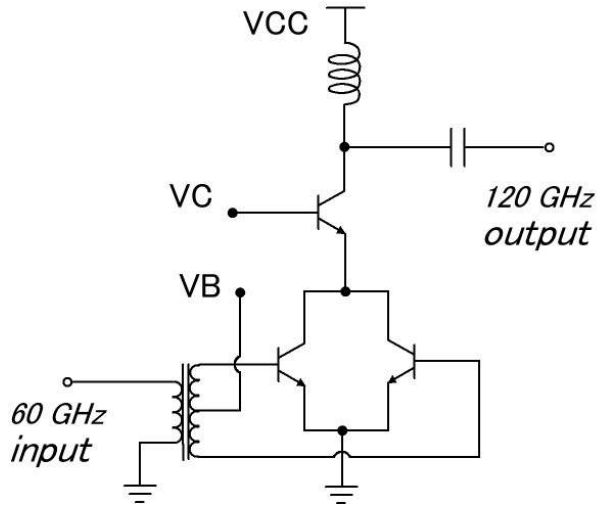


Figure 2. Simplified Schematic of the 122 GHz frequency doubler (*EuMIC 2011*).

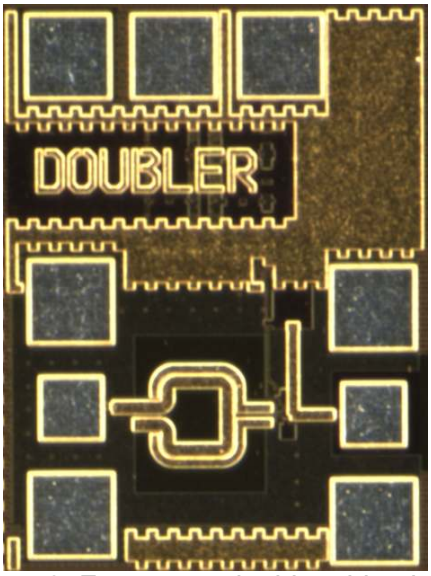


Figure 3. Frequency doubler chip photo.

The fabricated frequency doubler has been measured on-wafer on a probe station. Its 120 GHz output power versus 60 GHz input power is shown in figure 4, where the DC supply voltages were set to 2.0, 2.5 and 3.3 V respectively. With the input 60 GHz power higher than 2 dBm, the 120 GHz output power is all above 3 dBm thanks to the output common base amplification. For DC supplies of 2.5V and 3.3V, the 120GHz output saturated at 5dBm which eliminates the use of an extra 120GHz PA. The simulated output power for the typical DC supply of 2.5V is also shown in figure 4 for comparison. Its simulated output power is somewhat 1dB higher than the measured results. In figure 4 we can also find the collector current versus input power for the above mentioned DC supplies. With the increase of input power, the current also increases in the way similar to a class AB amplifier. For typical 2.5V DC supply, the collector current saturates at 27mA.

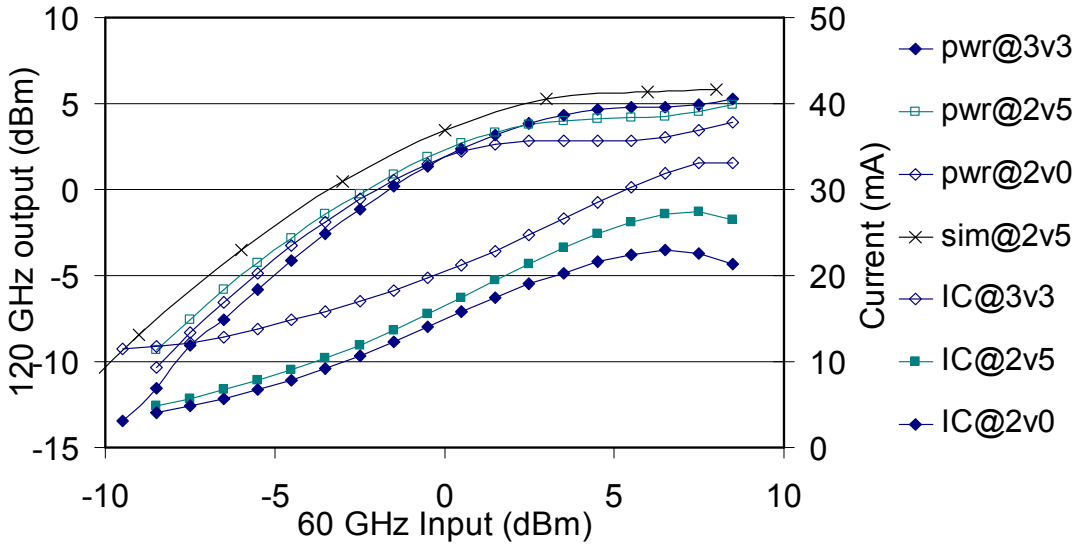


Figure 4. Measured and simulated output powers and their corresponding measured DC currents.

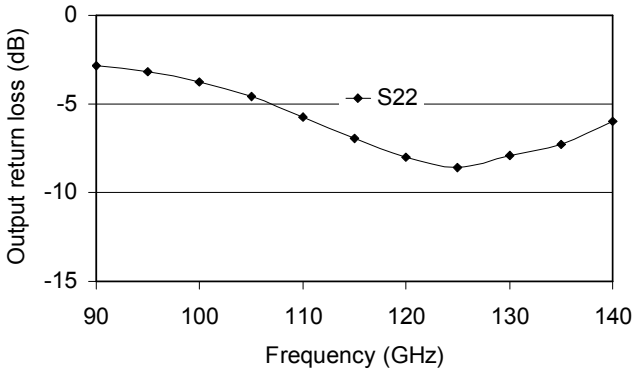


Figure 5. Output matching measurement of the doubler.

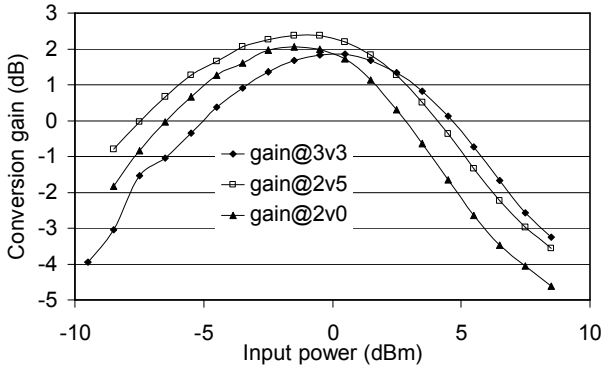


Figure 6. Measured conversion gain of the doubler for different DC supplies (61GHz input, 122GHz output).

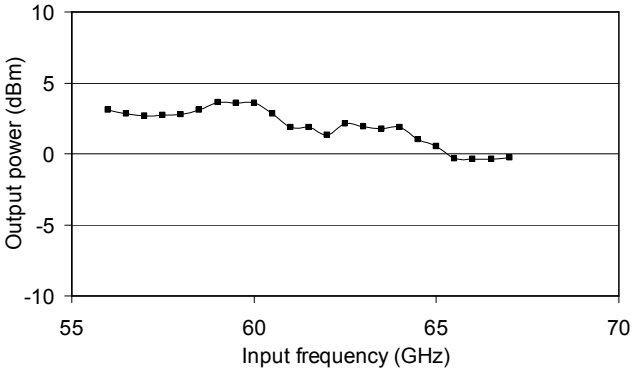


Figure 7. Doubler output power at different input frequencies.

Figure 5 shows the output matching of the doubler. Output S22 is about -7dB at 122GHz. Figure 6 shows the measured conversion gain from 61GHz to 122GHz. The measured conversion gain is about 2dB at around 0dBm input power. This is the biggest advantage of active frequency doubler compared to passive diode frequency multipliers. The peak conversion gain is 2.5dB at 2.5V DC supply with 0dBm input power. Figure 7 shows the frequency response. With input signal swept from 56GHz to 67GHz, the measured output variation is below 3dB.

2.1.2 Two-directional power detector

Figure 8 shows the simplified schematic of the 122GHz power detector, which is a standard Gilbert cell with its two inputs tied together. Small transistors are used to save power since the output is to drive a high impedance ADC. Its chip photo is shown in figure 9, where the directional coupler has coupling factor of -17dB. Two power detectors are used in at the two side of the directional coupler to detect both the forward and backward signal in order to minimize the insertion loss. However in this scheme we need to match the input of the two power detectors to the coupler output characteristic impedance in order to get rid of the reflections. Its measurement results are shown in figure 10 and 11. In figure 10, the output is loaded with a 50 ohm probe. We can see the backward and forward voltages are different in one order of a magnitude implying that the output matching is better than 20dB. Figure 11 is the output measurement with output open (probe tip lifted). We can see both of forward and backward output powers are following the same curve with respect to input power implying 100% of the power is reflected back. Due to the loss of the output matching structure, the reflected power did not reach the same level as the forward power. In figure 11, the loss the output matching structure has been calibrated out. Detailed information of the frequency doubler and the power detector can also be found in EuMIC2011 (European Microwave Integrated Circuit 2011) with the paper titled 'An Integrated Harmonic Transmitter Front-End for 122 GHz FMCW/CW Radar Sensor'.

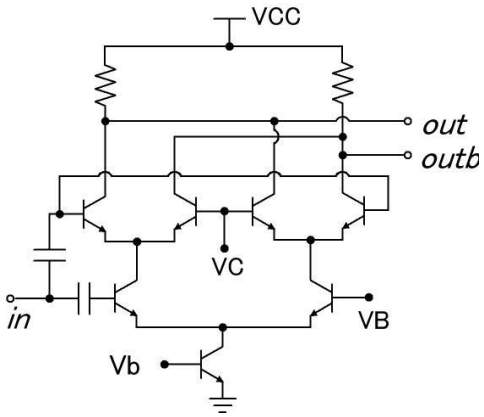


Figure 8. Simplified power detector schematic.

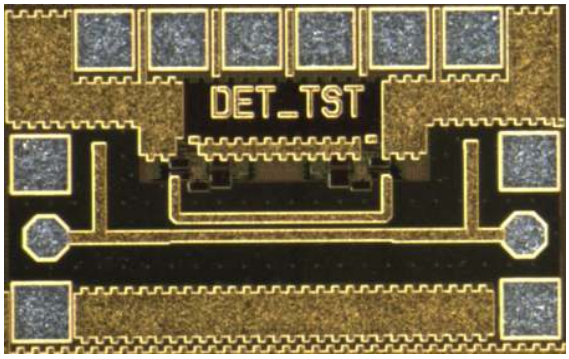


Figure 9. Chip photo of the two-directional power detector.

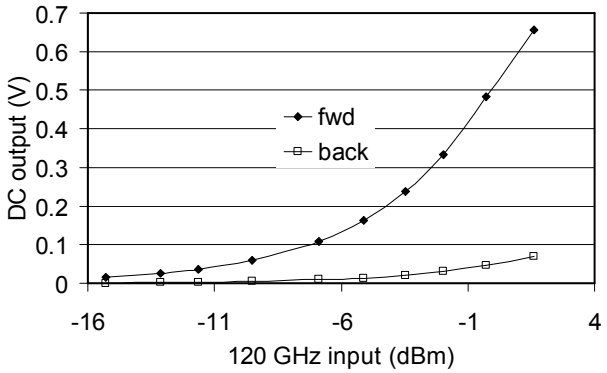


Figure 10. Detector measurement with output matched.

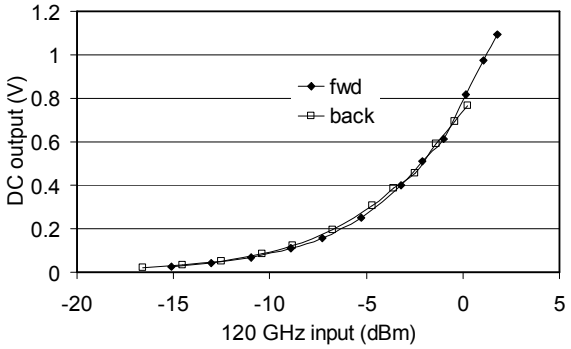


Figure 11. Detector measurement with output open.

2.1.3 60 GHz drive amplifier

A cascode 60 GHz driver amplifier has been designed, which occupies an area of 0.08 mm^2 excluding bond-pads. Its small signal S-parameter measurement is shown in figure 12, where the measured gain is about 13.5dB. Its input and output return losses are -12dB and -5dB, respectively.
With a typical 3.3 V DC supply, the output power has been measured for different DC biasing conditions. Figure 13 shows the output power measurement results with DC current changing from 13mA to 30 mA. Its highest 1dB compression point is 14dBm.
Figure 14 shows the PAE measurement results. At all current settings, the measured peak PAEs are above 27%. The highest PAE of 29.2% is achieved at 26mA biasing current corresponding to a 15dBm output power. Compared with all published 60GHz PAs in all silicon technologies, this driver amplifier has achieved the highest PAE and moderate output power.

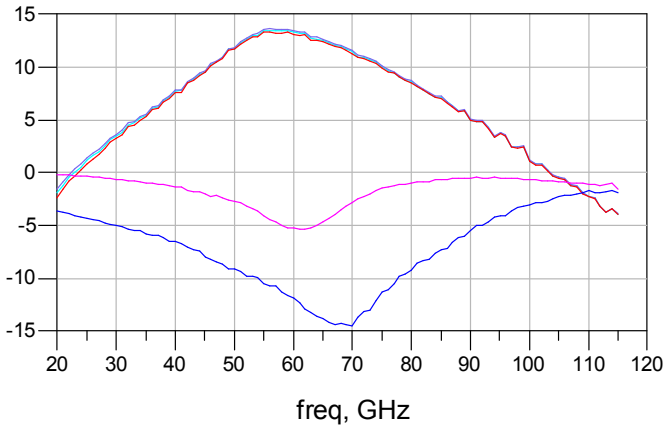


Figure 12. Small signal measurement of the 60GHz driver amplifier.

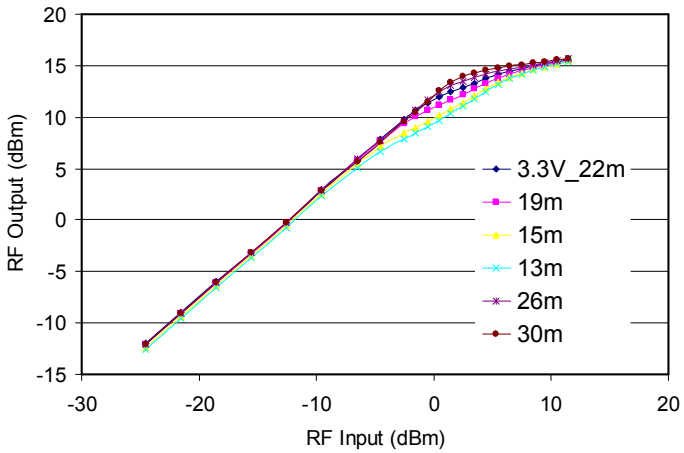


Figure 13. Output power measurement of the 60GHz driver amplifier at different biasing currents.

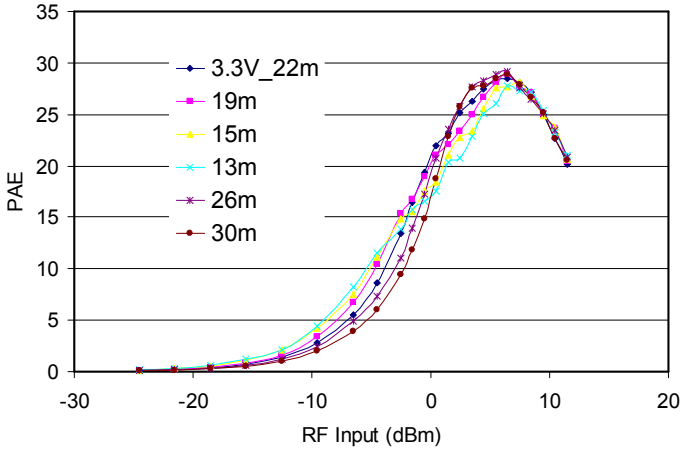


Figure 14. PAE measurement of the 60GHz driver amplifier at different bias currents.

2.1.4 122 GHz low noise amplifier

Figure 15 shows small signal measurement results of the designed 122 GHz LNA. Its core features a single stage cascode topology. The introduction of this LNA reduces

the receiver linearity. The purpose of this LNA is to reduce noise figure of the LNA. Therefore high gain is not desired. Figure 16 shows the linearity measurement of the LNA. It has a gain of around 10 dB and input P1dB is -5dBm.

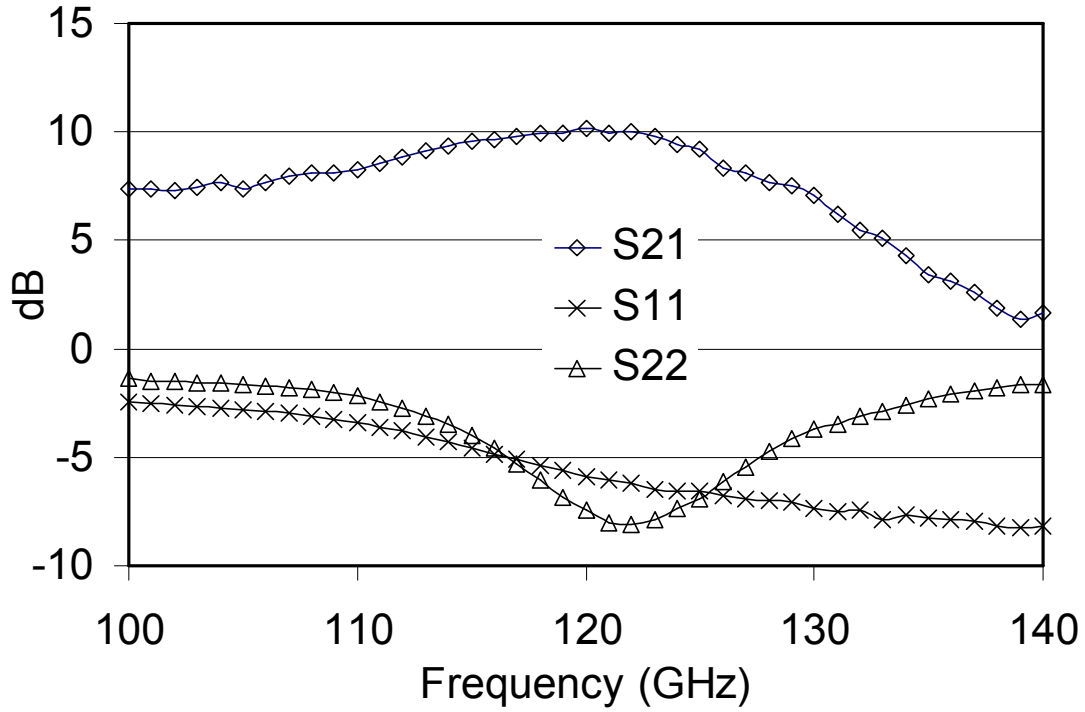


Figure 15. S-Parameter measurement of the 122GHz LNA.

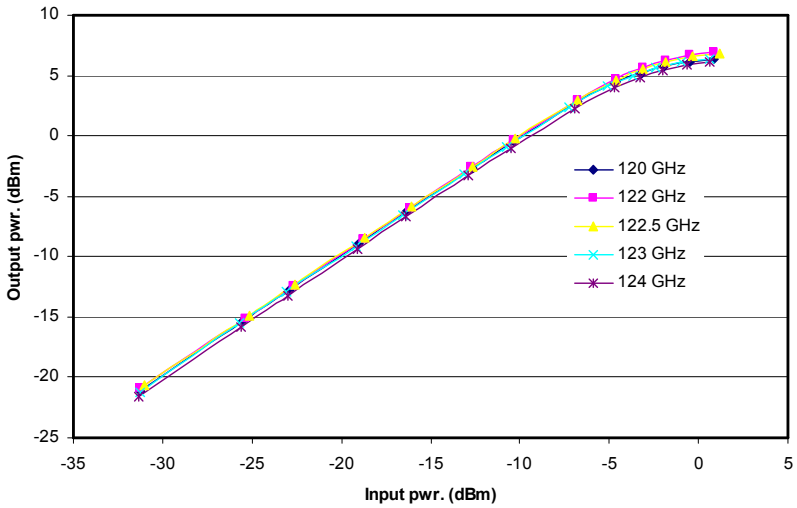


Figure 16. Linearity measurement of the 122GHz LNA.

2.1.5 Sub-harmonic mixer

An anti-parallel diode pair (APDP) is used to achieve sub-harmonic mixing. These diodes are realized by HBTs with base and collector tied together. The advantage of passive diode mixing is the higher linearity and reasonable noise figure. Plus passive mixers are less sensitive to 1/f noise which is proportional to the collector current. The sub-harmonic mixer core is shown in figure 17, which is a modified version from conventional APDP diode mixers. This mixer features single-ended RF and LO input but with fully differential IF output. Figure 18 shows the chip photo of the two fabricated passive sub-harmonic mixers, one is pure passive mixer and the other one has an IF output buffer.

For the pure passive mixer its measured conversion gain is shown in figure 19, where the peak conversion gain of -8dB is achieved at an LO power of 5dBm. Simulation shows similar results. The conversion gain with IF buffer is also plotted in figure 19. From 2 to 5dBm LO power, the conversion gain is 10dB together with an IF buffer. The pure passive mixer has a measured input P_1dB of -5dBm as shown in figure 20. The one with an output buffer has a -6dBm input P_1dB. The frequency response of the mixer with buffer has measured as shown in figure 21, where IF frequency is fixed at 1MHz and RF and LO powers are swept simultaneously. The measured 3dB bandwidth is from 117 to 124GHz. In figure 21, RF port matching, LO leakage, LO matching, 2nd LO harmonic leakage and noise figure are also plotted. Notice that except conversion gain, all other measurements are the results of the purely passive SHM.

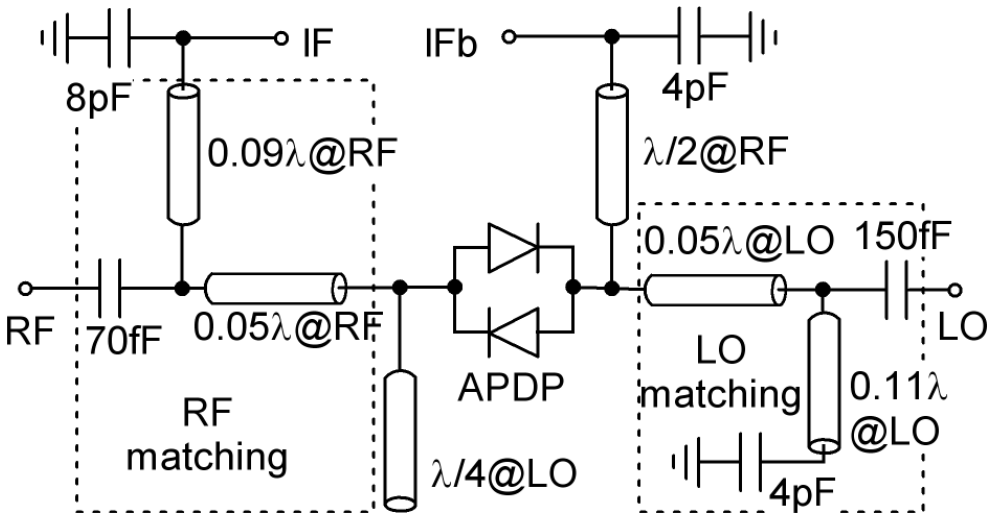


Figure 17. Schematic of the differential passive sub-harmonic mixer (accepted by *Microw. Wireless Compon. Lett.*).

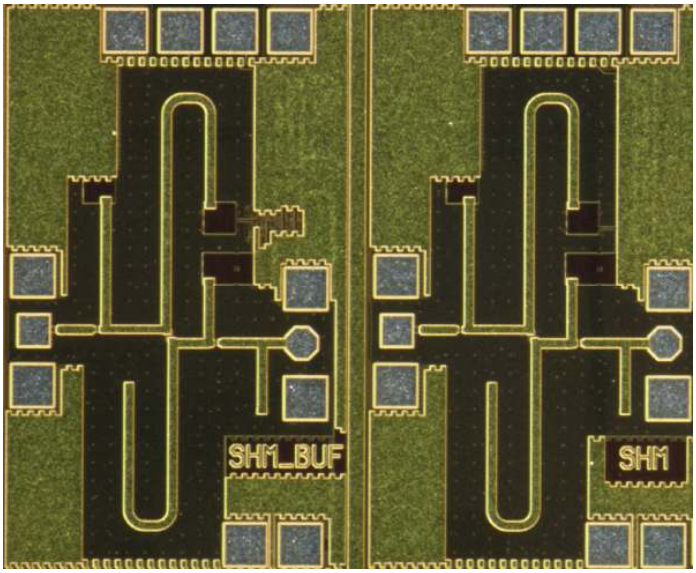


Figure 18. Chip photo of the SHM (left with output buffer, right without output buffer).

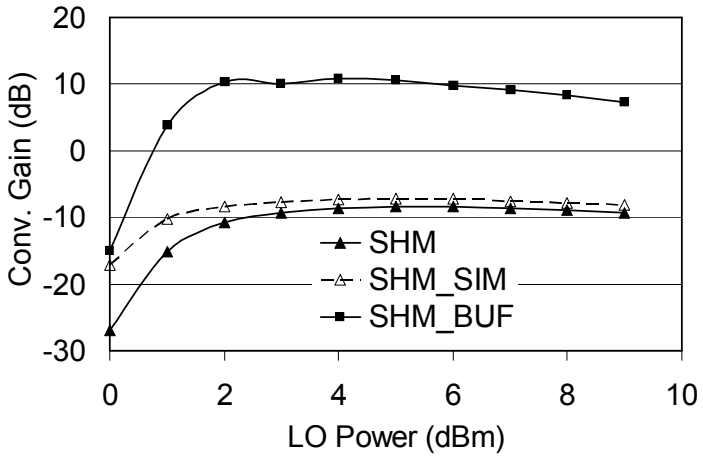


Figure 19. Measured conversion gain of the pure passive SHM.

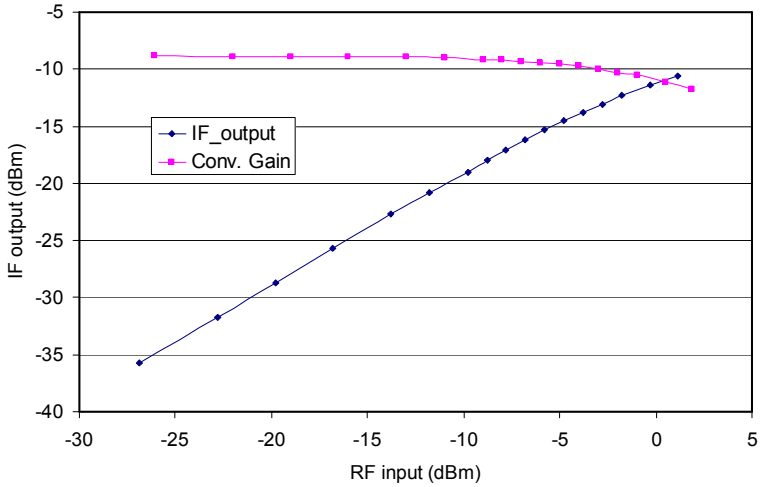


Figure 20. Linearity measurement of the pure passive SHM.

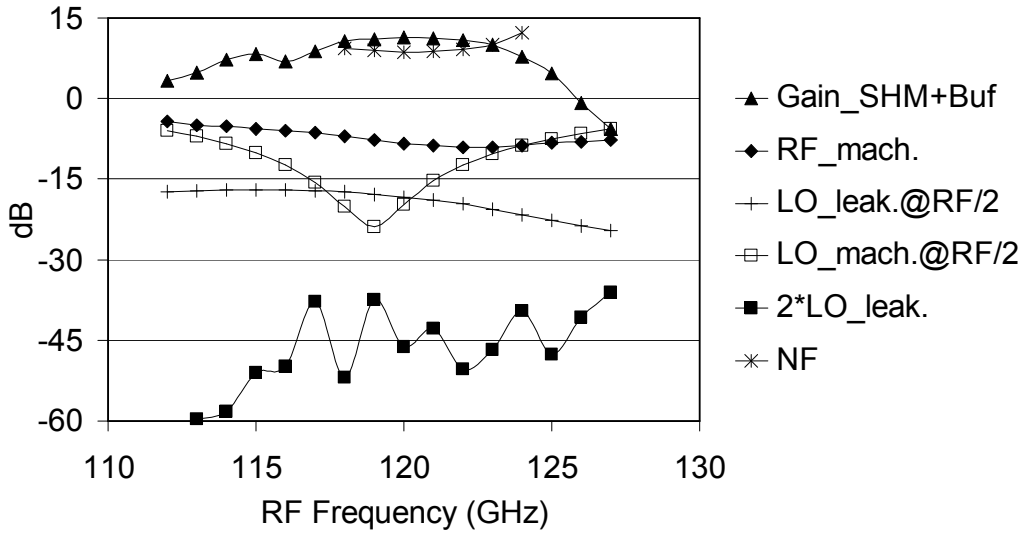


Figure 21. Conversion gain of the SHM with output buffer.

2.1.6 122 GHz quadrature coupler

A 122 GHz quadrature coupler has been designed and fabricated. Its chip photo is shown in figure 22. It is measured at two outputs separately with the other port loaded to 50 ohm. The microstrip lines have been curved to save chip area. Figure 23 shows the measured insertion loss of the two outputs. At the target range, the insertion loss is about 1 dB and the difference at the two outputs is less than 1 dB. Figure 24 shows the phase difference at the two ports. At the targeted 122-123 GHz band, the phase imbalance is below 2 degree.

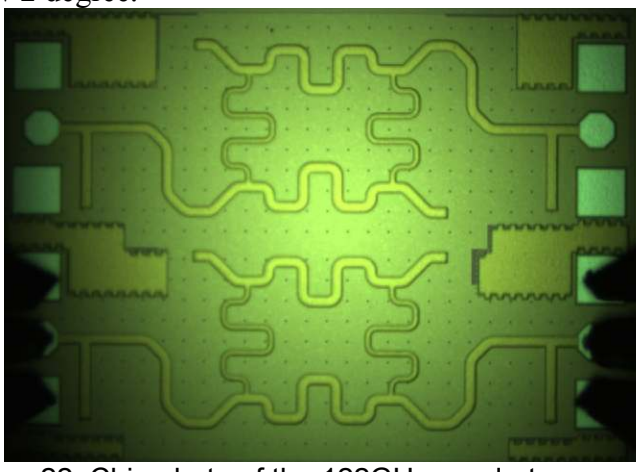


Figure 22. Chip photo of the 122GHz quadrature coupler.

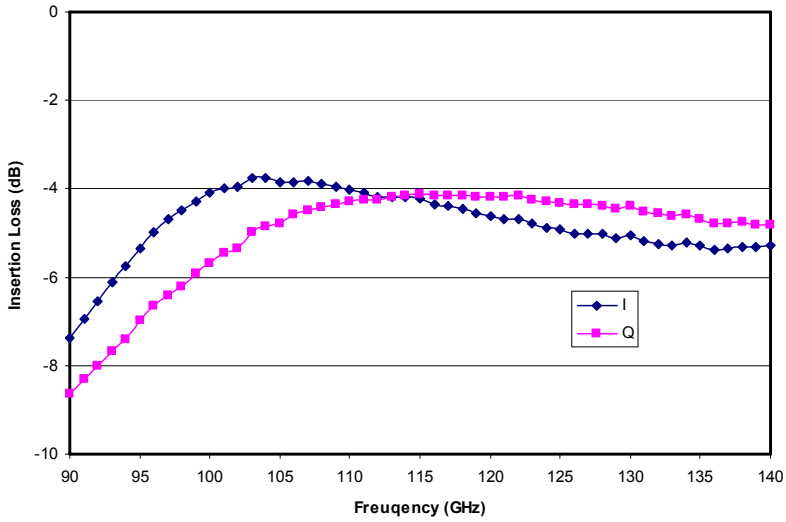


Figure 23. Amplitude imbalance of quadrature coupler.

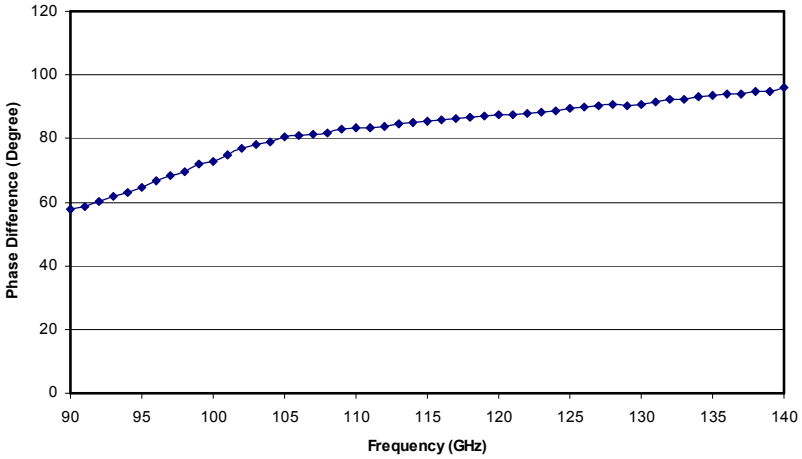


Figure 24. Phase difference between the two outputs.

2.1.7 IF VGAs

Two versions of IF VGAs have been designed and fabricated, one with overall gain of 18dB and 6 dB per tuning step, the other one with overall gain of 6 dB and 1dB per tuning step. The IF VGAs are designed by high voltage CMOS transistors to have better linearity. The gain tuning curve of the 18dB VGA is shown in figure 25 and the frequency response is shown in figure 26 for the highest and lowest gain settings. Its measured 3dB bandwidth is about 400 KHz. Figure 27 shows the gain measurement of the second VGA with 6dB overall gain. The gain tuning with respect to tuning setup is rather linear. Its frequency response is shown in figure 28 for the lowest and highest gain settings. The measured 3dB bandwidth is about 300 KHz.

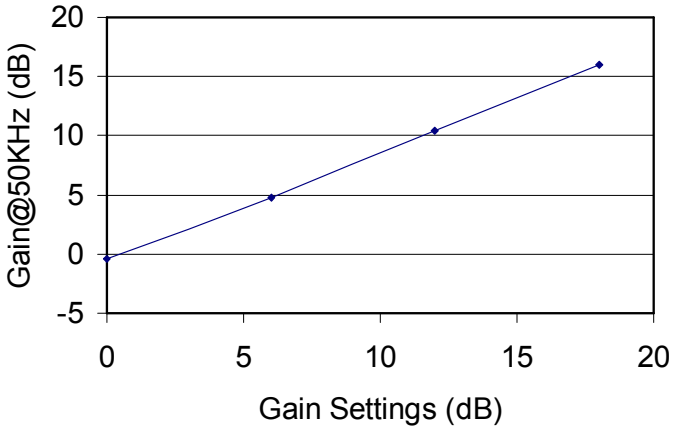


Figure 25. Gain measurement of the baseband VGA1 with 6 dB tuning step.

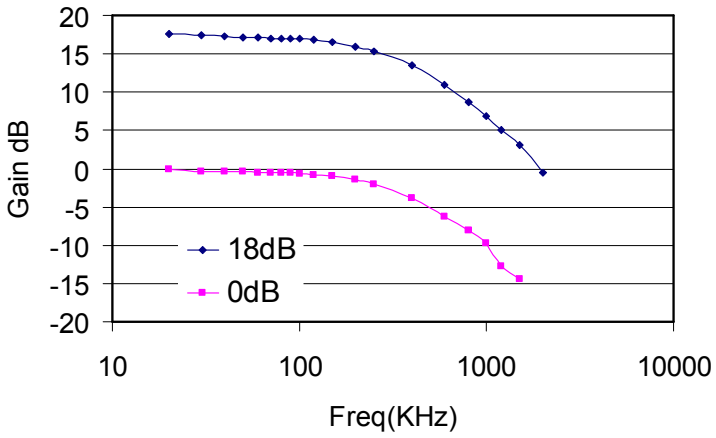


Figure 26. Frequency response of VGA1 at highest and lowest gain settings.

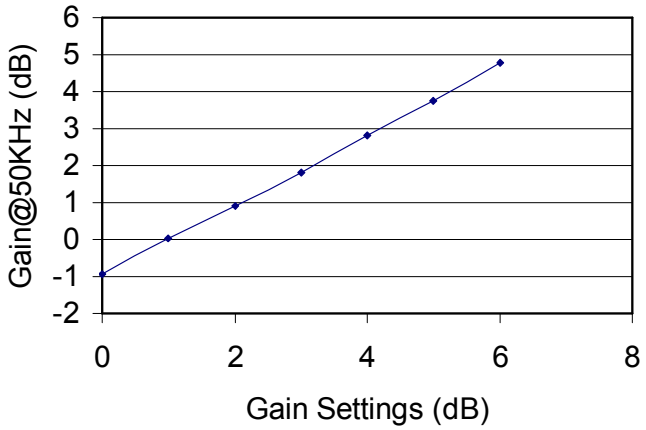


Figure 27. Gain measurement of VGA2 with 1dB tuning steps.

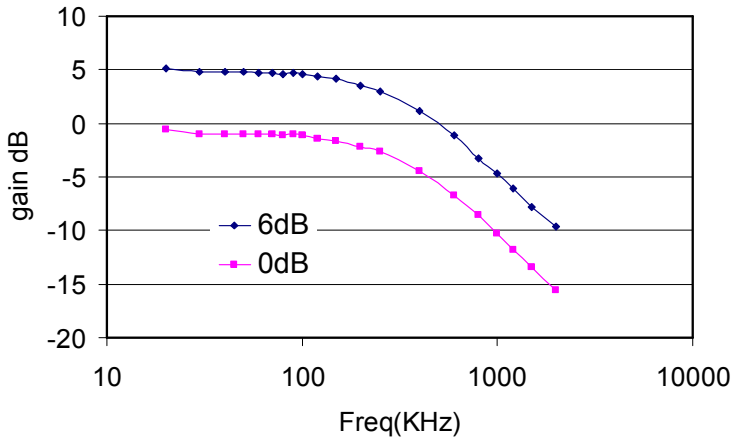


Figure 28. VGA2 frequency measurement with highest and lowest gain settings.

2.2 Integrated sub-harmonic front-end measurement

The building blocks in figure 1 have been integrated into the 1st version of AFE, where necessary components are added for RF routing, e.g. power splitters and power combiners. Digital controls have been added to each analog building block to vary their operation condition compensating the process variation. These digital controls can be accessed by an integrated SPI interface to reduce the number of bond-pads. Besides digital control, each analogue block has a duplicate analog control to mitigate the risk and increase the reliability. The complete chip photo is shown in figure 29, where the complete area is 1.8x2.2mm^2.

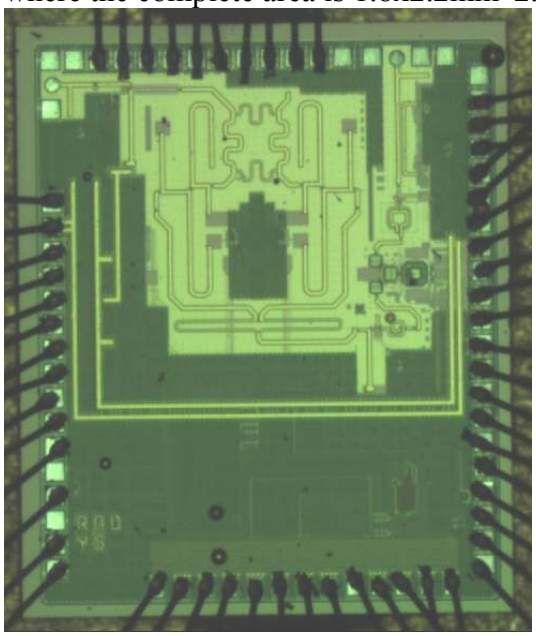


Figure 29. Chip photo of the sub-harmonic transceiver.

A rough measurement of the sub-harmonic transceiver chipset has been performed and its functionalities have been checked. The chipset was first mounted onto a PCB and wire-bonded to the board. Its transmitter and receiver are probed on a probe station to measure them separately. The setup of the measurement is shown in figure 30.

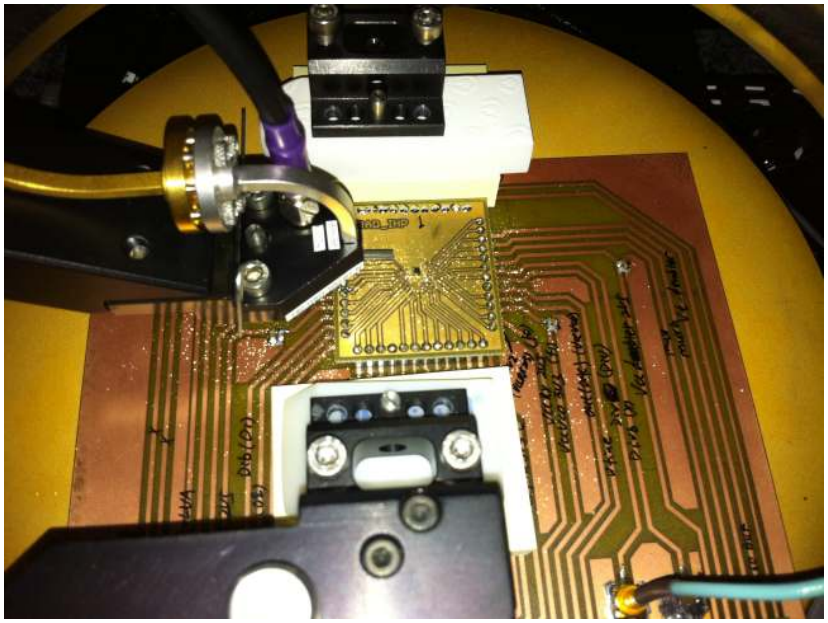


Figure 30. Probe station setup, the 122GHz interface is directly probed on-chip.

The VCO frequency has been measured at the divider output and is calculated according to division ratio. The overall tuning range is 118GHz to 121GHz with digital controlled sub-bands. Three bits are used to program the VCO sub-bands providing all together 8 sub-bands. Each sub-band has a tuning range of about 500MHz corresponding to a low VCO gain. The VCO fundamental frequency is 30GHz and the fixed static divider ratio is 16.

Receiver measurement has been performed by feeding the 120GHz signal to the input of LNA by an RF probe as shown in figure 30. Its input and output voltages are shown in figure 31. Input and output impedances are 50ohm and 20Kohm. The highest voltage conversion gain has been calculated as 38dB with an input P1dB of -26dBm. The calculated gain from each building block is 39dB, which is 10dB LNA, -4dB quadrature coupler, 11dB mixer +buffer, 22dB VGA. There is only 1dB difference between expected and measured value. The gain tuning range of the BB VGA is 24dB with a 1dB step. The highest input P1dB is roughly -14dBm. The output voltage has been measured by an oscilloscope because the output is high impedance. The measurement error is about 1 or 2 dB.

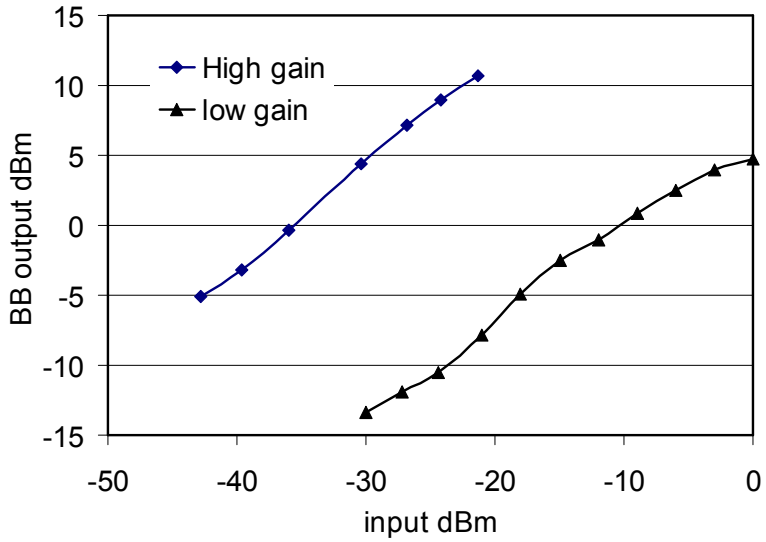


Figure 31. Receiver conversion gain measurement for high gain and low gain settings.

Transmitter output was probed by the same RF probe and measured its power is measured by a network analyzer as b1. The measured 120GHz output power is estimated as 0dBm due to the difficulties of calibrating out all the connection losses. The power detector outputs are 450 and 45 mV for forward and backward powers. Its output power can be tuned by tuning the frequency doubler current. Output power can be tuned to be 3dB lower, 30dB lower and more by SPI or continuous tuning by the analogue tuning node. The overall chip consumes 70mA from 3.3V and 86mA from a 2.5V in the default nominal operation.

Operation conditions of each building block have been tested through SPI interface and all are working. Each building block is controlled by a 4bit register of the SPI slave.

3. ZIF Transceiver front-end with fundamental mixing scheme

Together with IHP in the SUCCESS-project, Silicon Radar developed first radar test-structures which were fabricated in IHPs SG13 SiGe BiCMOS technology in the run T252. Figure 32 shows the circuit architecture of the two FMCW radar chips developed by Silicon Radar:

a) Complex radar system with RX and TX and with digital control of all the circuits via SPI-bus
b) Simple radar system w/o digital control

The complex radar system shown in Figure 32a) consists of 120GHz push-push oscillator as a central part of the system. The RF-power generated there is directed to the TX-antenna via power amplifier. The power level can be measured by two power detectors placed between the power amplifier and TX-output. The RF-signal from oscillator is directed to RX-path via buffer circuits. The RX-signal is amplified by LNA and converted to baseband in two mixers with qadrature LO. The 120GHz oscillator has a digital 3-bit coarse tuning input and one analog fine tuning input. The analog fine tuning input can be used for CW radar operation with fixed frequency in PLL-mode by using the internal frequency divider (1/16) or for FMCW-radar with internal ramp-generation by using the integrated DA-converter. For smoothing the staircase voltage from the DA-converter, an external filter is provided. For calibration of oscillator frequency, a frequency measurement unit is integrated. High-speed ramps can be generated with the internal memory (shift-register) with fast clocking. All the functionality is controlled by SPI-bus.
The second version is a more simple design. It is intended for CW radar system w/o all the digital and DA control to ensure functionality for the case that the complex radar system with the complicated interaction of RF, analog and digital parts will fail to work. The simple radar chip consists of oscillator, power amplifier, power detector, quadrature receiver and frequency divider for connection of external PLL-circuit. IF-amplifier and filter (marked in blue in Figure 32) are not integrated in the test-structure of the first run.

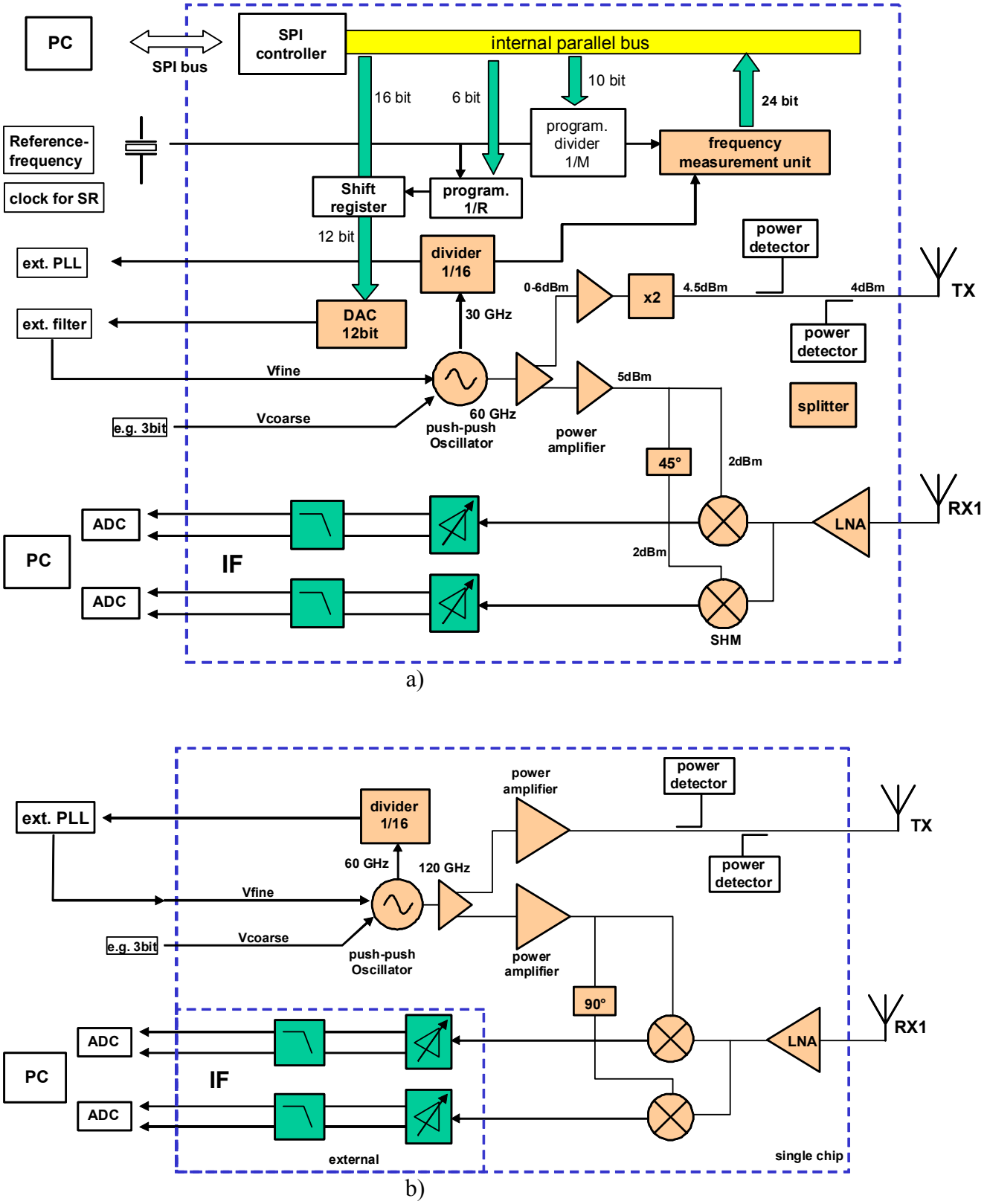
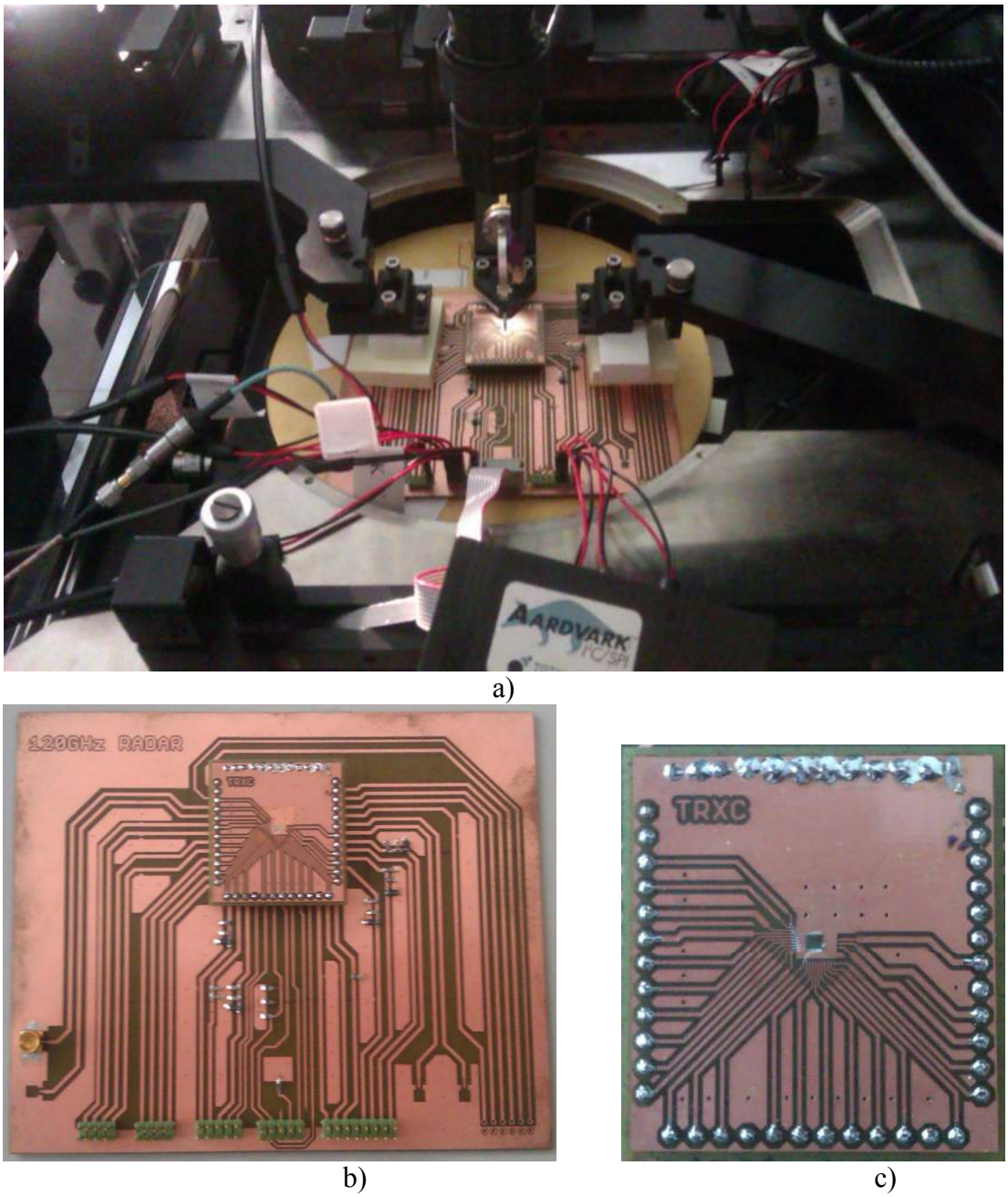


Figure 32: Block circuits of 122GHz Frontend a) complex radar system, b) simple radar system

3.1 Measurement Setup

Dedicated PCBs were developed for the measurement setup which is shown in Figure 33. The chips were mounted on small boards and then all the low-frequency interfaces were bonded. The 120 GHz transceiver input output were contacted using high frequency probes. The board with IC is attached to the so-called main-board equipped with all necessary connectors.



a)

b)

c)

Figure 33. Measurement Setup.

An Aardvark SPI host controller with appropriate software was used to access the digital control of the radar transceiver chip.

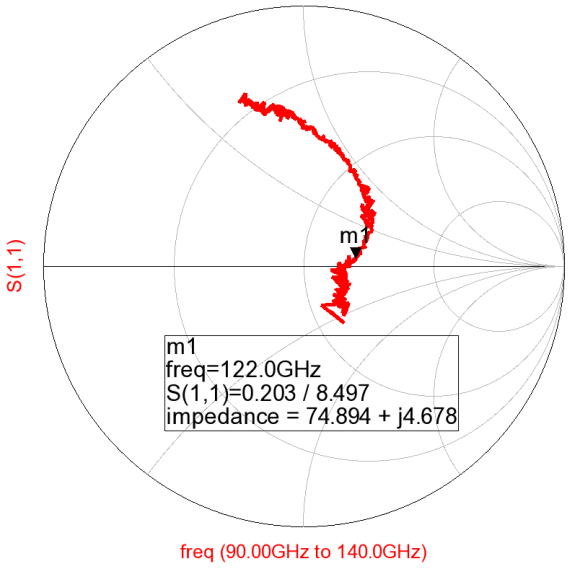
3.2 122 GHz Complex Radar System Measurement Results

3.3 RF frontend Measurements

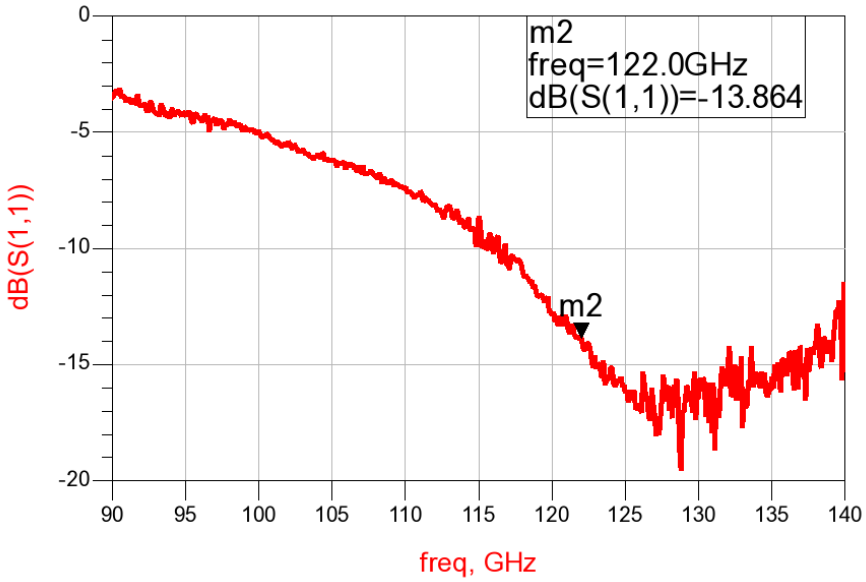
The measured parameters of the radar chip are summarized in Table 1. It features moderate power consumption of about 380 mW. The receiver input is well matched to 50 Ohm as presented in Figure 34 a) and b). The conversion gain of the receiver reaches 25.5 dB and can be reduced to 10 dB. The gain control is realized by digitally controlled VGAs. The receiver reaches 1 dB ICP at the input power of -25 dBm for the maximum gain as shown in Figure 35. Tuning characteristic of the VCO was measured at the divider output and then scaled by the division ratio (32). As shown in Figure 36, the overall tuning range of the VCO is 3.7 GHz divided in 8 sub-bands. The choice of the sub-band is done digitally by programming appropriate bits of the SPI register. The phase noise shown in Figure 37 is measured at the divider output as well. It was not corrected about the division ratio (extra 6 dBc per division by 2).

Table 1: Summary of measured parameters of the Complex Radar Transceiver

Parameter	**Value**
Supply voltage - analog	3.3 V
Supply voltage digital	1.2V
Current consumption ICC	114 mA
Gain	10-25.5 dB
Input Compression Point	-25 dBm
VCO tuning range	120.6 – 124.3 GHz
Output power	-2.5 – -7 dBm



a)



b)

Figure 34. Measured S11 of the Receiver.

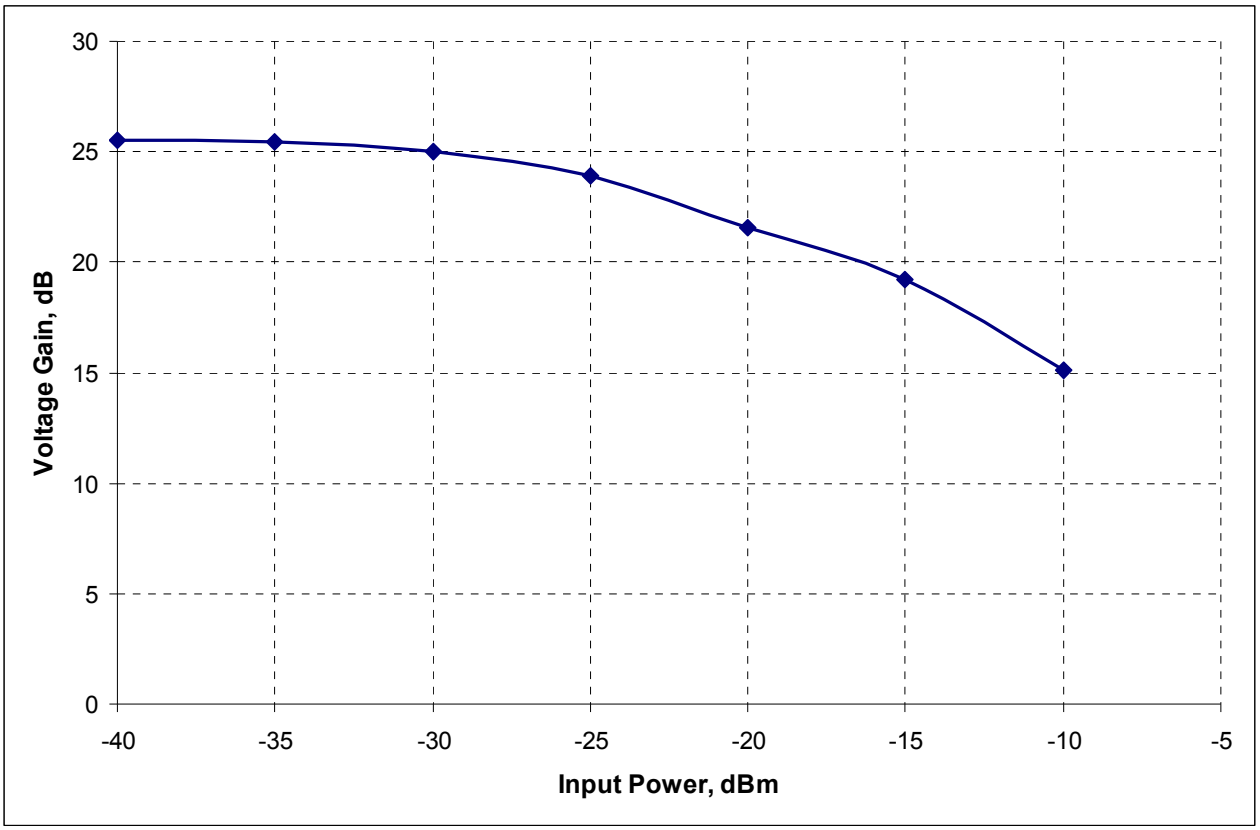


Figure 35. Measured Conversion Gain of the receiver.

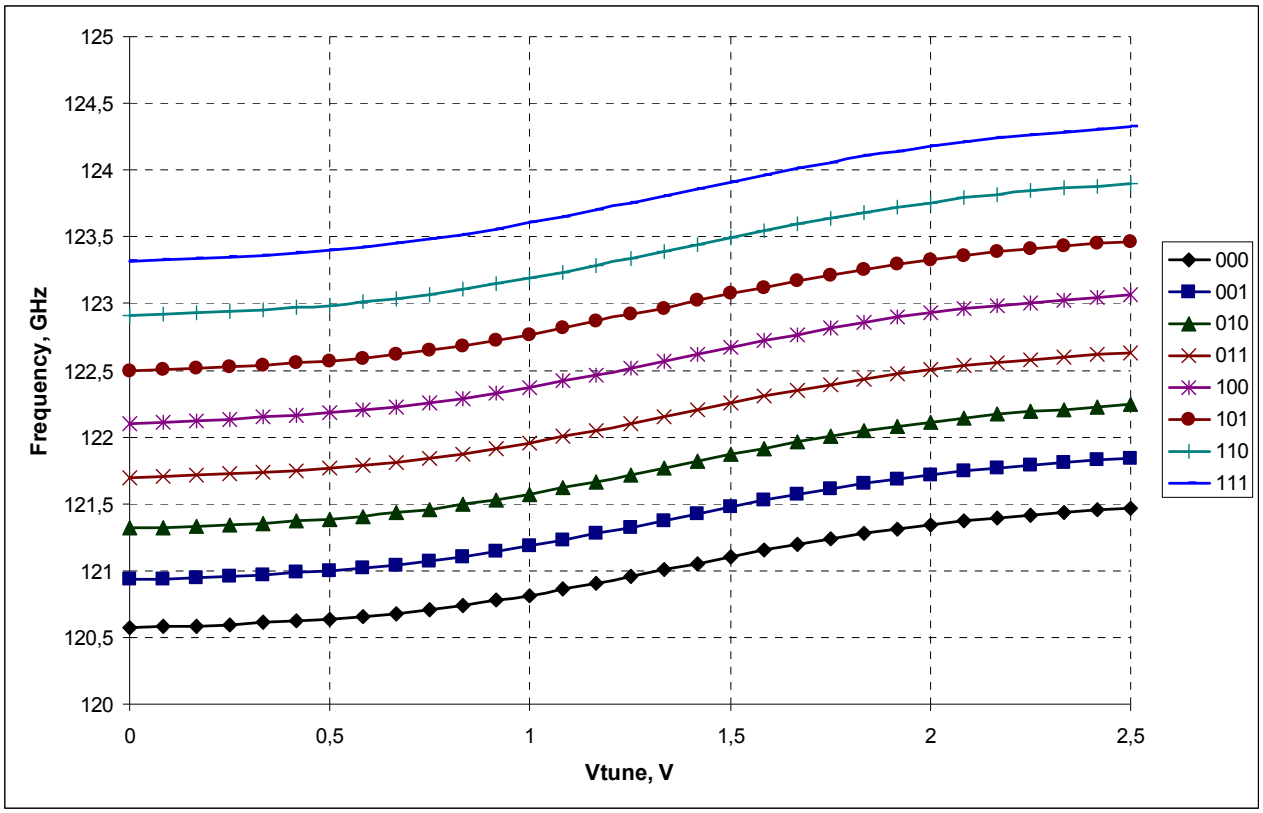


Figure 36. Measured tuning range of the VCO

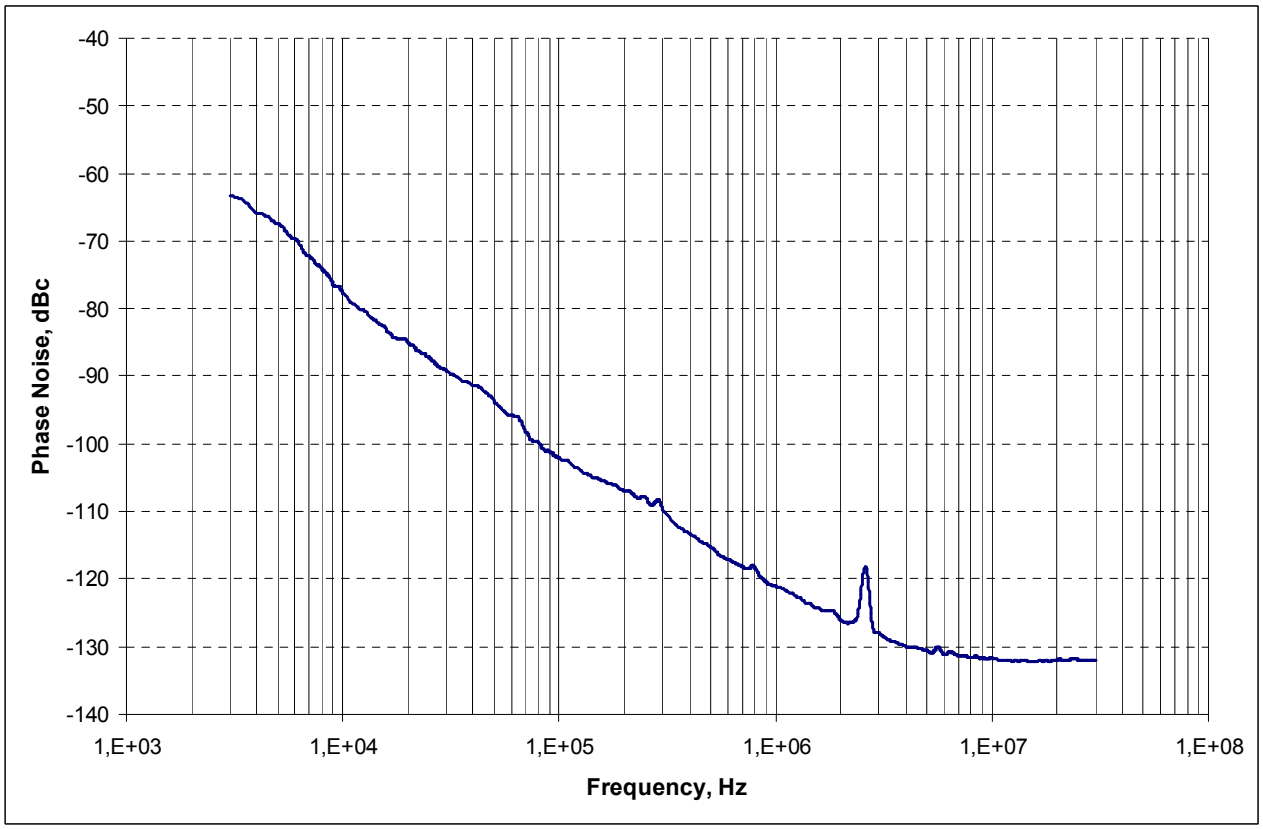


Figure 37. Measured Phase Noise of the VCO.

3.4 Digital Control

Detailed description of Digital control of AFE can be found in Digital control design specification. The block diagram of the digital control implemented as ASIC in IHP CMOS 0.13 um technology is shown in Figure 38

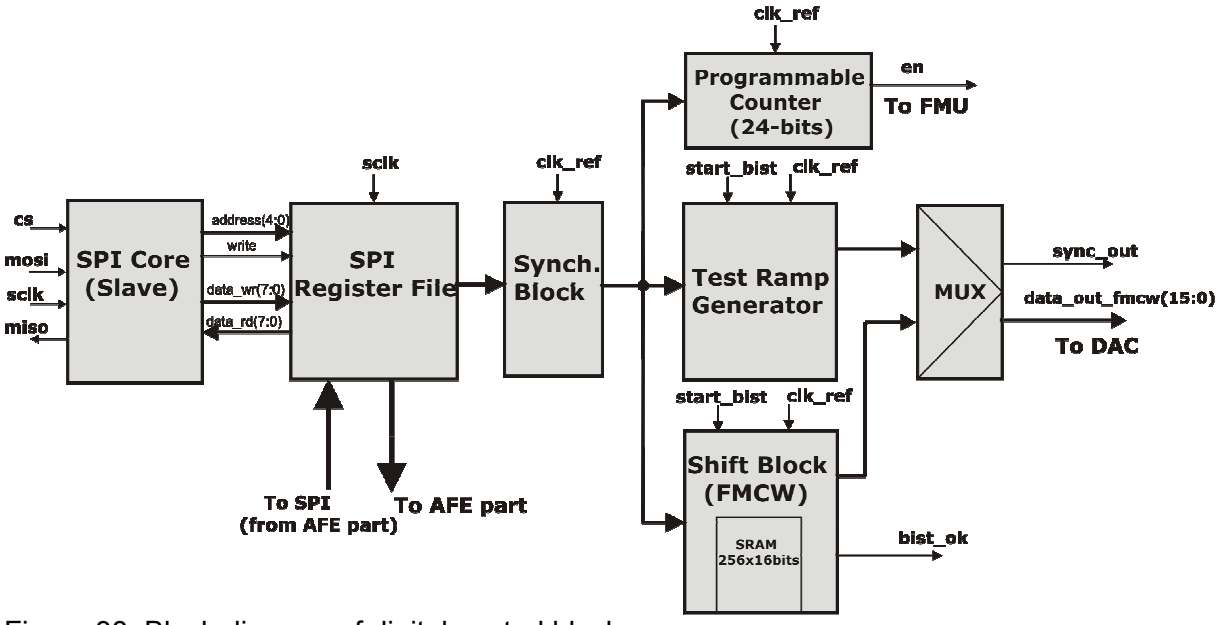


Figure 38. Block diagram of digital control block.

3.4.1 SPI Host Adapter and PC application

For accessing the digital control of the Radar 120 GHz chip, we have used Aardvark SPI host adapter (www.totalphase.com). That is a small box connected to an USB port of PC which provides a SPI host (or slave) and an I2C interface. The Aardvark software comprises a GUI for interactive access under Windows and Linux and a programming library for C, Labview, etc. The communication between PC, Aardvark adapter and Radar chip is illustrated in Figure 39. PC, Aardvark Adapter and Radar 120 GHz chip.. In our testing environment, Aardvark SPI adapter is always host (master) SPI.

Figure 39. PC, Aardvark Adapter and Radar 120 GHz chip.

We have used an C application developed for communication between the Aardvark SPI host adapter and the SPI slave implemented in the digital control of Radar chip. By using that C application, we are able to perform the operations summarized in Table 2: The SPI operation supported by C application

Table 2: The SPI operation supported by C application

1.	Read SPI register
2.	Write SPI register
3.	Configure SPI word
4.	Reset SPI slave
5.	Fast ramp programming: rising edge
6.	Fast ramp programming: rising + falling edge
7.	Fast ramp programming: rising edge + flat region + falling edge

3.4.2 Test procedures

Initialization (Reset)

After connection Aardvark SPI adapter and switching power-on, it is required to initialize (reset) the digital control before starting any programming of SPI registers. For this purpose we have used the operation "Reset SPI slave" Table 2: The SPI operation supported by C application. Basically, that operation delivers a low-level signal for a short time at input 'nres' pin of the chip. Since the reset signal is synchronized with clock reference signal, it is required to have active clock reference signal during reset. The timing diagram is shown in Figure 40: Initialization (reset)Figure 40.

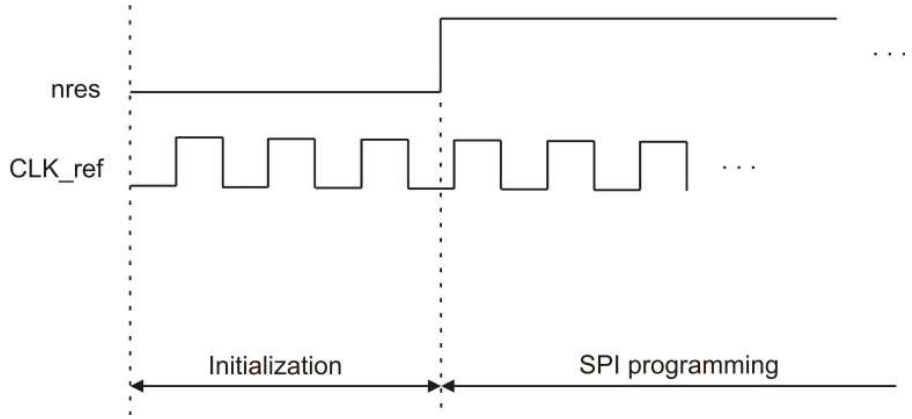


Figure 40: Initialization (reset) of SPI controller

In order to ensure correct operation of digital control, an initialization procedure shall be always done after switching power-on.

Configuration of SPI word

Before programming of any SPI register, it is required to configure the SPI word. The size and composition of the data word, which must be transferred on the SPI bus

in order to read or write registers in SPI slave, depends on the SPI slave configuration. It constitutes of: register address, read enable bit, data word and write enable bit. In our configuration, the read enable bit is not present. Configuration parameters of the SPI word in our chip are summarized in Table 3.

Table 3: Configuration parameters of the SPI word

Addressable Registers	Address Bits	Data Bits	Write Enable Bit	Read Enable Bit	Total SPI Word Bits
26	5	8	1	0	14

SPI programming

The SPI programming (writing and reading registers) is based on communication protocol shown in Table 4 and Table 5 . Since the Aardvark adapter may send and receive only 8-bit (a byte) words via SPI interface, the communication protocol is based on exchanging two data bytes.

Table 4. Write to SPI register.

SPI bit number	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SPI input	SPI register address					written data								1	0	0
SPI register	the first write								the second write							

Table 5. Read to SPI register.

SPI bit number	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SPI input	SPI register address					0	0	0	0	0	0	0	0	0	0	0
SPI output	-					read data								-	-	-
SPI register	the first read								the second read							

The chosen SPI clock polarity (CPOL) and SPI clock phase (CPHA) values are CPOL = ‘1’ and CPHA = ‘1’. Data transmission format for one byte of such configuration is shown in Figure 41. The SPI slave in digital control can support only this transmission format. SPI master and slave need to agree about data transmission format. Therefore, it is required to configure the Aardvark adapter (SPI master) to support the same transmission data format as the SPI slave.

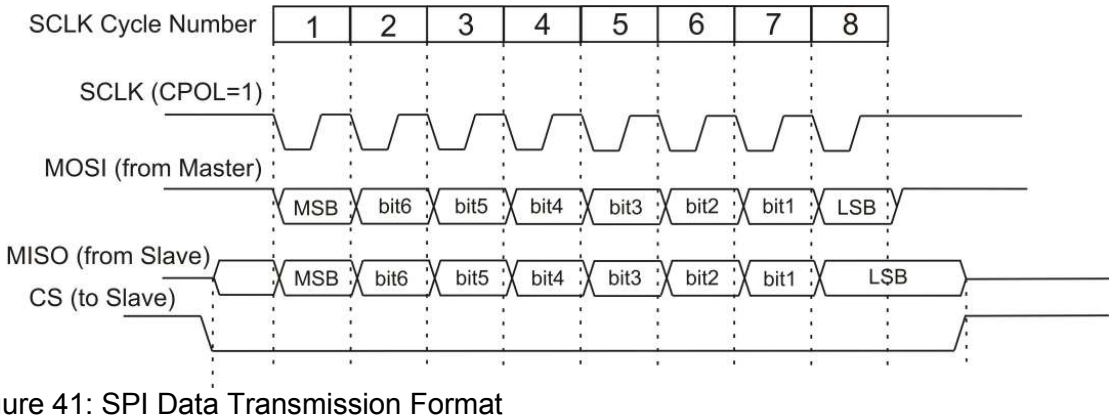


Figure 41: SPI Data Transmission Format

Functionality of the SPI slave itself can be checked by simple write-read procedure. An arbitrary data can be written in to a SPI register and then read out that register to check whether the same value is read out.

Example:

To write data value "10100110" in register 8 the following bits shall be sent:

address(4:0)					data value (7 :0)								we	dummy	
0	1	0	0	0	1	0	1	0	0	1	1	0	1	0	0

After a write enable bit (we) the two dummy bits (zeros) shall be sent to fill the complete SPI word consisting of two bytes.

To read the register 8, the following bits shall be sent:

address(4:0)					data value (7 :0)								we	dummy	
0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Note that after the address bits, all remaining bits are zero bits.

3.4.3 Digital Ramp Generation

We have used the following procedure to generate the digital ramp:

1. Set the following parameters: writing mode of RAM cell, number of ramp points, and programmable ratio R (bits(11:6)). This is done by programming SPI register 0 and 1. Please see "Digital Control – Design Specification" document.

2. Fast ramp programming. In this step the values of ramp which will be generated are written into RAM cell. By using the current version of C application we are able to perform fast ramp programming with three different ramp shape, see Table 3 and Figure 42. In principal, the shape of the ramp is only software issue which means that we are able to generate any shape of ramp by a software modification. Since we have implemented 12-bits DAC in Radar chip, the maximum value of ramp is 4095.

3. Set the following parameters: reading mode of RAM cell and programmable clock ratio R (bits (5:0)). This is done by programming again register 1. Once this step is finished, the digital ramp is generated with period of :

$$T_{ramp} = \frac{(R+1)N}{f_{clk\_ref}} \quad (1)$$

where R is programmable clock ratio, N is number of ramp points and f_{clk_ref} is reference clock frequency.

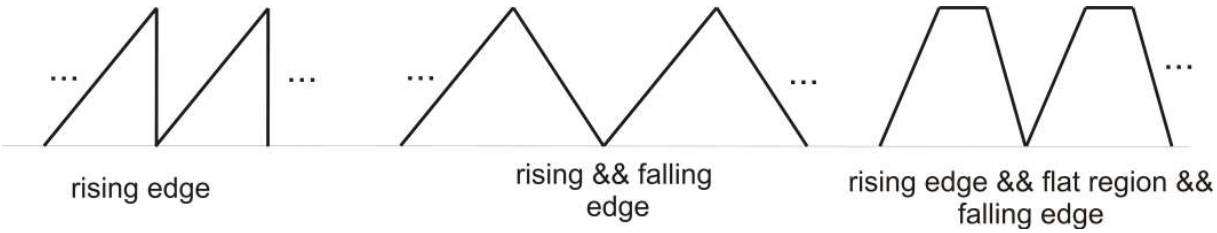


Figure 42: Shapes of digital ramp supported by SPI software (C application)

Example 1:

1. Programming of register 0 and 1:

Register 0: Write "00011111"; in hex format: 1F
Register 1: Write "11111111"; in hex format: FF

2. Fast ramp programming with rising edge:

num_ramp_points = 256; ramp_step = 16; start_value = 0;

3. Programming of register 1:

Register 1: Write "01100111"; in hex format 67

The period of the generated ramp is (f_{clk_ref} = 10MHz):

$$T_{ramp} = \frac{(499+1)*256}{10MHz} = 12.8 \text{ ms}$$

The maximum value of the ramp is 255*16 = 4080 corresponding to the almost maximum voltage level at the DAC output (1.2 V).

Figure 43: The rising edge ramp: the output of DAC (yellow colour)

Example 2:

1. Programming of register 0 and 1:

Register 0: Write "00000011"; in hex format: 03
Register 1: Write "11111111"; in hex format: FF

2. Fast ramp programming with rising edge:

num_ramp_points = 256; ramp_step = 16; start_value = 0;

3. Programming of register 1:

Register 1: Write "00010011"; in hex format 13

The period of the generated ramp is:

$$T_{ramp} = \frac{(9+1)*256}{50MHz} = 51.2\ \mu s$$

Figure 44. The rising edge ramp: the output of DAC (yellow color)

Example 3:

1. Programming of register 0 and 1:

Register 0: Write “00011111”; in hex format: 1F
Register 1: Write “11111111”; in hex format: FF

2. Fast ramp programming with rising and falling edge:

num_ramp_points = 256; ramp_step = 32; start_value = 0;

3. Programming of register 1:

Register 1: Write “01100111”; in hex format 67

The period of the generated ramp with symmetrical rising and falling edge is:

$$T_{ramp} = \frac{(499+1)*256}{10MHz} = 12.8 \text{ ms}$$

The maximum value of the ramp is 127*32 = 4064.

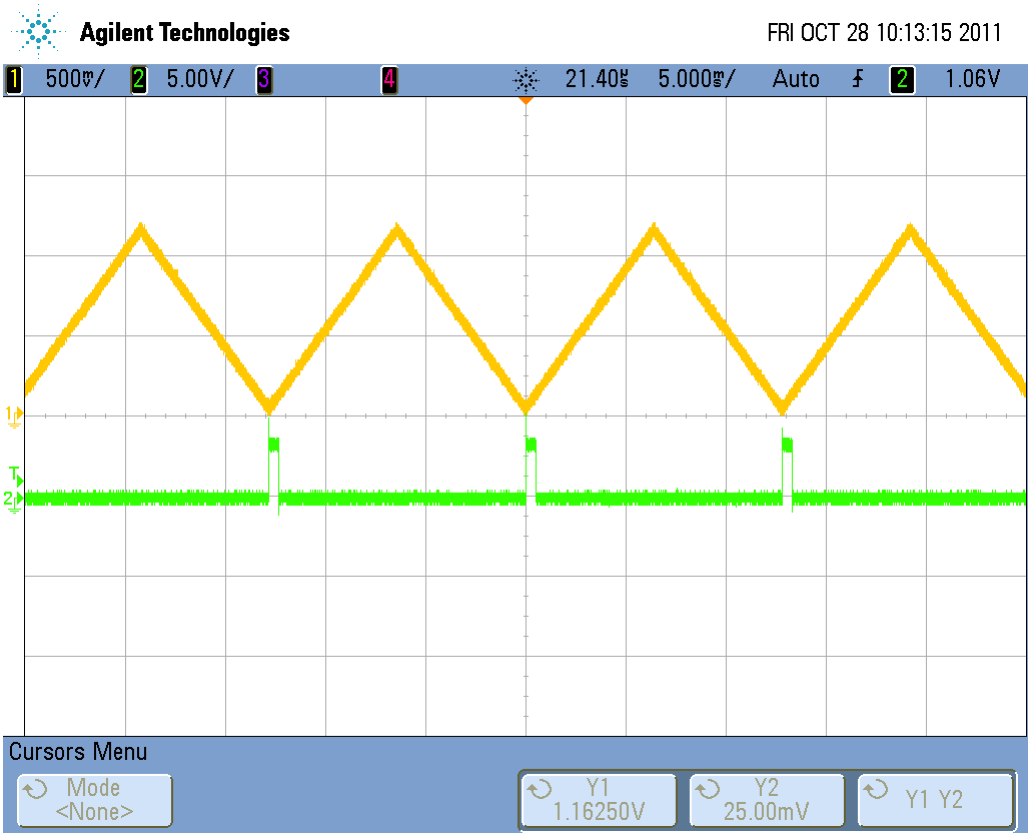


Figure 45. The ramp with rising and falling edge: the output of DAC (yellow color)

Example 4:

1. Programming of register 0 and 1:

Register 0: Write "00011111"; in hex format: 1F
Register 1: Write "11111111"; in hex format: FF

2. Fast ramp programming with rising edge, flat region and falling edge:

num_ramp_points = 256; num_ramp_points_flat_region = 56; ramp_step = 40; start_value = 0;

3. Programming of register 1:

Register 1: Write "01100111"; in hex format 67

The period of the generated ramp with flat region and symmetrical rising and falling edge is:

$$T_{ramp} = \frac{(499+1)*256}{10MHz} = 12.8 \text{ ms}$$

The maximum value of the ramp is 100*40 = 4000.

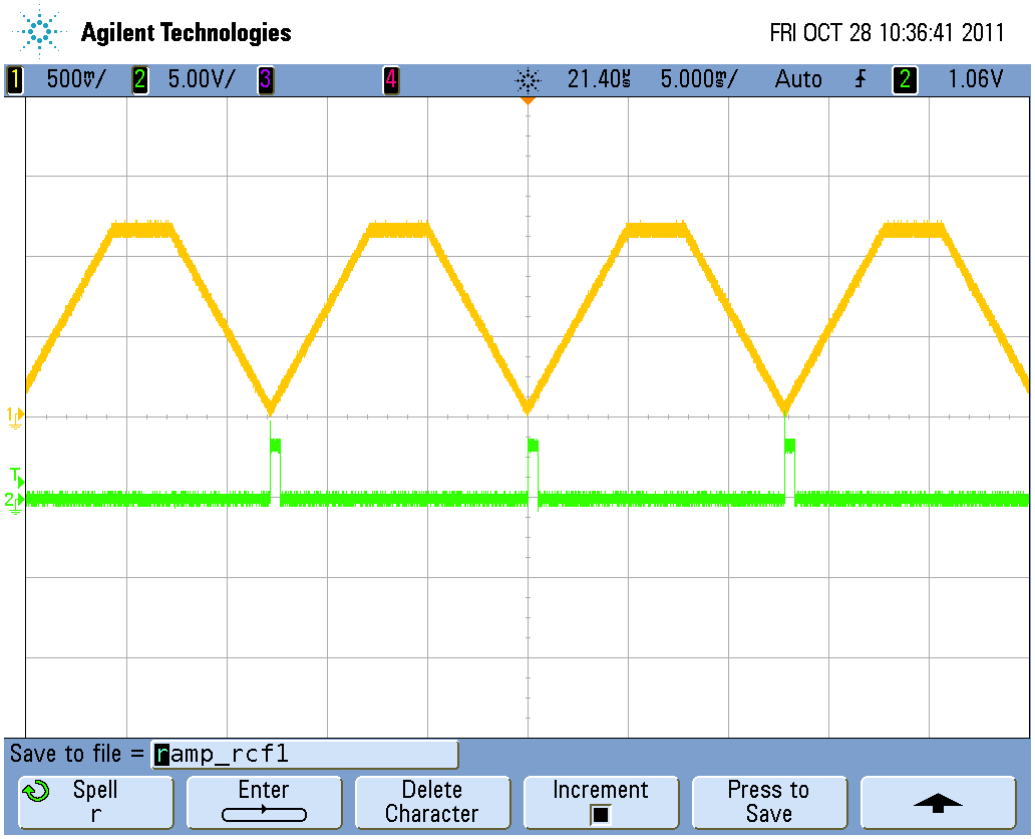


Figure 46: The ramp with rising edge, flat region and falling edge: the output of DAC (yellow colour) and 'sync_out' signal (green colour)

3.4.4 Frequency Measurement

A timer implemented in the digital control provides an enable signal for frequency measurement. The enable signal is active within time interval programmable via SPI. In order to define that time interval, registers 4, 5, and 6 shall be programmed.

Example:

1. Programming of registers 4, 5 and 6:

Register 4: Write "00000000"; in hex format: 00
Register 5: Write "00100111"; in hex format: 27
Register 6: Write "00010001"; in hex format: 11

The enable signal required for frequency measurement is active within the time interval of

$$T_{enable} = \frac{(M-1)}{f_{clk\_ref}} \quad (2)$$

where *M* is 24-bits value of register 4, 5 and 6.
Therefore, T_{enable} is :

$$T_{enable} = \frac{(10001-1)}{10MHz} = 1 \text{ ms}$$

3.4.5 BIST Test

BIST test is used to check functionality of RAM cell itself. Additionally, DAC functionality can be also tested without programming RAM cell. The clock reference signal needs to be active with the default frequency of 50 MHz.

The BIST procedure for RAM cell is as follows:

1. Reset the digital control

2. Set high level at '*start_bist*' pin

3. Check a level at '*bist_ok*' pin. If the BIST is successful, the high level is set at *'bist_ok'* pin.

The BIST procedure for DAC testing is as follows:

1. Reset the digital control

2. Set high level at '*start_bist*' pin

3. Check the output the DAC ('*Out_da'*) pin. If the BIST is successful, the DAC generates
the ramp with period of 500 μs.

By programming two bits of register 7, the ramp with period 1 ms or 2 ms can be generated.

The BIST procedure for DAC testing (the ramp with period of 1 ms or 2 ms) is as follows:

1. Reset the digital control

2. Programming of register 7:
Register 7: Write "00000001", in hex format "01" – for the 1 ms ramp
Register 7: Write "00000010", in hex format "02" – for the 2 ms ramp

3. Set high level at '*start_bist*' pin

4. Check the output the DAC ('*Out_da'*) pin. If the BIST is successful, the DAC

generates the ramp with period of 1 ms or 2 ms.

3.4.6 Test Results

The Radar 120 GHz chip with the digital control has been taped out in March 2011. Test results are summarized in Table 6.

Table 6: Test results

Test	Pass/Fail
SPI functionality	Pass
Memory BIST	Pass
DAC BIST	Pass
Ramp generation	Pass
Frequency measurement	Fail

3.5 Frequency Ramps

Having tested the ramp generation procedure and DAC we wanted to verify the response of the VCO to such tuning signal. We connected the output of the DAC to the tuning output (without any extra components). We used a Signal Source Analyzer (SSA) to observe the frequency ramps. Since the SSA can analyze signals with maximum frequency of 26.5 GHz we used the divider output of our radar chip. Following the procedure described in 0 we loaded ramps with different shapes. Figure 47 shows a frequency ramp with rising edge. The ramp uses the maximum range of the DAC, the internal memory was loaded with values from 0 to 4080. The next ramp, shown in Figure 48, was programmed by loading the memory with values starting from 2000 up to 4090. In both ramps the nonlinearities of the VCO tuning characteristics can be seen.

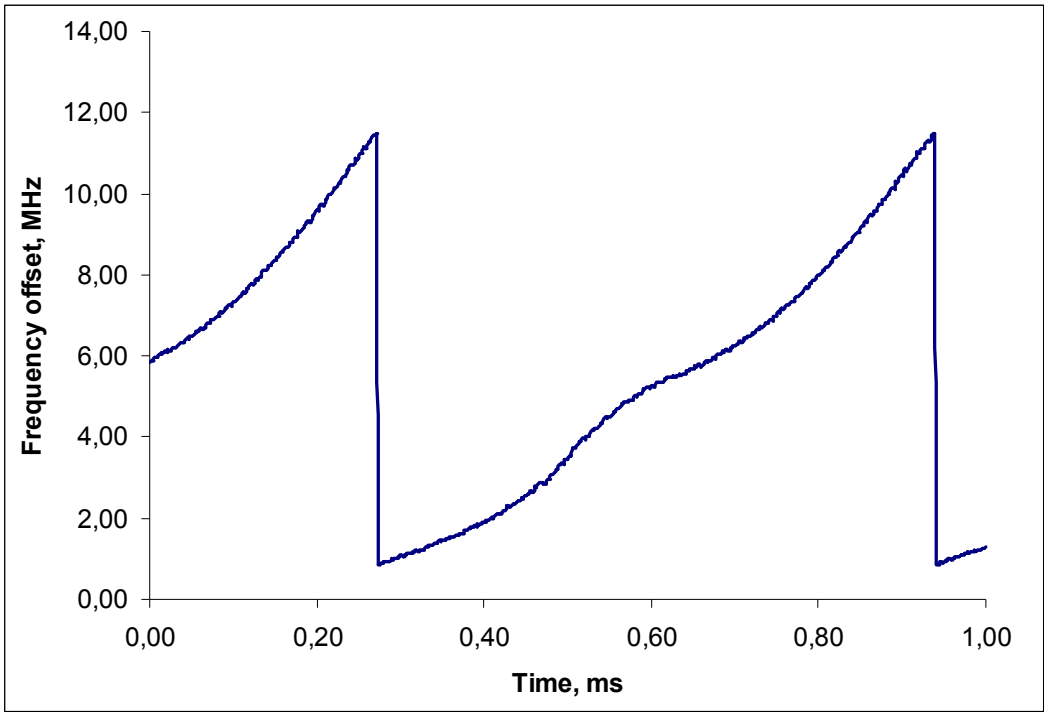


Figure 47. Ramp with rising edge, full range of the DAC.

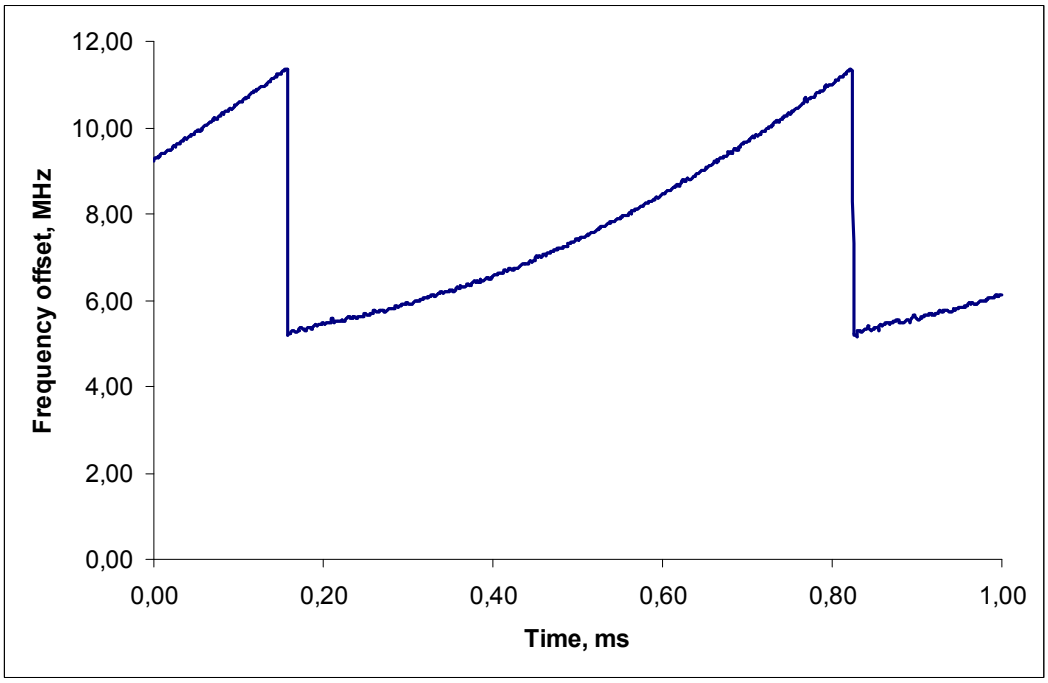


Figure 48: Ramp with rising egde, DAC values from 2000 to maximum.

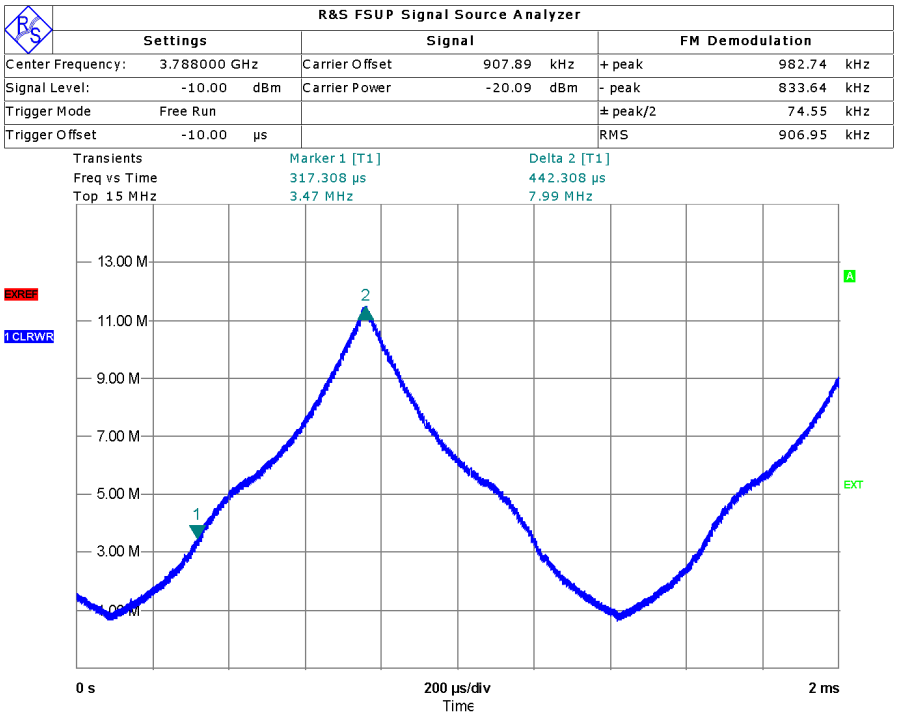


Figure 49: Ramp with rising and falling edge, full range of the DAC.

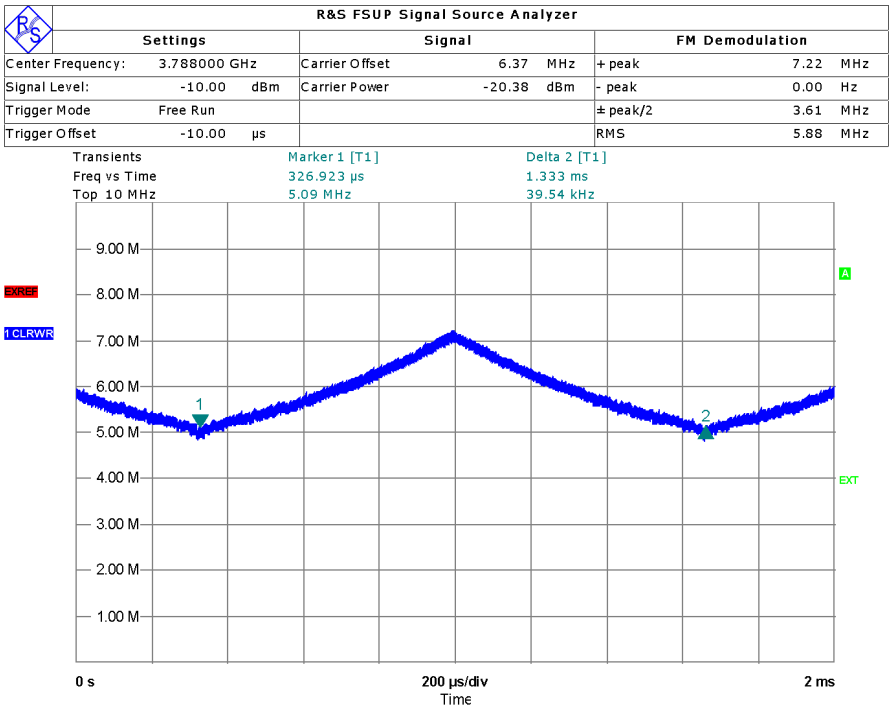


Figure 50: Ramp with rising and falling edge, DAC values from 2000 to maximum

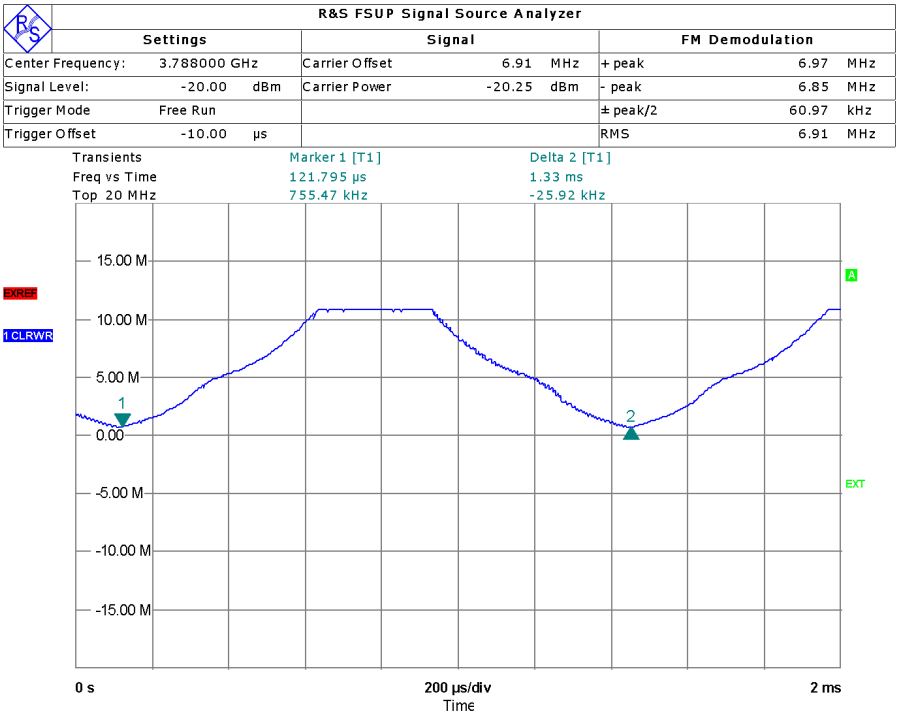


Figure 51: Ramp with rising edge, flat region and falling edge, full range of the DAC

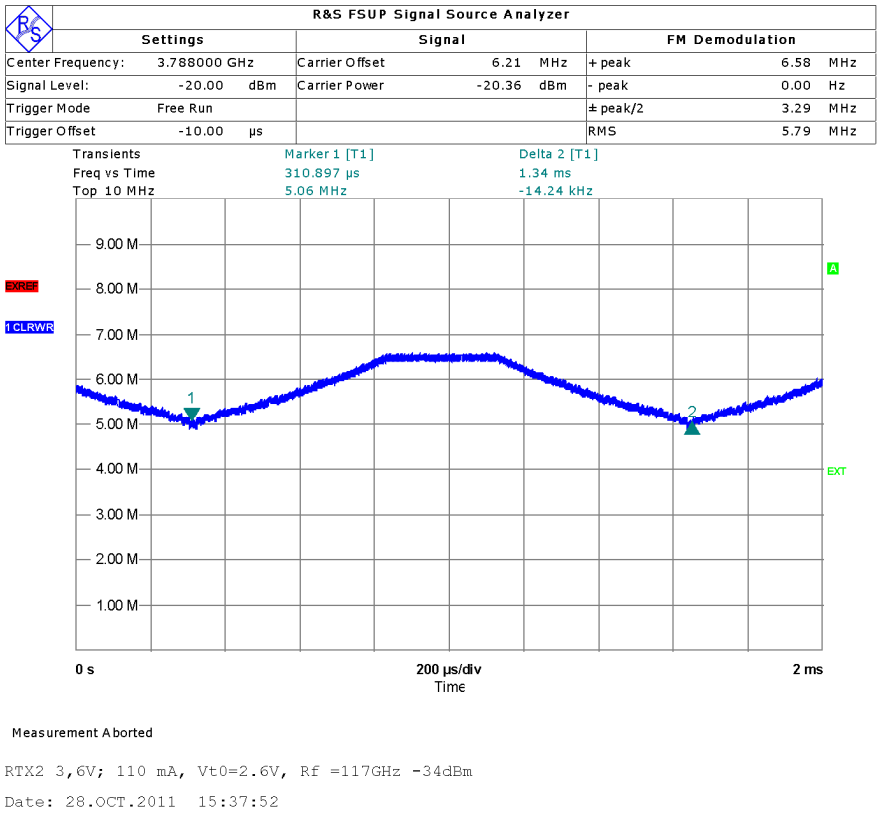


Figure 52: Ramp with rising edge, flat region and falling edge, DAC values from 2000 to maximum

The graphs shown in Figure 49, Figure 50, Figure 51 and Figure 52 show some examples of ramps which can be generated. The internal memory gives an opportunity of generating ramps with arbitrary shapes.

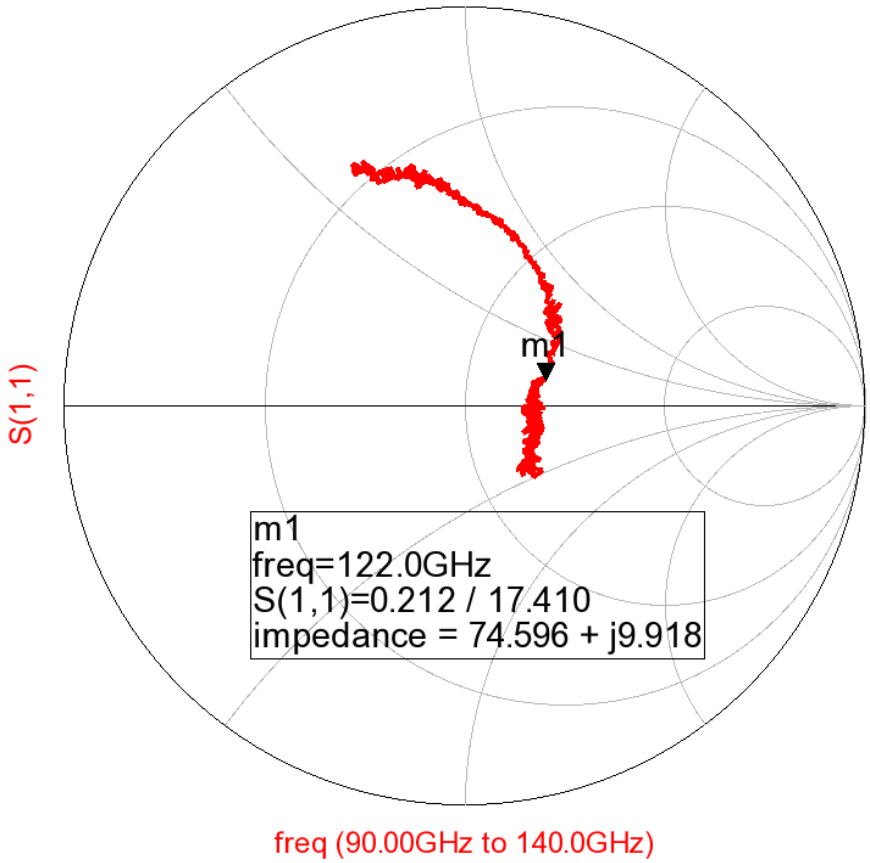
3.6 122 GHz Simple Radar System Measurement Results

The measured parameters of the radar chip are summarized in Table 1. It features moderate power consumption of about 380 mW. The receiver input is well matched to 50 Ohm as presented in Figure 53 a) and b). The receiver features a conversion gain of 10 dB. The receiver reaches 1 dB ICP at the input power of -20 dBm. Tuning characteristic of the VCO was measured at the divider output and then scaled by the division ratio (32). The overall tuning range of the VCO is 3.7 GHz divided in 8 sub-bands. The choice of the sub-band is defined by applying appropriate voltage level to tuning inputs VT (0 V or 2.5 V). The phase noise shown in Figure 54 is measured at the divider output, but it was not corrected about the division ratio (extra 6 dBc per division by 2).

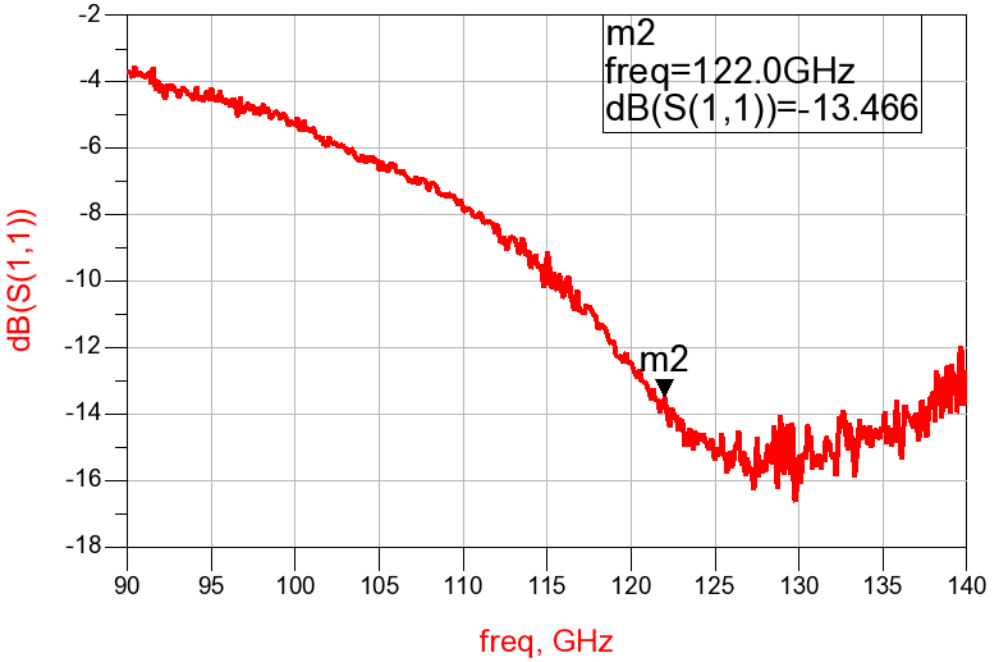
Table 7: Summary of measured parameters of the Simple Radar Transceiver

Parameter	**Value**
Supply voltage - analog	3.3 V
Supply voltage digital	1.2V
Current consumption ICC	113 mA

Gain	10 dB
Input Compression Point	-20 dBm
VCO tuning range	120.6 – 124.3 GHz
Output power	-2.5 – -7 dBm



a)



b)

Figure 53: Measured S11 of the receiver

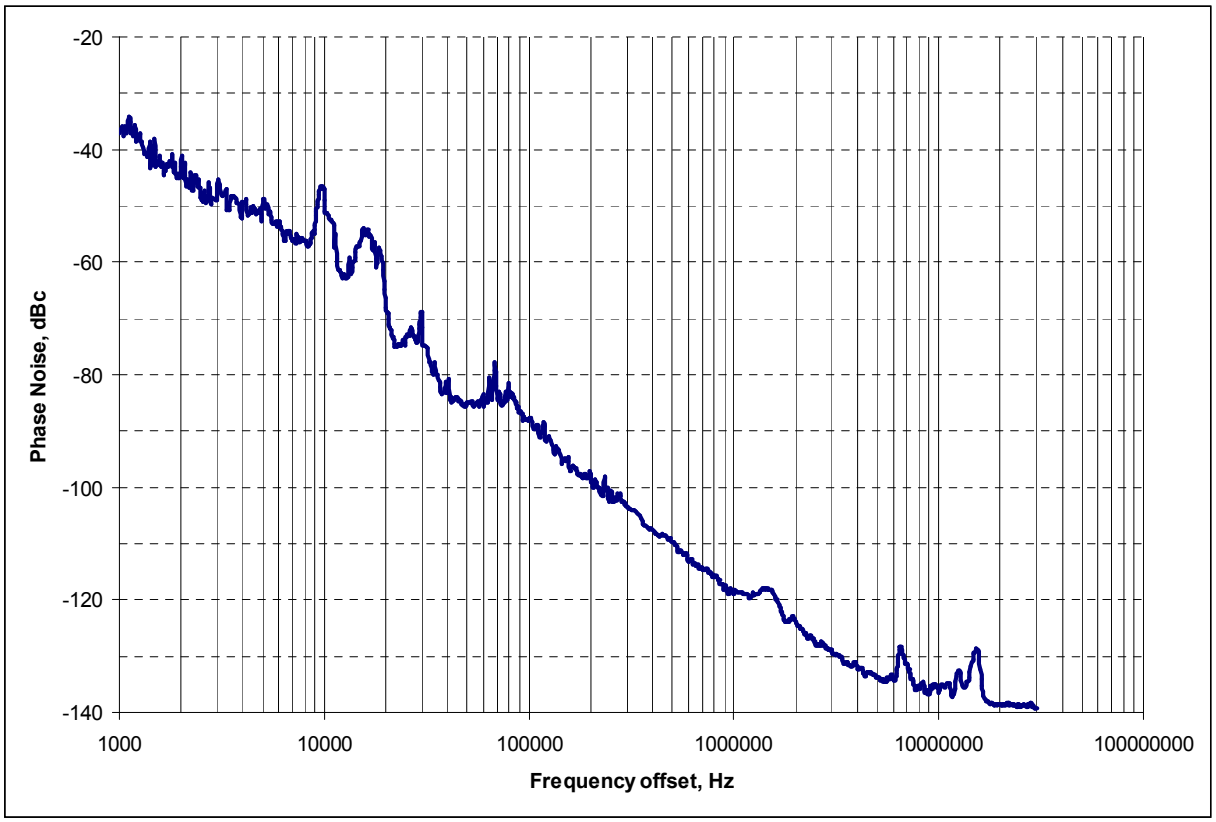


Figure 54: Phase Noise of the VCO, measured at the divider output

Conclusions

The test results of the 120 GHz Radar Chip are summarized in Table 8.

Table 8: Test summary

Building Block	**Parameter**	**Functionality**
Analog Frontend	Gain Linearity Output Power Frequency Range	+ + -+ +
Power Detectors and Temperature sensor		+
IF Variable Gain Amplifier		+
DAC		+- (output swing too low for VCO)
Digital Control	SPI functionality Memory BIST DAC BIST Ramp generation Frequency measurement	Pass Pass Pass Pass Fail

The overall functionality of the developed 120 GHz Radar Transceivers is satisfactory. The analog frontend meets the specification given by the project partners. The only parameter to be optimized is the output power which is couple dBms too low. The power detectors, temperature sensor and IF VGA work as required. The DAC functionality is proven, however, the output swing which is at the moment 1.2 V is too small to fully drive the VCO tuning input. It is required to integrate an amplifier which will amplify the DAC output signal approximately 2 times, to correctly drive the varactor diodes in the VCO. The Digital Control Block is capable of performing self test, controlling internal sub-circuits and generating various ramps. The performance of the frequency measurement was the only feature which didn't function correctly. Due to the complexity of the circuit it was unable to verify the real cause of the problem. The counter was working however the readouts of the counter values had very big spread and didn't give correct frequency values. Possible reasons for that could be incorrect operation of the block responsible for generating of the measurement duration signal or the interface between the digital circuitry and the bipolar part of the frequency counter.

Redesign outline:

- increase output power of the PA
- implement control of the output power
- develop an amplifier for the DAC output signal
- add an extra pad for the gating signal of the Frequency Measurement Unit
- insert additional stage(s) to frequency divider in simple chip

4. Finite IF transceiver front-end

4.1. Building block diagram

The block diagram of the designed and manufactured 120-GHz monostatic, superheterodyne sensor with finite-IF is illustrated in Fig. 55.

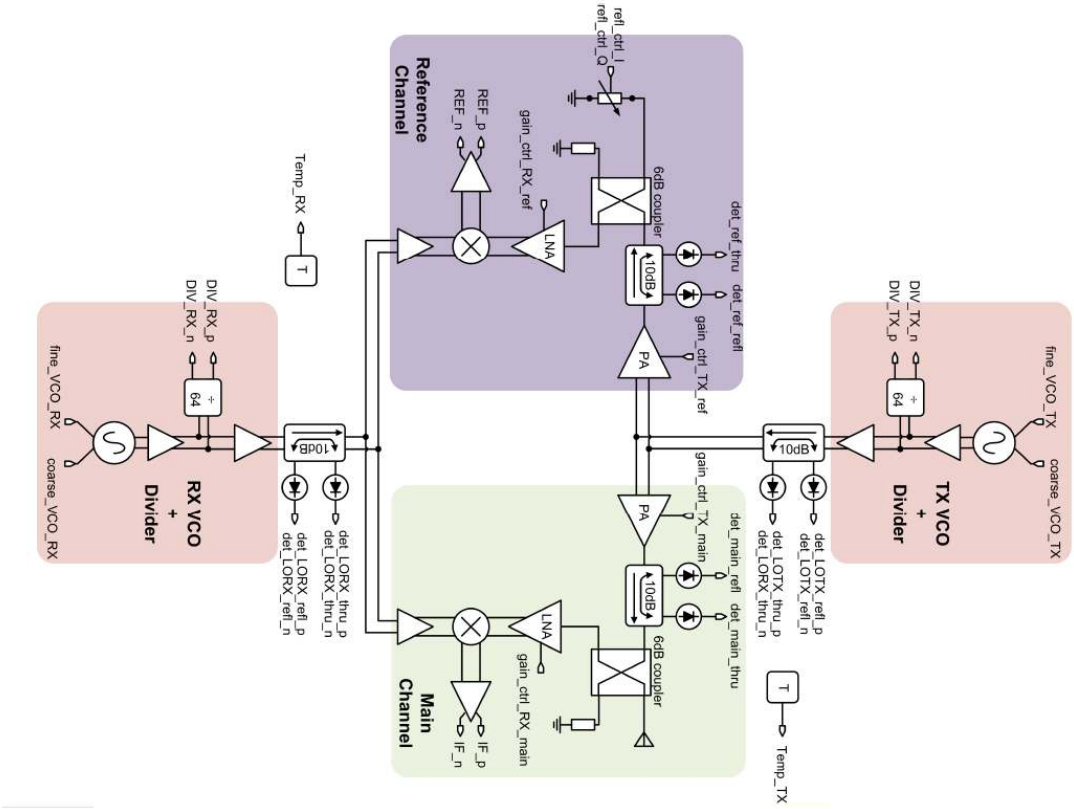


Figure 55. Sensor block diagram.

The system consists of two identical 120-GHz transmit-receive channels, one for distance measurements and one for reference generation. Since two different VCOs are available on chip, full functional 120-GHz loopback for self-test is possible, without employing external mm-wave equipment. The reference channel features a programmable reflective load (instead of the antenna) which can be used for calibration and measurement of the antenna reflection coefficient. The power levels of the 120-GHz signals are monitored with power detectors at various nodes within the chip in order to verify the proper operation of all 120-GHz circuits.

The chip was fabricated in STMicroelectronics' BiCMOS9MW. The die microphotograph of the chip is shown in Fig. 56:

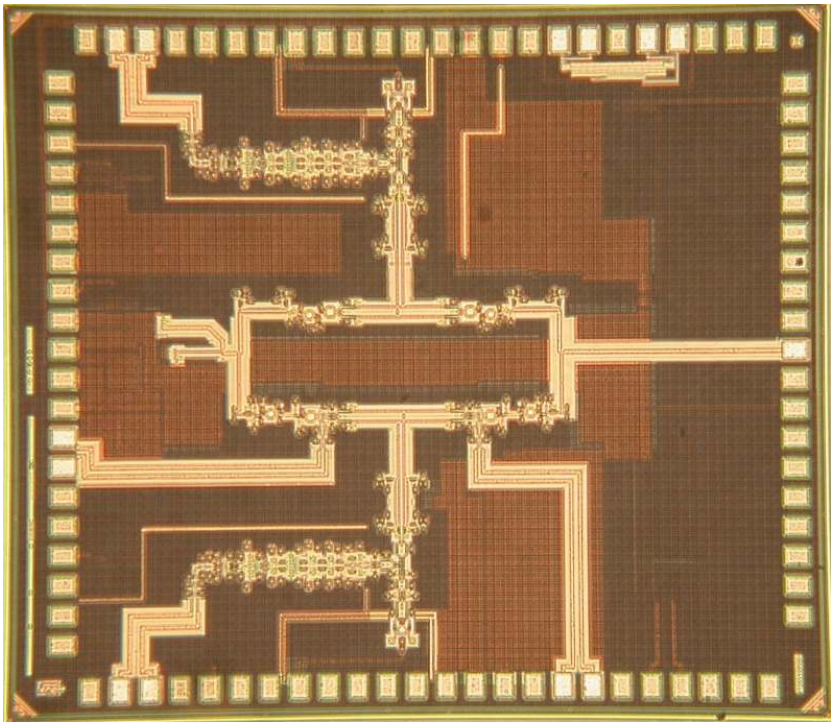


Figure 56. Sensor die photograph.

The chip was partially tested by powering up the RX VCO, LO distribution and divider and monitoring the divider output. The VCO oscillation frequency was found to be 142.5 – 150.2 GHz. This frequency shift of approximately 24 GHz is attributed to layout improvements that were performed in the original version of the VCO and were meant to increase the frequency of oscillation by 2-3 GHz. The change in frequency was higher than originally anticipated and could not be reproduced in simulation due to lack of a model for the thin-oxide, accumulation-mode varactor.

Several breakouts were manufactured in order to evaluate the performance of the individual blocks of the 122 GHz.

4.2 Transceiver breakouts

4.2.1 Receiver Breakout

The block diagram and die microphotograph of the receiver breakout are shown in Fig. 57.

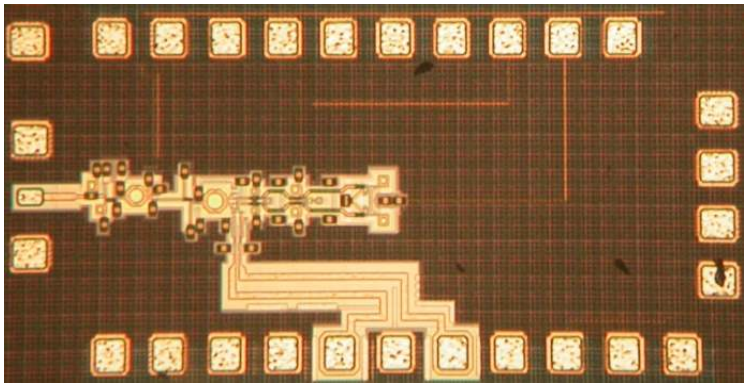


Figure 57. Receiver breakout block diagram and die photograph.

The receiver breakout is composed of the VCO, two VCO buffers, a double sideband Gilbert cell mixer and a low noise amplifier. With this breakout, we can reproduce and test the largest portion of the two receivers of the TXRX system. Figs. 58, 59, 60 and 61 illustrate the downconversion gain, noise figure and tuning range of the VCO as measured in the receiver breakout.

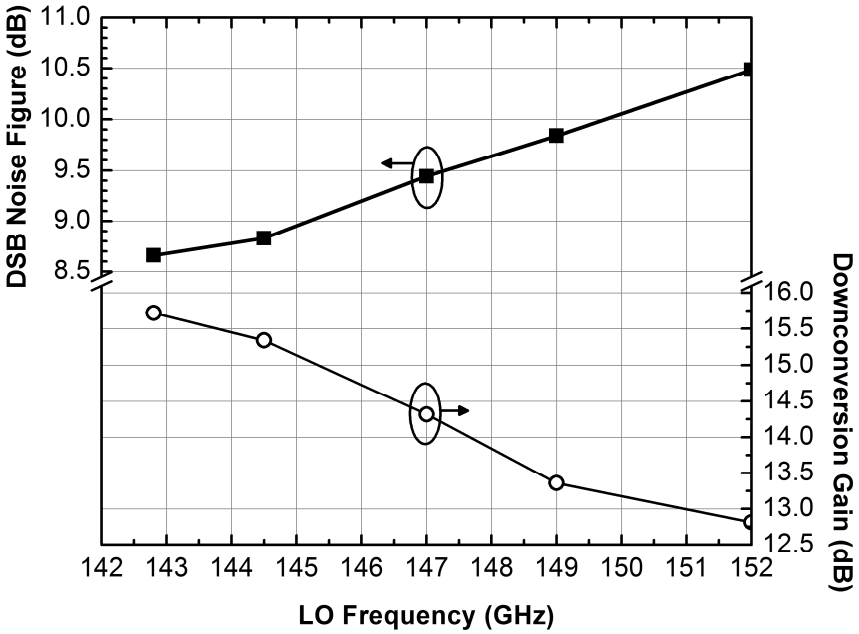


Figure 58. Gain and double sideband noise figure at a constant IF of 750 MHz versus LO frequency.

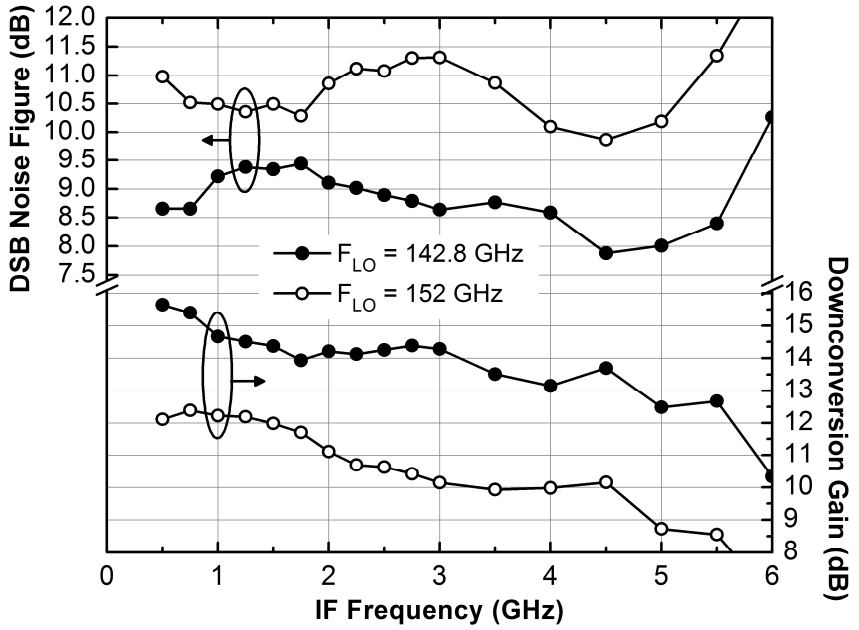


Figure 59. Gain and double sideband noise figure at constant LO frequency versus IF frequency. De-embedding of the mm-wave setup is performed at the LO frequency at and is increasingly inaccurate at higher IF frequencies.

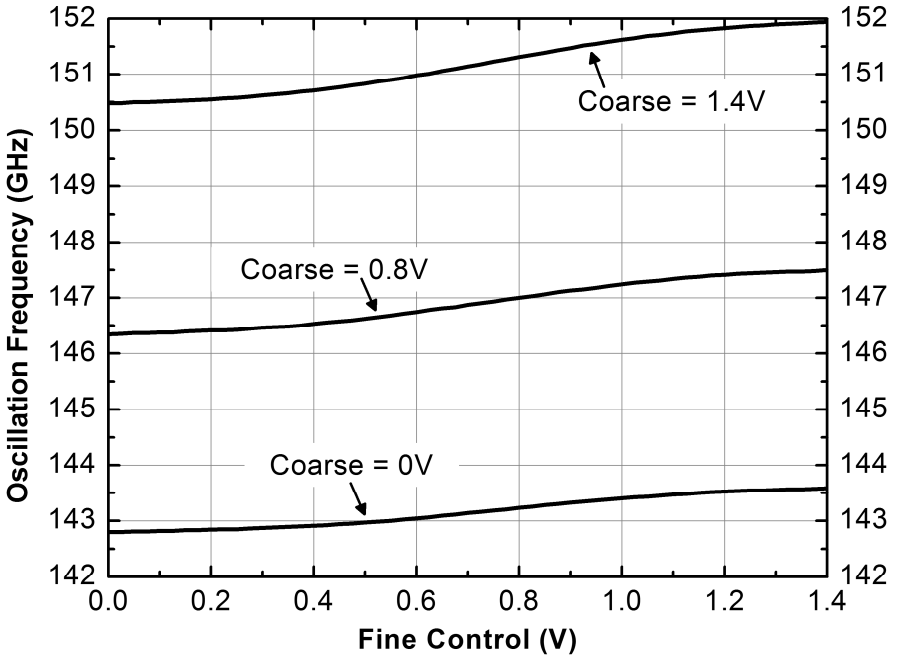


Figure 60. Tuning range of the VCO measured in the receiver breakout.

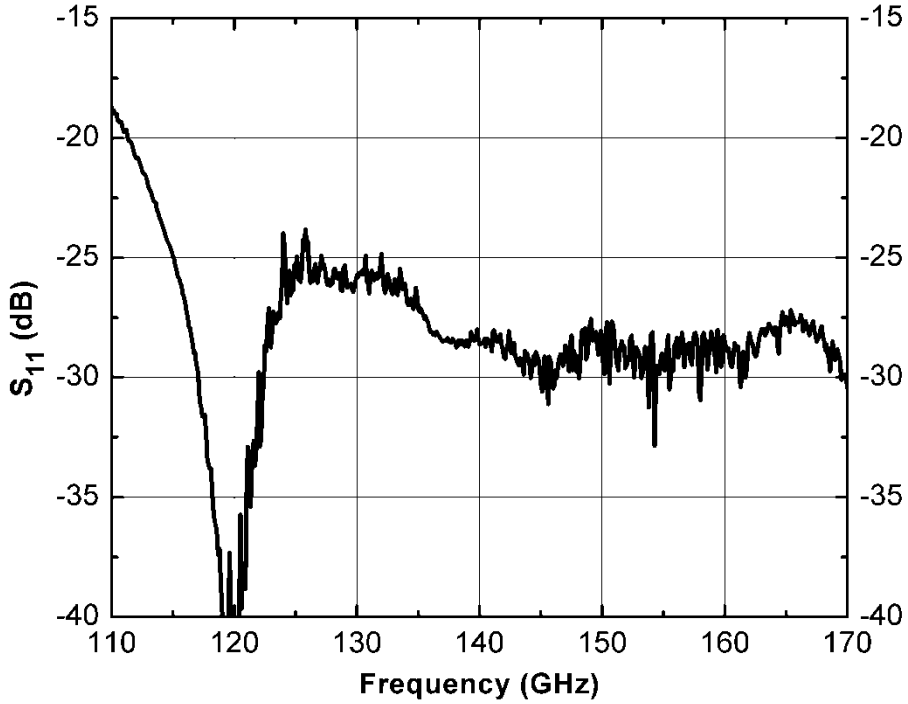


Figure 61. **Measured** S_{11} of the receiver breakout.

4.2.2 LNA Breakout

A separate breakout of the low noise amplifier was manufactured and is shown in Fig. 62.

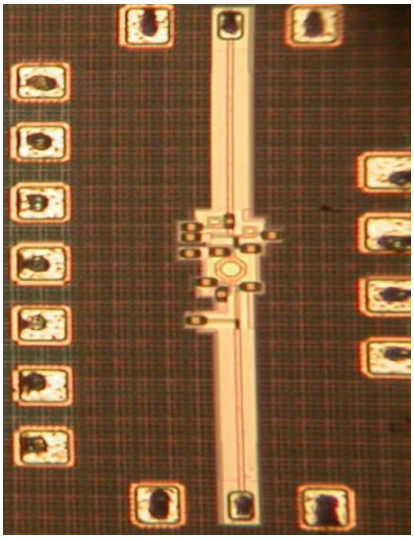


Figure 62. LNA breakout die photograph.

The LNA was modified with respect to the version in the sensor system in order to facilitate output matching to 50 Ω. (In the system, it is conjugately matched to the mixer input impedance). The measured S-parameters of the LNA are reproduced in Fig. 63.

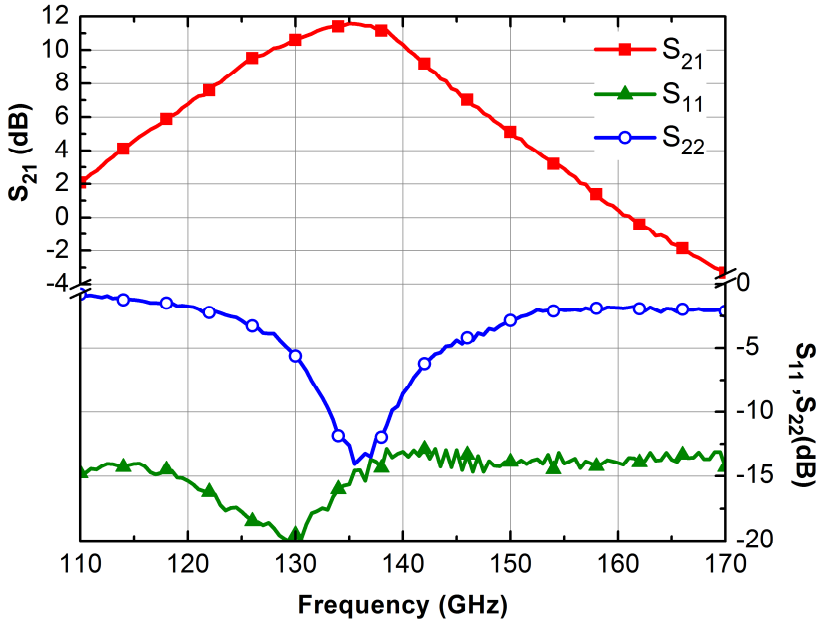


Figure 63. Measured LNA S-parameters.

4.2.3 Divider Chain Breakout

Two divider chain breakouts where manufactured. One consists of the VCO and the divide-by-64 chain and is shown in Fig. 64 while the other consists of the divide-by-32 (from approximately 60 GHz down to 2 GHz). This arrangement is necessary since it is difficult to measure the sensitivity of the divider chain above 110 GHz due to the low output power of the available D-Band signal source.

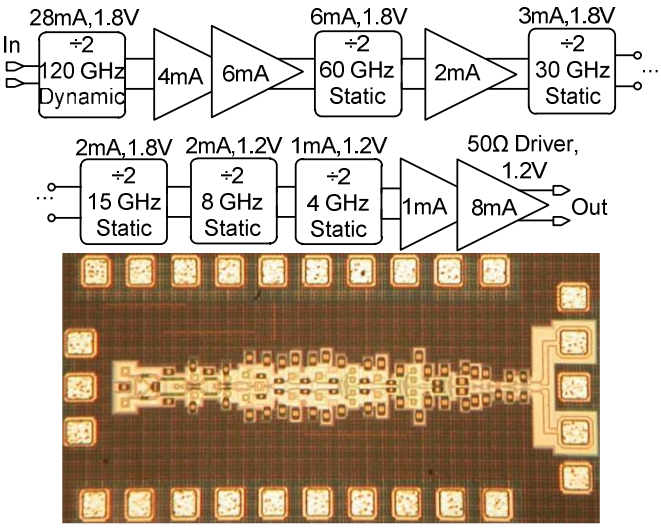


Figure 64. Divide-by-64 chain block diagram and breakout die microphotograph. The breakout includes the divider chain and VCO.

The division range of the divide-by-64 chain was found to extend to at least 150.2 GHz, the highest frequency of oscillation of the VCO in the divider breakout.
The die photograph of the divide-by-32 chain along with its measured sensitivity is illustrated in Fig. 65.

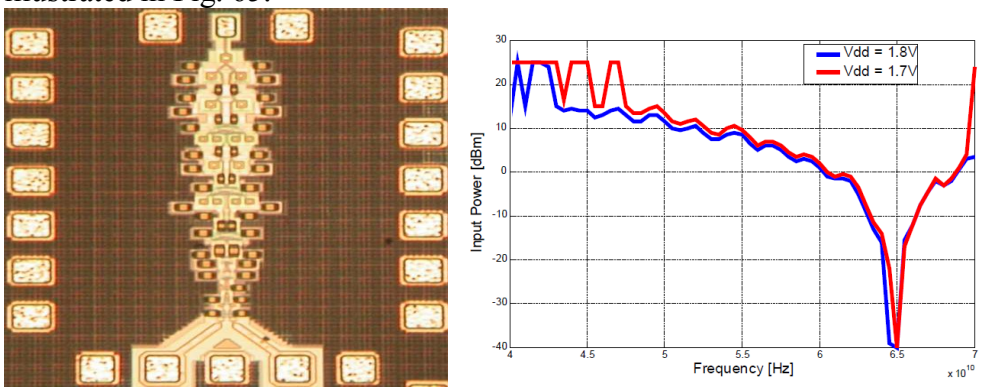


Figure 65. a) Die microphotograph of the divide-by-32 chain breakout b) Measured sensitivity curve without de-embedding setup losses.

4.2.4 Power sensor breakout

The die microphotograph of the bi-directional power sensor is shown in Fig. 66 along with its measured S-parameters. The characterization of the power sensor performance over power as well as the S-parameters of the tunable load is currently underway.

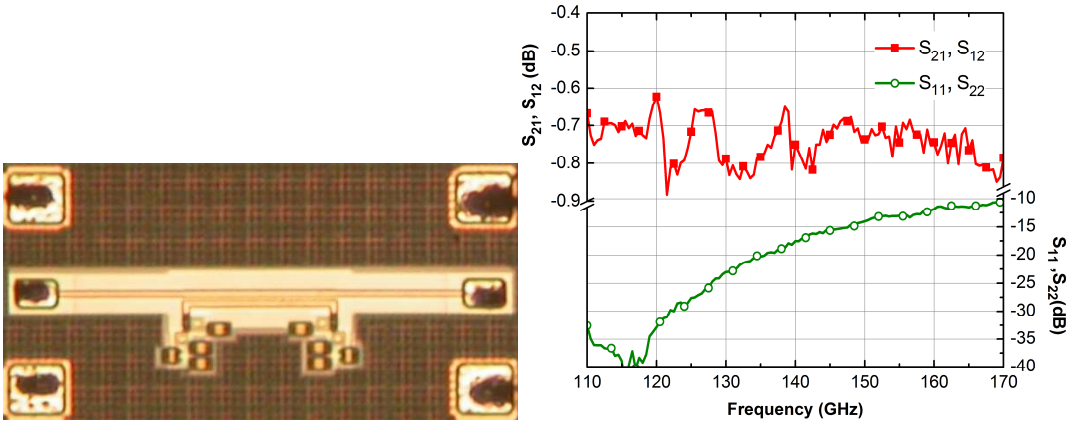


Figure 66. a) Die photograph of the directional couplers with detectors and b) Measured S-parameters.

The main performance parameters of the sensor chip based on die-level sensor and breakout measurements to date are summarized in Table 9.

Table 9: Measured sensor performance to date (VCO phase noise and TX output power not measured yet)

Parameter	P_{DC} [mW]	Tuning range [GHz]	RX NF_{DSB} [dB]	RX Gain [dB]	RX S11 [dB]	Divider range [GHz]
Value	890	143-152	<10.5	>13	<=-20	100-150

4.2.5 Phase-frequency-detector chip

A separate phase-frequency-detector chip that includes a differential charge pump and filter was also designed and manufactured in STMIcroelectronics' SiGe BiCMO9MW process. The chip was verified in an integrated 160-GHz PLL to operate with reference signals as high as 7 GHz and is meant to be used to build external PLLs for all 120-GHz sensors in the SUCCESS project.
The block diagram and the die photogtraph are illustrated in Figs.67 and 68, respectively. The chip is currently being packaged at Robert Bosch GmbH.

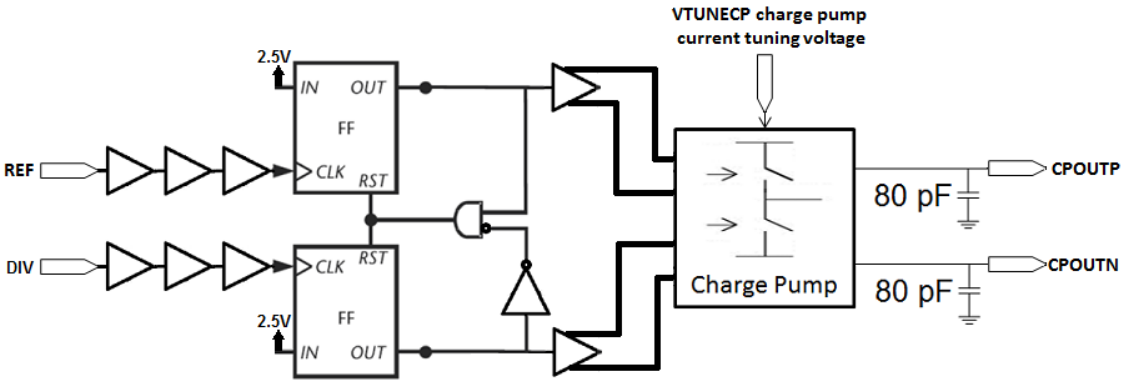


Figure 67. Block diagram of the phase-frequency-detector (PFD) chip.

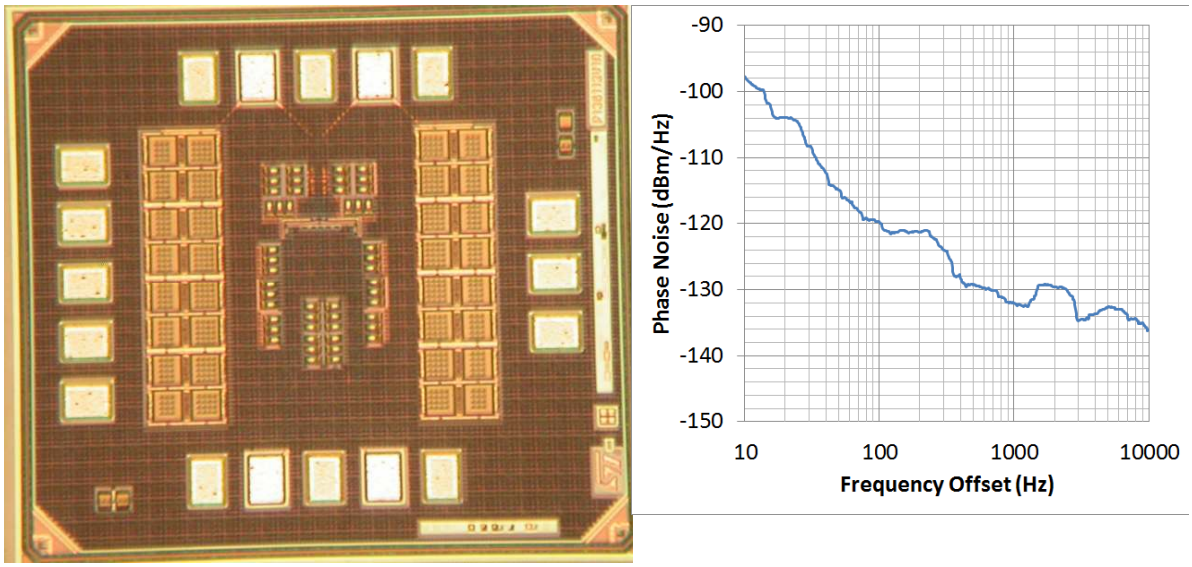


Figure 68. PFD die microphotograph and output noise measured for 700-MHz reference and and divider inputs to the PFD.

Conclusions and Future Work

The sensor chip and associated phase-frequency-detector have been designed fabricated and partially tested on die. Except for the frequency range of the VCO, which is higher than expected by 18-20%, everything appears to be in spec. The sensor is currently being packaged and will be fully characterized, along with its self-test capabilities.

Due to the shift in the VCO frequency, the antenna will be redesigned to operate in the 145-GHz range.

After validating the system operation and performance, the sensor will be redesigned in order to reduce the center frequency to the desired value of 122.5 GHz. This should not be a problem since an earlier version of the VCO, centered on 120 GHz was fabricated and tested in 2010.

The corrective tapeout is scheduled for the first quarter of 2012 in STMicroelectronics' BiCMOS9MW process.