Large Scale Collaborative Project

DOTFIVE

Towards 0.5 TeraHertz Silicon / Germanium Heterojunction bipolar technology

FP7 Contract Number: 216110

WP2 – Evolutionary technology concepts

Deliverable report

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Content

Section 1 - Executive summary

1.1 Description of the deliverable content and purpose

The objective of this deliverable is to provide the final status on the work done at STMicroelectronics within WP2. Process developments carried out on DPSA-SEG SiGe HBT architecture and related electrical results are detailed. First, results from last development phase - i.e. related to B4T technology - are updated, especially because electrical targets have been modified based on WP5 circuits results. Second, process trials targeting B5T technology are presented and analysed. It is shown that the final objective of 500 GHz f_{MAX} will not be met. A comparison with results obtained for other technologies studied in WP2 and WP3 shows the limitations of the DPSA-SEG architecture. Based on the developments done in WP3, proposals are made to overcome these limitations.

1.2 Brief description of the state of the art and the innovation brought

Results presented in [1] and summarized in Figure 1 show that f_T and f_{MAX} values of 300 GHz and 400 GHz respectively could be obtained simultaneously. They also confirm the well known trade-off between f_T and f_{MAX} related to the collector and base doping levels. One could be rather optimistic based on these results, since they were obtained with 110-nm wide emitters. Indeed, based on studies published in [2], f_{MAX} increase could be expected by further reduction of the emitter width. However, work described in [2] also pointed to the main risk associated with narrow emitters, which is the decrease of the transit frequency f_T due to the increase of the emitter resistance R_E. Therefore, developments were focused on two main aspects:

1. Evaluating a further lateral shrink based on B4T vertical profile
2. Investigating a shrink of the vertical profile in order to anticipate a degradation of f_T due to the lateral shrink

It is also worth pointing out that initial electrical targets of B4T technology have been revised, since better circuits results have been demonstrated in [3] with process changes leading to a larger f_T (and lower f_{MAX}). Therefore, B4T specifications have been modified from 250 GHz f_T / 400 GHz f_{MAX} to 270 GHz f_T / 370 GHz f_{MAX}. Although the modification at technology level was limited (increase of collector doping), this represented an important step since it brought back into question the objective of the project to focus on increasing f_{MAX} while circuit results indicate the advantage of a more balanced device design. The evolution of HF performances between BiCMOS9MW and B5T (target) is plotted in Figure 2. Final B5T results are not yet available since the lot gathering all the developments presented in Section 1.5 is not yet completed its fabrication. However, it is very likely that the B5T objective will not be met with respect to f_{MAX}. Reaching f_T = 300 GHz looks feasible, even if the reduction of the emitter width anticipated to increase f_{MAX} penalizes the emitter resistance. However, 450 GHz f_{MAX} seems out of reach since the reduction of the process thermal budget, applied to increase f_T, degrades the extrinsic base resistance. Therefore, ~ 400 GHz f_{MAX} appears to be the upper limit for this technology for $f_T \geq 300$ GHz… Although this is ~100 GHz lower in f_{MAX} (cf. Figure 6) compared to the best obtained results [4], results obtained by ST in the project are still at the state-of-the-art for the DPSA-SEG architecture [5].

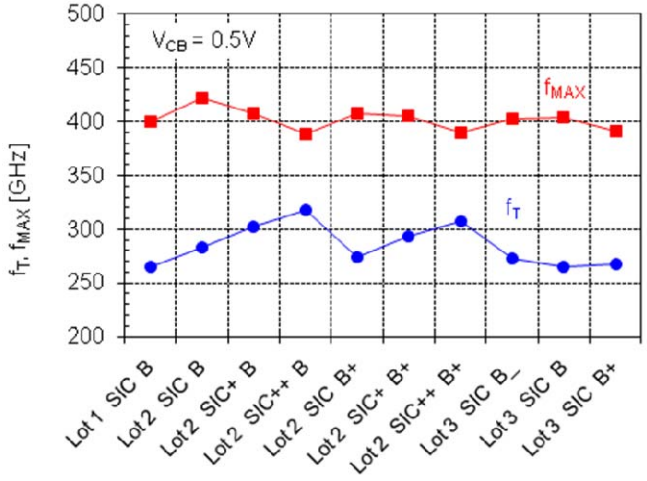

Figure 1: f_T, f_{MAX} performances measured on 10 splits from 3 different lots using 400GHz f_{MAX} SiGe HBT technology (wafer average values for 0.11×4.9µm² transistors)

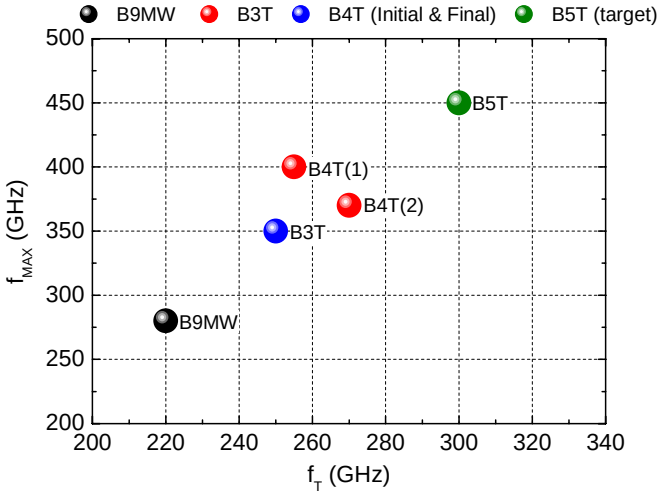

Figure 2: f_T, f_{MAX} performances evolution between BiCMOS9MW and B5T (target) – 1: B9MW to B3T: Vertical & lateral scaling – 2: B3T to B4T(1): Lateral scaling only – 3: B4T(1) to B4T(2) : Vertical scaling (increased collector doping) – 4: B4T(2) to B5T: Vertical & lateral scaling.

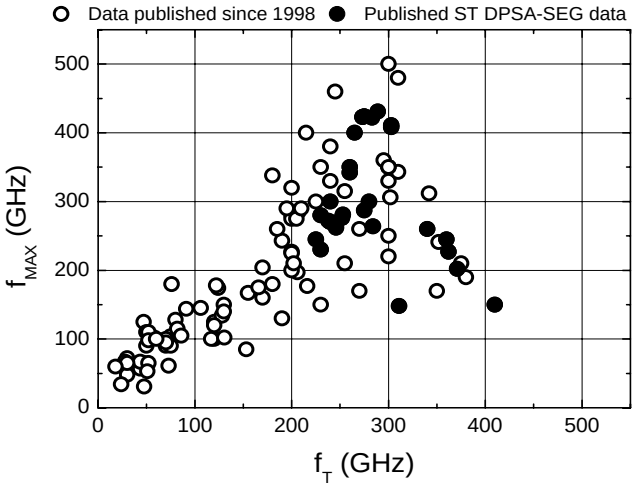

Figure 3: f_{MAX} vs f_T plot highlighting ST results obtained with DPSA-SEG architecture among all published data since 1998 (including recent DOTFIVE results to be published at BCTM'11).

1.3 Deviation from objectives

There is no deviation with respect to the work done in the project. However ST will not achieve 500 GHz f_{MAX} with its DPSA-SEG architecture. Explanations concerning the limitations of thisarchitecture are given in Section 1.7. However, data on ring oscillator gate delay are expected for the final review, and the 2.5 ps objective may still be met.

1.4 If relevant: corrective actions

No corrective action is planned today, since not being able to meet the 500 GHz f_{MAX} objective with DPSA-SEG architecture is not considered as a deviation from objectives, but rather as one of the conclusions of the project.

1.5 Technological progress

As mentioned in Section 1.2, technological progress focused on one hand on the evaluation of a further lateral shrink based on B4T vertical profile, and on the other hand on the shrink of the vertical profile in order to anticipate a degradation of f_T due to the lateral shrink. 3 lots of 25 wafers, combining trials on both vertical and lateral scaling, have been used for these studies (J030PGT, J040TCP and J047RPR).
Experiments on the downscaling of the vertical profile were based on the studies published in [6] and therefore could be considered as 'conventional'. They included variations on buried layer doping and collector doping (SIC), reduction of the spike annealing temperature from 1080°C to 1050°C, and adaptation of the base profile to the modified thermal budget. Variations on base doping concentration have been performed too. Furthermore, ion implantations determining values of resistances offered in the Design Kit have been modified in order to account for changes in activation annealing temperature.
Most of the efforts were devoted to the lateral shrink, with the development of 193-nm lithography both for emitter window and polyemitter patterning. This led to significant process changes, since the SIC module had to be moved before the emitter window patterning in order to cope with the reduced resist thickness. This change had a major impact on base cavity opening [7]. The inside spacer module has also been modified, in order to reduce the spacer width from ~75nm to ~40nm, and the associated extrinsic base resistance component. Figure 4 shows the evolution of collector current (I_C), base current (I_B), and effective emitter width (W_E) with emitter window opening, using 193-nm lithography. It demonstrates that W_E as narrow as 45nm, illustrated in Figure 5 (left), can be achieved without using any Optical Proximity Correction. Moreover, Figure 5 (right) shows that emitter window lengths as small as 0.4 µm can be defined for an emitter window width of 0.19 µm, again without any OPC.

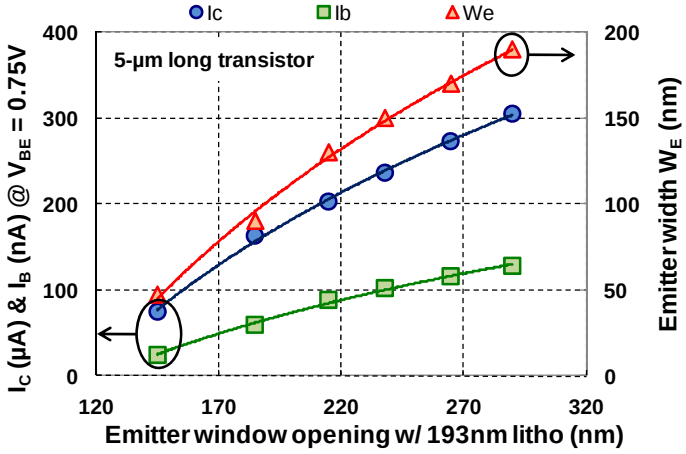

Figure 4: Evolution of the collector (I_C) and base (I_B) currents, and of the effective emitter width (W_E) with the emitter window opening obtained by using 193-nm lithography & modified inside spacers' module.

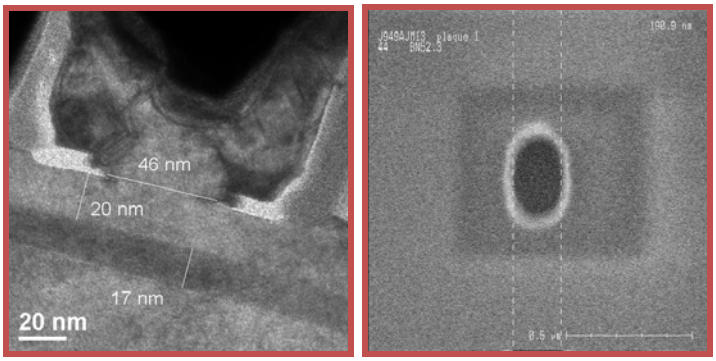

Figure 5: Cross-section of a transistor with an effective emitter width (W_E) of 45nm (left) and top view of 190-nm wide and 400-nm long emitter window opening (right), both obtained by using 193-nm lithography.

1.6 Analysis of the results

Results obtained on vertical scaling experiments performed on the 3 lots aforementioned are summarized in Figure 6. They show that while the f_T increase was successful, not surprisingly, it was accompanied by a decrease of f_{MAX}. As explained in Section 1.2, it is the objective of the lateral scaling to increase f_{MAX} by reducing both the base resistance (intrinsic part related to W_E) and the collector/base capacitance (related to the collector/base junction area). Figure 7 presents the evolution of f_T and f_{MAX} with the emitter window width for 2 vertical profiles, which are potential candidates for the B5T technology. It confirms that f_T is negatively impacted by the increase of the emitter resistance. This penalizes the increase of f_{MAX} brought by the reduction of the intrinsic base resistance. f_{MAX} suffers from the extrinsic base resistance, which is degraded by the reduction of the thermal budget too.
The process and layout modifications selected for the B5T technology (last ST run), compared to the B4T technology, can be summarized as follows:

- Increase of the collector doping (buried layer)
- Reduction of the spike annealing temperature from 1080°C to 1050°C
- Modification of the base profile accordingly, and increase of the base doping to minimize the degradation of the base resistance
- Reduction of the emitter window width from 230 nm to 180 nm, but modification of the inside spacer module to get the same final effective emitter width (100 nm).

Electrical results from the actual B5T technology are expected end of August 2011. f_{MAX} is not expected to exceed 400 GHz (f_T ~300 GHz).

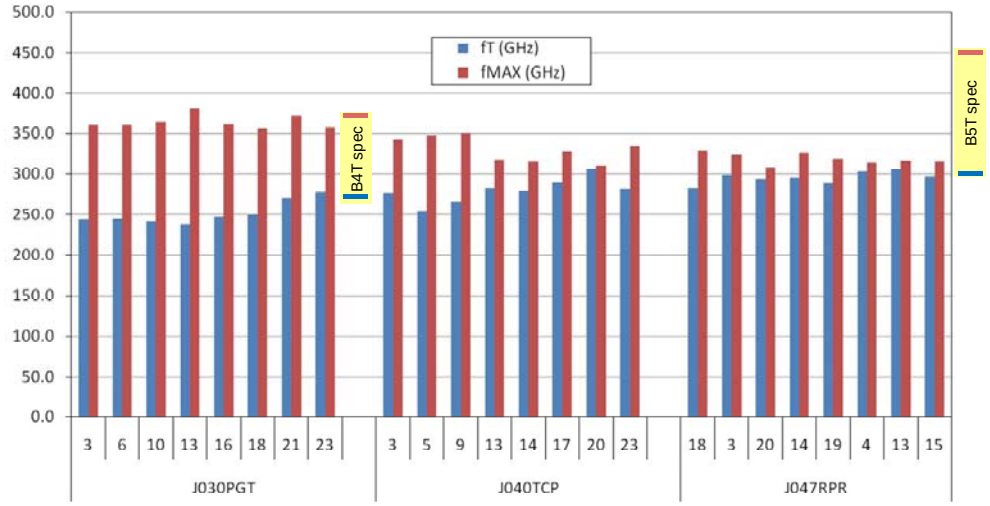

Figure 6: f_T, f_{MAX} performances measured on 24 splits done on vertical profile from 3 different lots with B4T design rules (wafer average values for 0.11×4.9µm² transistors)

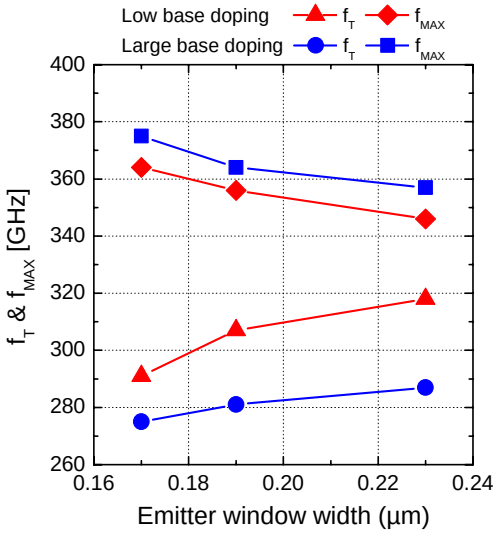

Figure 7: f_T, f_{MAX} evolution with the emitter window width for 2 different process splits on base doping performed on lot J040TCP.

1.7 Impact of the results

The main purpose of these results is to outline the limitations of the DPSA-SEG architecture, as developed by ST. A detailed comparison of the results obtained on the various architectures investigated in WP2 and WP3 has been done in the frame of an invited paper at the 2011 Bipolar/BiCMOS Technology Meeting [5]. The first generation of ST B4T technology, i.e. with reduced collector doping, is compared to other DOTFIVE partners' architectures in Table 1. B4T technology exhibits the largest base resistance (cf. $(R_B+R_E)\times L_E$). A better result is obtained on IFX DPSA-SEG HBT, which could be explained by the possibility offered in this technology to optimize the base link resistance independently from the final anneal (not possible in ST technology due to the constraint of CMOS compatibility). These electrical parameters (obtained by a model parameter extraction) are not yet available for ST B5T technology, but it is expected that the base resistance will be even larger due to the increased weight of the extrinsic component R_{Bx}. Therefore, any reduction of the intrinsic base resistance component, brought by the emitter width reduction, is counterbalanced by an increase of R_{Bx}. A reduction of R_{Bx} with the current architecture may be possible by modyfying the ion implantation conditions of the polybase, or by replacing it by a boron in-situ doped polybase. However, a strong reduction of R_{Bx} to the value of the IHP2 HBT in Table 1 will likely require a similar technological solution as the ones developed for the IHP2 and IMEC HBTs, i.e. the deposition of the external base after the growth of the intrinsic base.

This is a very important conclusion since developments done at ST on DPSA-SEG SiGe HBT architecture are being used for the start of a new BiCMOS technology based on 55nm CMOS. Indeed, the final spike annealing temperature in 55nm CMOS is 1050°C and therefore the same f_{MAX} limitation due to R_{Bx} is anticipated. Evaluations have started to determine whether major architecture modifications have to be adopted in 55 nm SiGe BiCMOS, based on the electrical specifications currently being discussed with ST customers.

Table 1 Comparison of the main electrical characteristic of the different HBTs developed in DotFive (from [5])

Parameter	Unit	IFX	ST	IHP1	IMEC	IHP2
W_E	µm	0.13	0.10	0.16	0.08	0.12
L_E	µm	2.70	4.90	0.93	0.93	0.96
n_E	-	1	1	2	1	8
Contacts #	-	1E/1B/1C	1E/2B/2C	2E/2B/2C	1E/2B/1C	8E/8B/8C
A_E	µm²	0.351	0.490	0.298	0.074	0.922
Peak f_T	GHz	240	260	300	215	300
$J_{C,peak}$	mA/µm²	10.0	14.3	16.0	17.5	18.5
f_{MAX}	GHz	380	400	350	400	500
β (V_{BE}, V)	-	1300 (0.6)	2100 (0.65)	250 (0.87)	800 (0.75)	700 (0.7)
BV_{EBO}	V	2.3	1.7	1.5	2.1	1.7
BV_{CBO}	V	5.5	6.0	4.3	5.2	5.2
BV_{CEO}	V	1.50	1.55	1.85	1.70	1.60
V_A	V	110	270	85	60	180
Rs_{pbi}	kΩ/sq	2.6	2.5	3.3	2.7	2.6
C_{BE}	fF	5.2	9.7	4.4	2.7	20.1
C_{BC}	fF	3.5	6.1	3.4	1.6	13.9
C_{CS}	fF	2.4	4.1	4.0	4.3	8.5
R_E	Ω	3.8	2.3	6.5	40.0	2.3
R_B	Ω	28.2	24.0	51.1	35.0	4.7
R_{CX}	Ω	9.2	4.0	10.5	-	4.8
τ_D	ps	2.4	-	2.5	-	2.0
$R_E \times A_E$	Ω.µm²	1.33	1.13	1.93	2.98	2.12
$(R_B+R_E) \times L_E$	Ω.µm	86	129	107	70	54
$R_{CX} \times A_E$	Ω.µm²	3.23	1.96	3.12	-	5.21
C_{BE} / A_E	fF/µm²	14.8	19.8	14.8	36.3	21.8
C_{BC} / A_E	fF/µm²	10.0	12.4	11.4	20.8	15.1
C_{CS} / A_E	fF/µm²	6.8	8.4	13.4	57.8	9.2

I am not aware of any time constant that contains Rcx*AE. In my opinion, a better figure would be Rcx*LE (all devices considered have sufficiently long fingers), assuming the distance between C and E contact edge to be similar for all processes.

1.8 IPR

NA.

1.9 Publishable information

An invited paper is going to be published at the 2011 Bipolar/BiCMOS Circuits and Technology Meeting [5]. This paper, written in cooperation with all partners involved in WP2 and WP3 (ST, IFX, IHP and IMEC), presents the status of the technogical developments done within the Project.

1.10 Conclusion

State-of-the-art results have been demonstrated for the DPSA-SEG SiGe HBT architecture, whose main advantage is to offer an overall simple fabrication process. Furthermore, manufacturability of this solution has been demonstrated since the 2 partners involved in

WP2 use this architecture for technologies already in production (B7HF200 at IFX and BiCMOS9MW at ST). The limitations of this architecture have been clearly identified however, and 400 GHz f_{MAX} was hardly exceeded (430GHz f_{MAX} is the largest value which has been measured [1]), especially when large f_T values are targeted too. Trials are still ongoing but 300 GHz f_T / 400 GHz f_{MAX} is probably today the best performance trade-off expected from this technology without major process modifications. On the other hand, such performance may be sufficient for next generation BiCMOS which has started at ST on 55 nm CMOS node. 55 nm SiGe BiCMOS will largely benefit from the developments done in DOTFIVE. It is also possible that a larger f_{MAX} will be targeted in 55 nm BiCMOS. If this is the case, developments done in WP3 give some clues since the main limitations of the DPSA-SEG architectures have been successfully adressed in this workpackage. Indeed, as could be expected, the best results in DOTFIVE have been obtained with the new architectures developed in WP3 [4][8]. Of course, some innovations are available at the expense of process complexity but developments done by IHP in WP3 open up the road for the modifications to be done to overcome the limitations of the conventional DPSA-SEG architecture [9][10].

Section 2 - Annex

2.1 References

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