Large Scale Collaborative Project

DOTFIVE

Towards 0.5 TeraHertz Silicon / Germanium Heterojunction bipolar technology

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WP2 – Evolutionary technology concepts

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Content

Section 1 - Executive summary

1.1 Description of the deliverable content and purpose (1 page max)

The manufacturability of the double-polysilicon self-aligned (DPSA) HBT architecture, in which the SiGe base is integrated by selective epitaxial growth (SEG), is well established and the transistor architecture is now employed by several companies for industrial production. One of the main objectives of WP2 in DOTFIVE was to evolutionary evaluate the potential of the conventional DPSA-SEG HBT architecture for further performance improvements in order to achieve goals such as 2.5 ps ring oscillator gate delay time (τ_D) and 500 GHz maximum oscillation frequency (f_{max}). In this context the starting point of IFX's investigations and developments in DOTFIVE was the SiGe bipolar technology B7HF200, which is using 0.35 µm lithography and which is dedicated to automotive radar applications at 77 GHz. The high speed transistors offered in B7HF200 feature a transit frequency f_T of 190 GHz, a maximum oscillation frequency f_{max} of 250 GHz, and a CML ring oscillator gate delay time τ_D of 4.0 ps. The present report describes the performance progress, which has been achieved by IFX in DOTFIVE with the conventional DPSA HBT. For improving ring oscillator gate delay and maximum oscillation frequency mainly lateral and vertical scaling of the DPSA-SEG HBT has been investigated in numerous iteration steps. In these investigations the lateral dimensions of the emitter/base configuration have been drastically decreased by reducing emitter window width, emitter/base spacer width, and critical overlaps. Vertical scaling included the development of new SiGe base profiles with increased Ge fraction, the investigation and improvement of the base link annealing cycles, as well as a significant reduction of collector thickness.

1.2 Brief description of the state of the art and the innovation brought (1 page max)

The worldwide best published values for maximum oscillation frequency and ring oscillator gate delay time stem now from partners of the DOTFIVE consortium [1]. The best values of 500 GHz f_{max} and 2.0 ps ring oscillator gate delay time have been achieved by the developments of IHP in WP3 [2]. The developments of ST have provided an f_{max} of 430 GHz for the case of the conventional DPSA-SEG HBT [3], which is at the state of the art for this architecture. The best values for f_{max} and τ_D, which have been reported from companies or institutes outside of the DOTFIVE consortium, are 350 GHz f_{max} and 3.26 ps τ_D, respectively [4].
The present state of the art for SiGe bipolar production technologies is for example well represented by IFX's SiGe bipolar technology B7HF200, which is qualified according to automotive standards. The conventional DPSA-SEG HBT of B7HF200 features an f_{max} of 250 GHz and a τ_D of 4 ps. The target of IFX in WP2 was to evolutionary increase the performances of the conventional DPSA-SEG HBT. Consequently mainly lateral and vertical scaling has been performed on the HBT of IFX's initial technology B7HF200 in DOTFIVE. These investigations have now led to an HBT technology with considerably increased HF performances. As it is shown in this deliverable report, now values for maximum oscillation frequency of 380 GHz and values of 2.4 ps for ring oscillator gate delay time have been realized with IFX's scaled DPSA-SEG HBT technology. The 2.4 ps ring oscillator gate delay, obtained by IFX in the project are state of the art for the conventional DPSA-SEG architecture.

1.3 Deviation from objectives

The realized values for the ring oscillator gate delay time meet the 2.5 ps τ_D objective in the project. However, on contrary to the HBT developments in WP3, the other DOTFIVE performance target of 500 GHz f_{max} could not be realized by IFX with the DPSA-SEG HBT.

This is mainly explained by the disadvantage of the conventional DPSA-SEG HBT in providing a higher base link resistance in comparison to the HBT structures investigated in WP3 [1]. On the other hand IFX probably could not yet fully exhaust the performance potential of the conventional DPSA-SEG HBT. This may have been partly caused by the time consuming developments, which were necessary for the change from 0.35 µm i-line to DUV lithography. In DOTFIVE this implementation of advanced DUV lithography has required the introduction of wafer shuttles between the 0.35 µm fabrication site in Regensburg and the 90 nm CMOS fab in Dresden.

1.4 If relevant: corrective actions

None.

1.5 Technological progress

Fig. 1 shows a schematic cross section of the emitter/base structure in which the intrinsic and extrinsic contributions to the base resistance, the base/collector capacitance and the emitter/base capacitance are shown. From this figure it is clear that the reduction of the emitter window width W_{EW} simultaneously decreases the contributions from the intrinsic transistor to collector/base capacitance, base resistance, and emitter/base capacitance. A reduction of the emitter polysilicon width W_{EP} reduces the parasitic oxide capacitance CBEox and also shortens the path of the base current through the non silicided part of the base poly electrodes. Therefore, both base resistance and emitter/base capacitance are reduced by this measure. Furthermore, a reduction of the active area width W_{AA} decreases base/collector capacitance by a reduction of the parasitic oxide capacitance contribution CBCox. Finally a reduction of the emitter/base spacer width shortens the path of the base current through the SiGe base and therefore decreases the base resistance.

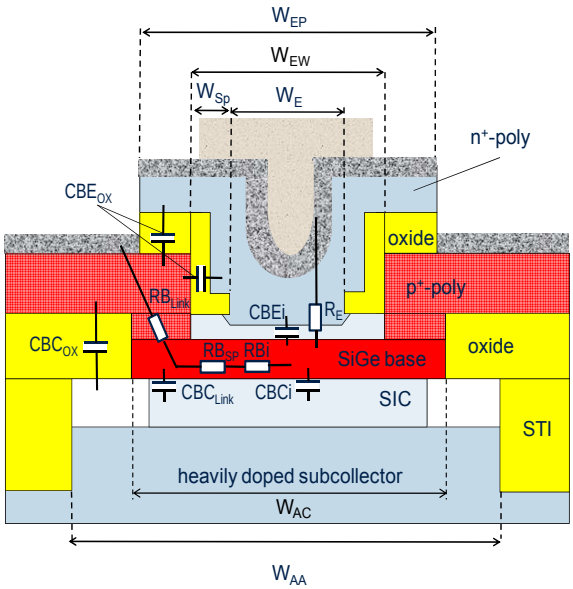
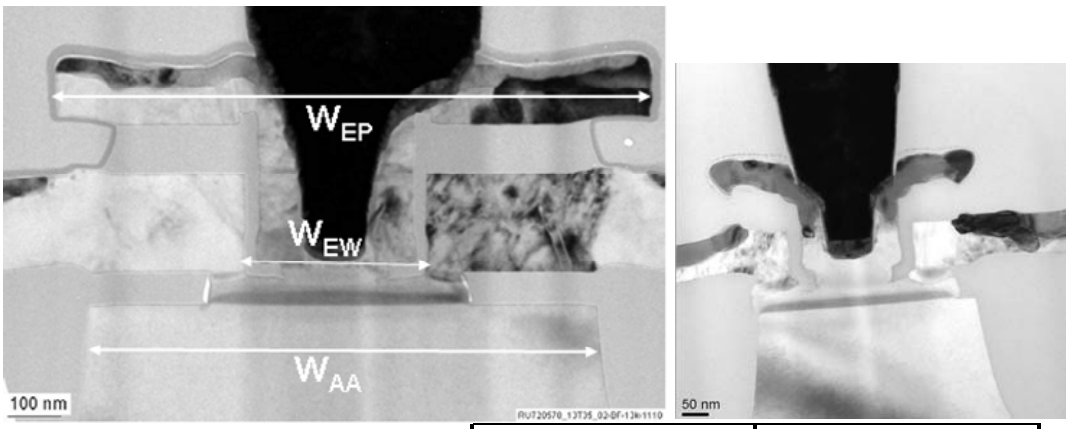


Fig. 1: Capacitances and resistances in DPSA-SEG HBT

Infineon's initial technology B7HF200 uses 0.35 µm i-line lithography. Therefore, lateral scaling of the emitter/base configuration has required the implementation of DUV lithography which was not available at the fabrication site in Regensburg. Via wafer shuttles to the 90 nm fabrication site in Dresden the access of an advanced 248 nm DUV scanner has been

become possible for the DOTFIVE developments. After the various process developments (e. g. modification of reactive ion etching processes), the DUV scanner is now routinely used for the fabrication of the scaled HBT technology at 4 lithographic mask steps (STI, emitter window, emitter polysilicon, contact). The introduction of these new lithographic mask steps into the HBT fabrication process was necessary to decrease emitter window width W_{EW} as well as to benefit from the small alignment tolerances of the DUV scanner for reducing critical overlaps in the transistor.
The progress of IFX in lateral scaling of the emitter/base configuration, which has been achieved in DOTFIVE, is clearly evident from the TEM cross sections shown in Fig. 2. These cross sections compare a SiGe HBT in the B7HF200 process and an HBT in the scaled technology.



	B7HF200 HBT	Scaled HBT
Emitter window width W_{EW}	350 nm	230 nm
Emitter width W_E	200 nm	130 nm
E/B Spacer width W_{SP}	70 nm	50 nm
Active area width W_{AA}	1000 nm	410 nm
Collector junction width W_{AC}	500 nm	370 nm
Emitter polysilicon width W_{EP}	1100 nm	470 nm

Fig. 2: TEM cross section of a B7HF200 HBT (left) and of a scaled HBT featuring an effective emitter width W_E of 130 nm

As compared with the B7HF200 HBT, the emitter window width has been reduced from 350 nm to 230 nm and the width of the emitter/base spacer has been decreased from 70 nm to 50 nm. The resulting emitter width W_E of the scaled HBT is 130 nm. For reducing extrinsic capacitances and extrinsic base resistance, both the emitter polysilicon width W_{EP} and the active area width W_{AA} have been decreased by more than a factor of 2. The transistor parameters, discussed before, are all improving with lateral scaling. However, the evolution of emitter resistance is opposite. To keep emitter resistance sufficiently small, the height of the emitter window stack (p^+-polysilicon/oxide) and the emitter polysilicon thickness have been both decreased by about 40% in comparison to B7HF200. Furthermore, the TiSi silicidation module has been replaced by a CoSi silicidation module from the Dresden fab, which has decreased total base resistance by 10% and 20% for p^+-polysilicon thicknesses of 120 nm and 90 nm, respectively.
Together with lateral scaling also several vertical scaling steps were performed. To increase transit frequency tighter Si/SiGe base profiles with an increased Ge fraction of 30% have been employed for the scaled HBT. To increase transit frequency also the thickness of the intrinsic collector has been reduced to 50 nm by more than a factor of 2 in comparison to the B7HF200 HBT. We have also changed from a phosphorous to an arsenic implanted collector

which is helpful for decreasing base/collector capacitance. On the arsenic implanted collector several iteration steps have been performed for optimizing the trade-off between transit frequency and base/collector capacitance. To improve the trade-off between base resistance and transit frequency in the conventional DPSA-SEG HBT also different base link anneal conditions have been investigated (see D2.3.2). Up to now the best results have been found by performing two anneals. The first one, which is serving to reduce the resistance of the base link region, has been done at 1040°C/5s immediately before emitter deposition. The second one has been performed at lower temperature and serves for emitter drive-in before silicidation. The finally chosen IFX DPSA-SEG HBT fabrication process is sketched in the annex.

1.6 Analysis of the results

The DC characteristics of the scaled DPSA-SEG HBTs are found well behaved. The transfer and output characteristics of HBTs with an effective emitter area A_E of 0.13 x 2.7 µm^2 are depicted in Fig. 3 and Fig. 4, respectively.

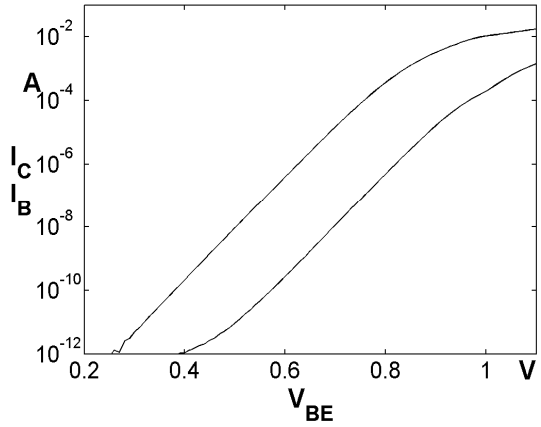


Fig. 3: Transfer characteristic of HBT with A_E = 0.13 x 2.7 µm^2

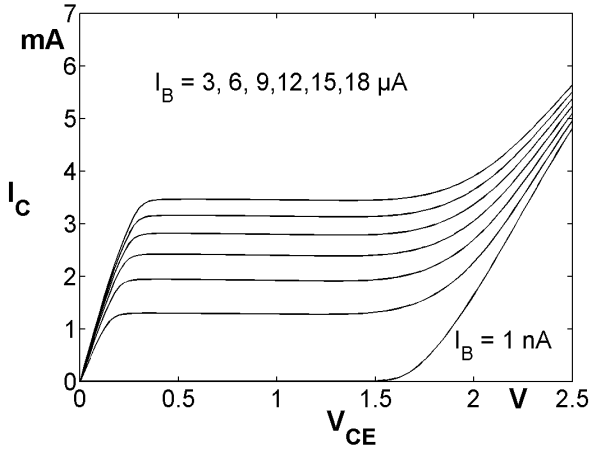


Fig. 4: Output characteristic of HBT with A_E = 0.13 x 2.7 µm^2

The maximum current gain is about 1300 at an emitter/base voltage V_{BE} of ~ 0.6 V. At V_{BE} = 0.8 V a current gain of about 750 is obtained. The intrinsic base sheet resistance is 2.6 kΩ/sq. The transistors have a collector/emitter breakdown voltage BV_{CE0} of 1.5 V and a collector/base breakdown voltage BV_{CB0} of 5.5 V. In spite of a significantly reduced

emitter/base spacer width, sufficiently high values for emitter/base breakdown voltage BV_{EB0} of 2.3 V have been obtained at a current of 1 µA.
The results of HF measurements for the transit frequency f_T and maximum oscillation frequency f_{max} are shown in Fig. 5 and Fig. 6 at a collector/base voltage V_{CB} of 0.5 V.

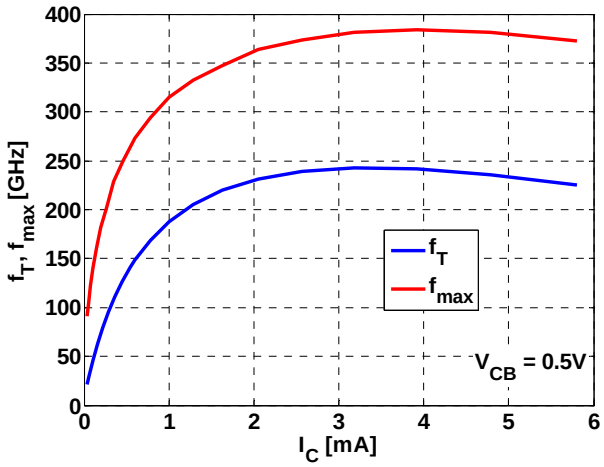


Fig. 5: f_T and f_{max} vs. collector current I_C for transistors with A_E = 0.13 x 2.7 µm^2

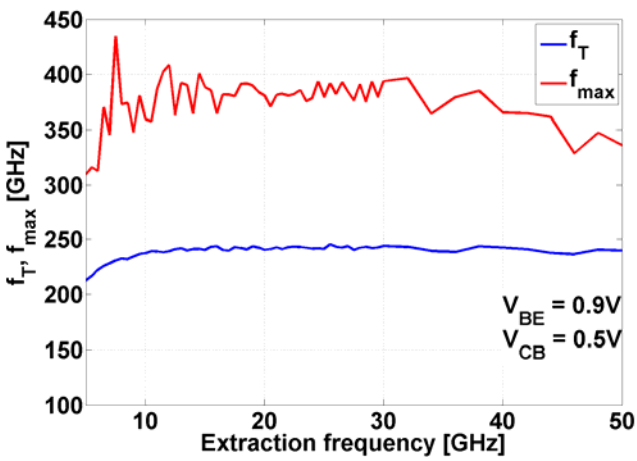


Fig.6: f_T and f_{max} vs. extrapolation frequency (A_E = 0.13 x 2.7 µm^2)

These measurements have been performed on the scaled HBT in the BEC configuration. The transit frequency and the maximum oscillation frequency peak at 240 GHz and 380 GHz, respectively. The peak f_T is reached at a collector current density of 10 mA/µm^2. The f_T and f_{max} curves in Fig. 5 were determined from the frequency dependence of the AC current gain h_{21} and Mason's unilateral gain U, respectively. Fig. 6 shows the transit and maximum oscillation frequency versus extraction frequency. In the frequency range between 10 GHz and 35 GHz the determination of f_T and f_{max} is reasonable independent of the extraction frequency. The f_T vs. I_C and f_{max} vs. I_C curves, which are shown in Fig. 5, have been extrapolated from the frequency dependence of h_{21} and the unilateral gain U in the frequency range between 18 GHz and 22 GHz.
The ring oscillator gate delay time was the main figure of merit for the device optimizations which have been performed at IFX. The gate delay performance of the new technology has been evaluated on our 53 stage CML ring oscillators for laboratory measurements.

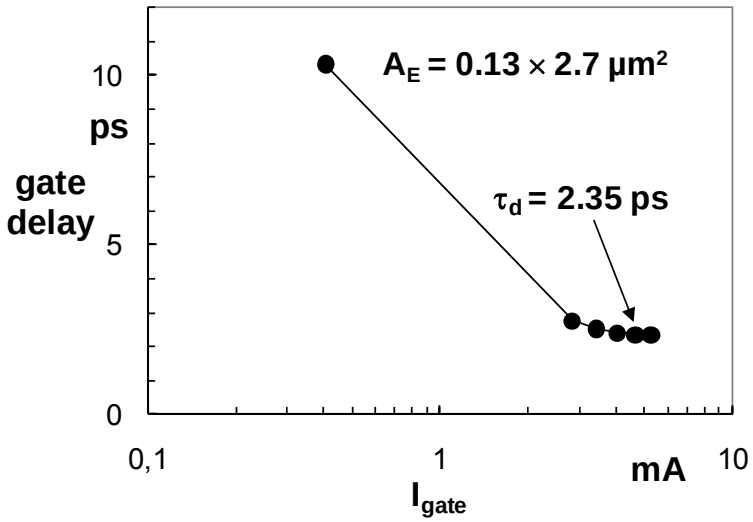


Fig. 7: CML ring oscillator gate delay time vs. current per gate of a scaled HBT with A_E = 0.13 x 2.7 µm^2 and of a B7HF200 HBT with A_E = 0.2 x 2.65 µm^2

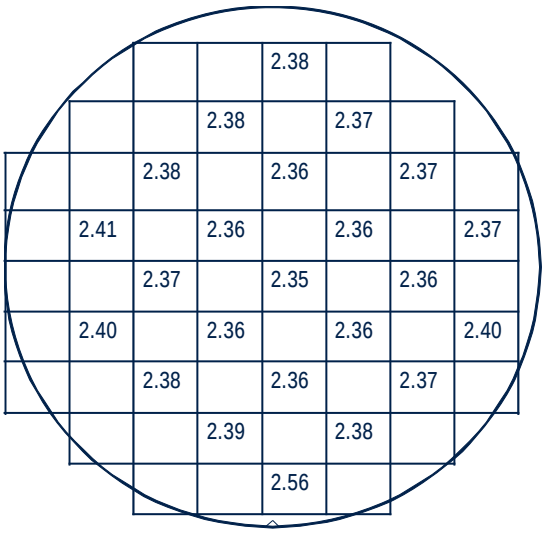


Fig. 8: Wafer map of ring oscillator gate delay time (in ps) at a current per gate of 4.7 mA (mean value: 2.38 ps, emitter area: 0.13 x 2.7 µm^2)

The ring oscillators operate with 2.5 V supply voltage and a single ended voltage swing of 200 mV. The inverter transistors are designed in the BEC configuration and have an effective emitter area of 0.13 x 2.7 µm^2. Fig. 7 shows the dependence of the gate delay time on the current per gate I_{gate}. With the scaled DPSA-SEG HBT technology a minimum gate delay time of 2.35 ps is achieved at I_{gate} = 4.7 mA, which corresponds to a switching current density of ~ 13 mA/µm^2. Fig. 8 shows a wafer map of the gate delay time which has been obtained for an inverter current of 4.7 mA. The mean value of the gate delay time is 2.38 ps and the standard deviation for the variation of the gate delay time over a wafer is 1.7%.
Table 1 summarizes the most important transistor parameters of the new technology which has been realized in this work. For comparison also the corresponding device parameters for an HBT of Infineon's initial technology B7HF200 are shown. The values for emitter/base capacitance C_{EB} and collector/base capacitance C_{BC} have been obtained by s parameter measurements at $V_{BE} = V_{BC} = 0$.

	This work	B7HF200
A_{EW}	0.23 x 2.8 µm^2	0.34 x 2.8 µm^2
A_E	0.13 x 2.7 µm^2	0.2 x 2.65 µm^2
β @ V_{BE} = 0.8 V	750	300
R_{bi}	2.6 kΩ/sq	2.1 kΩ/sq
BV_{EB0}	2.3 V	2.8 V
BV_{CE0}	1.5 V	1.7 V
BV_{CB0}	5.5 V	6.0 V
C_{EB}	5.2 fF	8.0 fF
C_{BC}	3.5 fF	5.1 fF
f_T	240 GHz (V_{CB} = 0.5V)	190 GHz (V_{CB} = 0.5V)
f_{max}	380 GHz (V_{CB} = 0.5V)	250 GHz (V_{CB} = 1V)
τ_D	2.38 ps	4.0 ps

Table 1: Device parameters of a scaled HBT and of a B7HF200 HBT

HV HBT	f_T = 60 GHz, BV_{CB0} = 14 V, BV_{CE0} = 3.5 V
Varactor diode	C(5V)/C(0V) = 2.3, Q @ 77GHz ~ 8
2 poly resistors	150 Ω/sq and 1000 Ω/sq
Metal film resistor	TaN, 20 Ω/sq
MIM capacitor	Al_2O_3 dielectric, 1.4 fF/µm^2

Table 2: Passive and additional active devices in the technology

The scaled HBT has been fabricated together with various passive and additional active devices (Table 2) to support the circuit design activities in DOTFIVE. To avoid degradation of the electrical properties of the varactor diode and of the high voltage (HV) HBT, the 50 nm collector high speed HBT has been integrated together with these additional devices within the framework of a double collector epitaxy concept (see D2.4.2). The high voltage (HV) HBT has a transit frequency of 60 GHz, a collector/base breakdown voltage of 14 V and a collector/emitter breakdown voltage of 3.5 V. The varactor diode provides a capacitance tuning ratio of 2.3 and has a quality factor of 8 at 77 GHz. The two polysilicon resistors have sheet resistances of 150 Ω/sq and 1000 Ω/sq, respectively. The TaN metal resistor is placed between the first and the second metallization layer and has a sheet resistance of 20 Ω/sq.

1.7 Impact of the results

The results described above show that by evolutionary lateral and vertical scaling of the conventional DPSA HBT architecture, the DOTFIVE target of 2.5 ps for the ring oscillator gate delay time can be achieved. The conventional DPSA-SEG HBT has the advantage of an overall simple fabrication process. Since the DPSA-SEG architecture is already used for industrial production (e. g. B7HF200 at IFX, BiCMOS9MW at ST, ...) it benefits from proven manufacturability. The technology has been used in DOTFIVE at various development stages for benchmark and demonstration circuit fabrication in 3 design cycles. The fabricated WP5 circuits have shown very good performance results [5]-[8].

1.8 IPR

None.

1.9 Publishable information

The results, which we have described in this deliverable report, have been also included in an invited technology paper that will be published at the 2011 Bipolar/BICMOS Circuits and Technology meeting [1]. The organisation of the paper was led by ST and has been written in cooperation with all partners involved in WP2 and WP3 (ST, IFX, IHP, and IMEC). It presents the status of the technological developments done in the project.

1.10 Conclusion

In the report we have presented the results from evolutionary scaling of the conventional DPSA-SEG HBT for improvement of ring oscillator gate delay time and maximum oscillation frequency. Lateral scaling has allowed the fabrication of HBTs with an emitter window width of 230 nm and an emitter width of 130 nm together with strongly decreased overlaps in the emitter/base configuration. Vertical scaling included the development of new SiGe base profiles with increased Ge fraction, the investigation and improvement of the base link annealing cycles, as well as a significant reduction of collector thickness. SiGe HBTs with an emitter area A_E of 0.13 x 2.7 μm^2 have provided an f_T of 240 GHz, an f_{max} of 380 GHz, and a wafer average value of 2.38 ps for the ring oscillator gate delay time τ_D. These results strongly improve the high frequency performance of IFX's initial SiGe HBT technology B7HF200 in DOTFIVE. Moreover, they demonstrate that by evolutionary lateral and vertical scaling, the final DOTFIVE target of 2.5 ps for the ring oscillator gate delay time can be achieved with the conventional DPSA-SEG architecture. On contrary to the HBT developments in WP3, the other DOTFIVE performance target of 500 GHz f_{max} could not be realized by IFX with the DPSA-SEG HBT. In comparison with these WP3 HBT developments, the main disadvantage of the DPSA-SEG HBT is found to be the higher base link resistance together with the temperature budget, which is required for its reduction [1]. On the other hand the conventional DPSA-SEG HBT, which is used by ST (BiCMOS9MW) and IFX (B7HF200) already in production, benefits from a simpler fabrication process and proven manufacturability. It is worth to mention that the DPSA-SEG HBT technology was used in the project at various development stages for circuit fabrication and was capable to provide very good circuit results [5]-[8].

1.11 References

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Section 2 - ANNEX – IFX DPSA-SEG HBT fabrication process

The SEG-HBT fabrication process has been already described in detail in D2.3.2. For the fabrication of the scaled DPSA-SEG technology, whose results have been discussed before, in the meantime some changes in the fabrication process (outlined in D2.3.2) have been performed. These changes were a CoSi instead of a TiSi silicidation module and the emitter drive-in at a different process stage. Therefore, for completeness the DPSA-SEG fabrication process is shortly updated in this appendix.

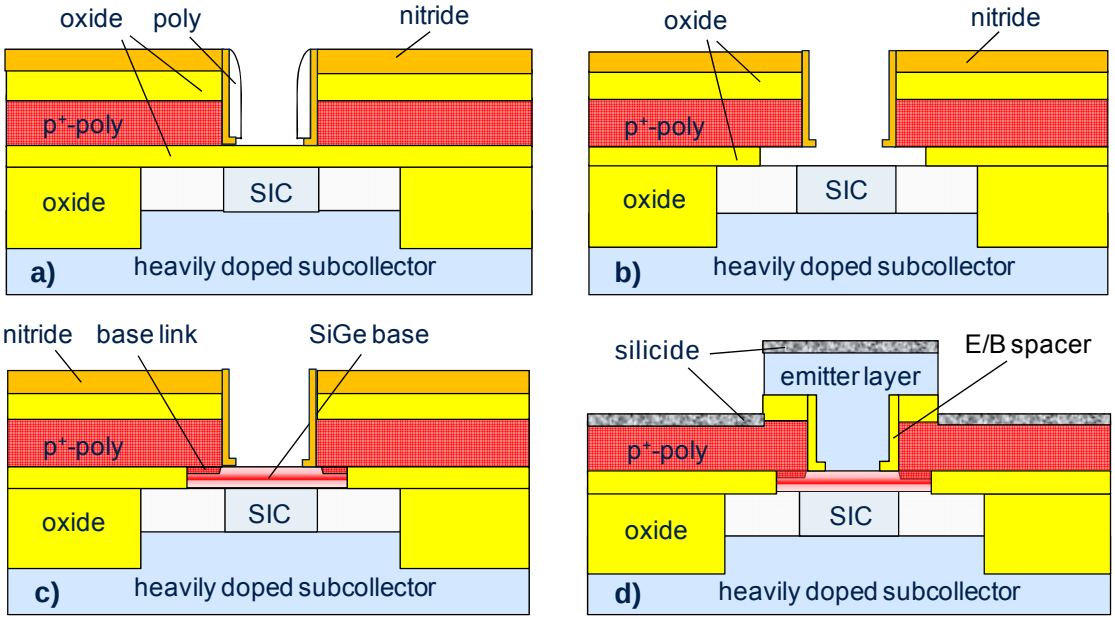

Fig. 1: DPSA-SEG fabrication process

The main fabrication steps are depicted in Fig. 1. It starts with the deposition of a pedestal oxide/p+-polysilicon/oxide/nitride stack in which an emitter window is opened by RIE, stopping on the pedestal oxide. Then a stack consisting of a nitride and a polysilicon layer is deposited and spacers - made of the material of the nitride/poly stack - are formed inside the emitter window by RIE. The self-aligned collector (SIC) is implanted into the emitter window by arsenic, using the nitride/poly spacer for reducing the width of the implantation area (Fig. 1a). After collector implantation the polysilicon material of the spacers is removed so that only L shaped nitride spacers are remaining at the sidewalls of the emitter window. Next steps are the wet removal of the pedestal oxide to form self-aligned adjusted p+-polysilicon overhangs (Fig. 1b), which is followed by the deposition of the SiGe base by selective epitaxial growth (Fig. 1c). Now the thin nitride spacers and the sacrificial nitride layer on top of the emitter/base stack are removed and subsequently the emitter/base spacer is formed. At this process stage the base link anneal is done usually at 1040°C/5. The base link anneal serves to diffuse boron from the p+-polysilicon into the base link region to reduce the resistance of that region. The next steps are the deposition and patterning of the heavily arsenic (1.4×10^{21} cm^{-3}) and carbon doped emitter layer which is followed by the emitter drive-in. The emitter drive-in has been done at comparatively low RTP anneal temperatures around 930°C/3s. SiGe HBT processing is completed by silicidation with Co (Fig. 1d) and the formation of the metallisation. The sheet resistance of the Co silicided p+-polysilicon region has been adjusted to ~3 Ω/sq.